ECM-3612

All-in-One VIA Eden ESP6000 Single Board with LCD, Dual LVDS, AC97 Audio, 10/100Base-Tx Ethernet, 4 COM & 2 USB 1.1

User's Manual

1st Ed – 26 May 2005

Part No. 2047361200

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(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

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Headquarters
Evalue Technology Inc.
7F, 228, Lian-cheng Road,
Chung Ho City, Taipei,
Taiwan
Tel : +886-2-8226-2345
Fax : +886-2-8226-2777
http://www.evalue-tech.com
E-mail: service@evalue-tech.com

Europe Branch Office
Evalue Europe A/S
Nordre Strandvej 119C,
3150 Hellebaek,
Denmark
Tel : +45-7025-0310
Fax : +45-4975-5026
http://www.evalue-tech.com
E-mail: service.europe@evalue-tech.com

China Branch Office
Evalue Technology Shanghai Inc.
Room 909, 9F, Section B, No.900,
Yisan Road, Caohejing Hi-tech Park,
Shanghai 200233, China
Tel : +86-21-5423-4170
Fax : +86-21-5423-4171
http://www.evalue-tech.com
E-mail: service.china@evalue-tech.com

US Branch Office
Evalue Technology Inc.
Suite 210, 200 Tornillo Way,
Tinton Falls, NJ 07712
USA
Tel: +1-732-578-0200
Fax: +1-732-578-0250
http://www.evalue-tech.com
E-mail: service.usa@evalue-tech.com

Product Warranty

Evalue warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Evalue, or which have been subject to misuse, abuse, accident or improper installation. Evalue assumes no liability under the terms of this warranty as a consequence of such events. Because of Evalue's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If any of Evalue's products is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details. If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU type and speed, Evalue's products model name, hardware & BIOS revision number, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information available.
3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.
4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Contents

1. Getting started

1.1 Safety Precautions

Warning!

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ECM-3612 All-in-One VIA Eden ESP 6000 Computing Module
- 1 x Quick Installation Guide for ECM-3612
- 1 x Quick Installation Guide for AUX-001 daughter board
- 1 x Audio jacks and USB connector daughter board (AUX-001)
- 1 x CD-ROM(or DVD-ROM) contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities
- 1 x Cable set includes the followings:
  - 1 x PS/2 keyboard and mouse Y cable (6P-6P-6P, Mini-DIN)
  - 1 x IDE HDD cable (40P/2.54mm-40P/2.54mm-40P/2.54mm)
  - 1 x Bracket with one printer port cable (26P/2.0mm) and one serial port cable (10P/2.0mm)
  - 2 x Serial port cables (9P/Mini-DIN - Dupont 10P/2.0mm)
  - 2 x Audio or USB cables (10P/2.0mm-10P/2.0mm)

If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	By	Comment
1st	May 2005	Vicky Lin	Initial Release

1.4 Manual Objectives

This manual describes in detail the Evalue Technology ECM-3612 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ECM-3612 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

1.5 System Specifications

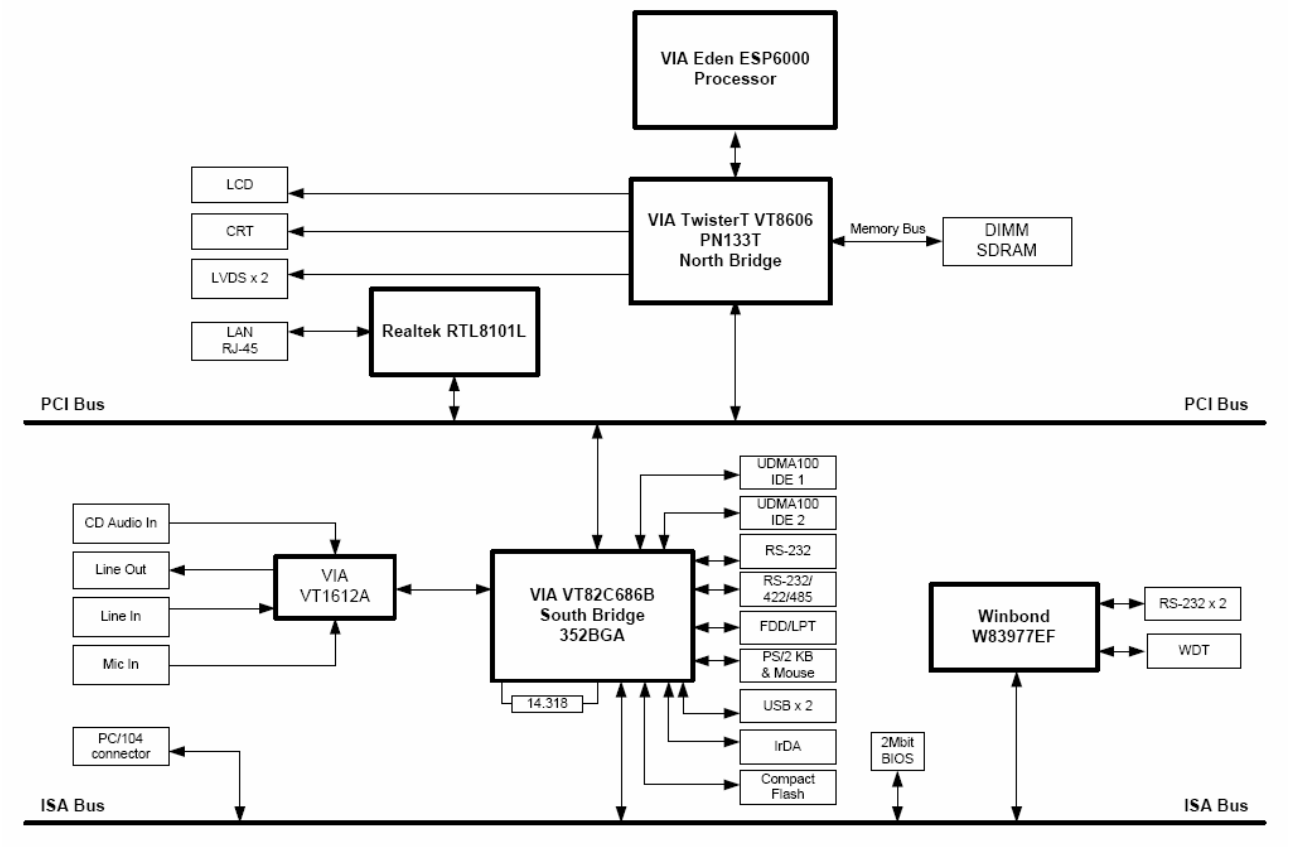
System	
CPU	Onboard VIA Eden ESP6000 667 MHz Note: Available in different CPU speeds by request
FSB	66/100/133 MHz
BIOS	Award 256 KB Flash BIOS
System Chipset	VIA TwisterT VT8606/VT82C686B
I/O Chip	VIA VT82C686B / Windbond W83977EF
System Memory	Onboard 128 MB SDRAM (32/64 MB by request)
SSD	One CompactFlash Type I/II socket
Watchdog Timer	Reset: 32 sec.~254 min., 1 min./step
H/W Status Monitor	Monitoring system temperature, voltage, and cooling fan status. Auto throttling control when CPU overheats.
Expansion	One PC/104 connector
I/O	
MIO	2 x EIDE (Ultra DMA 100), 1 x LPT, 3 x RS-232, 1x RS-232/422/485, 1 x K/B & Mouse
IrDA	115k bps, IrDA 1.0 compliant
USB	2 USB 1.1 ports
Display	
Chipset	VIA VT8606 TwisterT with integrated 2D/3D graphics engine
Display Memory	8/16/32 MB frame buffer using system memory
Resolution	CRT mode: 1280 x 1024 @ 32 bpp (85 Hz) LCD/Simultaneous mode: 1280 x 1024 @ 32 bpp (85 Hz)
VGA/LCD Interface	AGP 4x VGA/LCD interface
LVDS	VIA VT8606 supports dual-channel 18-bit LVDS panels
Audio	
Chipset	VIA VT82C686B
AC97 Codec	VIA VT1612A
Audio Interface	Mic in, Line in, CD Audio in, Line out

Ethernet	
Chipset	Realtek RTL8101L
Ethernet Interface	IEEE 802.3u 100Base-Tx Fast Ethernet compatible
Remote Boot ROM	Optional built-in boot ROM in Flash BIOS
Mechanical & Environmental	
Power Requirement	+5 V @ 2.15 A, +12 V @ 0.06 A (with VIA Eden ESP6000 CPU & onboard 64M SDRAM)
Power Type	AT/ATX
Operation Temperature	0~60® C (32~140® F)
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	5.7" x 4" (146 mm x 101mm)
Weight	0.44 lbs (0.2 Kg)

1.6 Architecture Overview

1.6.1 Block Diagram

The following block diagram shows the architecture and main components of ECM-3612.



The following sections provide detail information about the functions provided onboard.

1.6.2 VIA TwisterT VT8606 (ProSavage PN133T Chipset)

The VIA Apollo PLE133T combines integrated AGP 4X graphics and AC'97 audio capabilities with support for PC133 SDRAM to provide a highly scalable solution for building Value PCs using the industry standard Socket 370 platform. The VIA Apollo PLE133T is also fully compatible with both the Intel® Pentium® III and Intel® Celeron™ processors, as well as the VIA C3™ processor. Its support for PC133 SDRAM ensures memory bandwidth for Internet applications at minimal cost. In combination with the VIA VT82C686B South Bridge Controller, the VIA PLE133T includes integrated 10/100 BaseT Ethernet and home PNA controller, AC'97 audio, MC'97 modem, Super I/O, hardware monitoring capabilities, and support for four USB ports, ATA-100, and Advanced Power Management. The following functionality listed below:

- Supports Intel® Celeron™, Intel® Pentium™ III (including Tualatin), and VIA C3™ processors
- 66/100/133MHz FSB settings
- Integrated AGP 4X graphics core
- Support for PC100/133 SDRAM
- Support for Advanced Communications Riser (ACR)
- Integrated AC'97, MC'97 Audio/Modem
- Integrated 10/100Mb BaseT Ethernet controller or 1/10Mb Home PNA
- Support for ATA 33/66
- 4 USB ports, UHCI compliant
- Integrated Super I/O
- Support for LPC (Low Pin Count) bus Support for CRT, Digital Flat Panel and TV display
- Integrated hardware monitoring
- Advanced power management capabilities
- 510-pin BGA VT8602 North Bridge
- 376-pin BGA VT82C686B South Bridge

Featuring a new super-pipelined 128-bit engine, TwisterT utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. TwisterT also offers the industry’ s only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. TwisterT further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. TwisterT’ s advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

TwisterT' s advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to optimize SMA performance and to provide acceleration in all color depths.

TwisterT supports a wide variety of DSTN or TFT panels through a 36-bit CMOS interface. This includes support for VGA, SVGA, XGA, and SXGA+ TFT color panels with 9-bit, 12-bit, 18-bit (both 1 pixel/clock and 2 pixels/clock), and 24-bit CMOS interfaces. Enhanced STN hardware with 256 gray scale support and advanced frame rate control to provide up to 16.7 million colors. In addition, the integrated 2-channel LVDS interface can support 18-bit color panels. All resolutions are supported up to SXGA+ (1400x1050). The integrated ZV-Port allows display of video from an external source.

1.6.3 VIA VT82C686B South Bridge

The VT82C686B PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686B includes standard intelligent peripheral controllers:

- Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C686B also supports the UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput. The VT82C686B also supports the UltraDMA-66 and UltraDMA-100 (ATA-100) standards. The IDE controller is SFF-8038I v1.0 and Microsoft Windows-family compliant.
- Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686B includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.
- Keyboard controller with PS2 mouse support.

- Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard. Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.
- Hardware monitoring subsystem for managing system / motherboard voltage levels, temperatures, and fan speeds
- Full System Management Bus (SMBus) interface.
- Two 16550-compatible serial I/O ports with infrared communications port option on the second port.
- Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.
- Two game ports and one MIDI port
- ECP/EPP-capable parallel port
- Standard floppy disk drive interface
- Distributed DMA capability for support of ISA legacy DMA over the PCI bus. Serial IRQ is also supported for docking and non-docking applications.
- Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of onboard peripherals for Windows family compliance.
- Internal I/O APIC (Advanced Programmable Interrupt Controller)

The VT82C686B also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT82C686B supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (doublewords) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

1.6.4 VIA VT1612A

The VIA VT1612A Audio Codec conforms to the AC'97 2.2 specification providing 18-bit resolution performance. With 2 channel outputs the VIA VT1612A provides high-performance stereo quality for headphones or speaker connections. Furthermore, an integrated headphone amplifier with thermal shutdown reduces the need for further external components. The VIA VT1612A includes analog mixer circuitry for stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. For a completely digital audio path the VIA VT1612A includes an integrated IEC958 line driver for S/PDIF compressed digital or LPCM audio out.

Four stereo and 2 mono audio inputs provided by the VIA VT1612A enable connections to a wide range of audio inputs such as microphones, line inputs, and phone connections. Sample rate converters in the VIA VT1612A can be adjusted in 1Hz increments providing maximum recording manipulation capabilities, and hardware VU peak meters are provided for PCM streams.

For maximum ease of integration the VIA VT1612A is designed with aggressive power management to achieve low power consumption. When used with a 3.3v analog power supply, the power consumption can be further reduced. The VIA VT1612A is available in a small footprint 48-pin LQFP package. Typical applications of the VIA VT1612A include integration into audio on motherboard solutions, add-in cards, and other audio subsystems that require stereo I/O with S/PDIF digital outputs.

- 18-bit independent rate stereo ADC/DAC
- 18-bit stereo full duplex
- 1 Hz resolution VSR (Variable Sampling Rate)
- Integrated IEC958 line driver for S/PDIF
- S/PDIF compressed digital or LPCM audio out
- Hardware VU peak meters for PCM streams
- 2 stereo, 2 mono analog line-level inputs
- Alt. Line-level output with volume control
- AC'97 2.2 S/PDIF extension compliant codec
- 3D stereo expansion for simulated surround
- Headphone Amplifier with Thermal Protection
- Exceeds Microsoft® WHQL logo requirements
- 48-pin LQFP small footprint package
- Low Power consumption mode
- 3.3V digital, 3.3 or 5V analog power supply

1.6.5 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation. The VT82C686B also supports the UltraDMA-33, UltraDMA-66, and UltraDMA-100 (ATA-100) standards. The IDE controller is SFF-8038I v1.0 and Microsoft Windows-family compliant.

1.6.6 USB

Universal Serial Bus controller is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686B includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

1.6.7 Ethernet

1.6.7.1 Realtek RTL8101L Ethernet Controller

The Realtek RTL8101L is a highly integrated and cost-effective single-chip Fast Ethernet controller. Featuring an MC'97 interface, the device is able to provide a combo-solution for LAN and software modem applications. It is equipped with a PCI and Boot ROM share interface (Realtek patent pending) for both EPROM and Flash Memory to provide maximum network security and ease of management.

The RTL8101L offers an ACPI (Advanced Configuration Power Interface) management function to provide efficient power management for advanced operating systems with OSPM (Operating System Directed Power Management). A remote wake-up function is also provided by support to Magic Packet, Link Change, and Wake-up Frame to increase cost-efficiency in network maintenance and management. In addition, it supports analog Auto Power-down and provides an auxiliary power auto-detect function to further save power.

1.6.8 Winbond W83977EF

The W83977EF is an evolving product from Winbond's most popular I/O chip W83877F which integrates the disk drive adapter, serial port (UART), IrDA 1.0 SIR, parallel port, and configurable plug-and-play registers for the whole chip --- plus additional powerful features: ACPI, 8042 keyboard controller with PS/2 mouse support, 14 general purpose I/O ports, full 16-bit address decoding, OnNow keyboard Wake-Up, and OnNow mouse Wake-Up.

The disk drive adapter functions of W83977EF include a floppy disk drive controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83977EF greatly reduces the number of components required for interfacing with floppy disk drives. The W83977EF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83977EF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems.

The W83977EF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode, allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95TM, which makes system resource allocation more efficient than ever.

W83977EF provides functions that comply with ACPI (Advanced Configuration and Power Interface), including support for legacy and ACPI power management through SMI or SCI function pins. W83977EF also has auto power management to reduce power consumption.

The keyboard controller is based on 8042 compatible instruction set, with a 2K Byte programmable ROM and a 256-Byte RAM bank. Keyboard BIOS firmware is available with optional AMIKEYTM-2, Phoenix MultiKey/42TM, or customer code.

The W83977EF provides the system designer with a set of flexible I/O control functions through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O, or may be individually configured to provide a predefined alternate function.

The W83977EF also supports Power-loss control, and ensures that the system never fails to detect any Wake-Up event provided by a chipset such as INTEL PIIX4 TM.
W83977EF is made to fully comply with Microsoft PC98 Hardware Design Guide. IRQs, DMAs, and I/O space resource are flexible to adjust to meet ISA PnP requirements.
Moreover, W83977EF is made to meet the specification of PC98's requirements in power management: ACPI and DPM (Device Power Management).
Another benifit is that W83977EF has the same pin assignment as W83977AF, W83977F, W83977TF, W83977ATF. This makes the design very flexible.
The features are as below:

- Plug & Play 1.0A compatible
- Supports 12 IRQs, 4 DMA channels, full 16-bit address decoding
- Capable of ISA Bus IRQ Sharing
- Compliant with Microsoft PC98 Hardware Design Guide
- Supports DPM (Device Power Management), ACPI
- Reports ACPI status interrupt by SCI# signal issued from any of the 12 IQRs pins or GPIO xx
- Programmable configuration settings
- Single 24/48 Mhz clock input

1.6.9 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

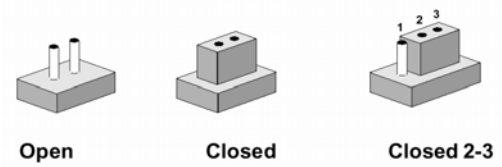
2. Hardware Configuration

2.1 Product Overview

2.2 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip. To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

The following tables list the function of each of the board's jumpers and connectors.

Jumpers

Label	Function	Note
ATATX1	AT/ATX power select	3 x 1 header, pitch 2.0mm
J3	COM2 – RS-232/422/485 select	4 x 3 header, pitch 2.00mm
J4	Clear CMOS	3 x 1 header, pitch 2.54mm
J5	COM2 – RS-232/422/485 select	3 x 2 header, pitch 2.00mm
J6	COM1 – Ring, +12V, +5V Select	3 x 2 header, pitch 2.00mm

Connectors

Label	Function	Note
CM1	Serial port 3 connector in RS-232 mode	5 x 2 header, pitch 2.0mm
CM2	Serial port 1 connector in RS-232 mode	9-pin male D-sub connector
CM3	Serial port 4 connector in RS-232 mode	5 x 2 header, pitch 2.0mm
CM4	Serial port 2 connector in RS-232/422/485 mode	5 x 2 header, pitch 2.0mm
CN1	IDE connector	20 x 2 header, pitch 2.54mm
CN2	CPU fan connector	2 x 1 wafer, pitch 2.54mm
CN3	10/100Base-Tx Ethernet connector	RJ-45
CN4	CD-ROM audio input connector	4 x 1 wafer, pitch 2.0mm
CN5	Audio connector	5 x 2 header, pitch 2.0mm
CN6	Primary LCD panel connector	HIROSE DF13-40DP-1.25V
CN7, CN10	PC/104+ connector	
CN8	Secondary LCD panel connector	HIROSE DF13-40DP-1.25V
CN9	IrDA connector	5 x 1 header, pitch 2.0mm
J1	LCD inverter connector	5 x 1 wafer, pitch 2.0mm
J2	Auxiliary Power Connector	3 x 1 wafer, pitch 2.54mm
J9	ATX Soft-power Connector	2 x 1 header, pitch 2.0mm
J11	(J11 is reserved for printer compatibility use)	2 x 2 header, pitch 2.0mm
KB1	Keyboard and PS/2 mouse connector	6-pin mini DIN
PNT1	Parallel port connector	13 x 2 header, pitch 2.0mm
PWR1	Primary power connector	
PWR2	Secondary power connector	4 x 1 wafer, pitch 2.0mm
SN1	Compact Flash connector (Rear side)	
SW1	(Reserved)	
USB1	USB connector	5 x 2 header, pitch 2.0mm
VGA1	CRT connector	DB-15 female connector
VR1	LCD backlight brightness adjustment connector	3 x 1 header, pitch 2.54mm

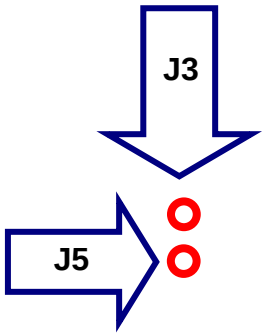
USB1

2.3 Setting Jumpers & Connectors

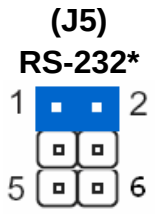
2.3.1 AT/ATX Power Select (ATATX1)

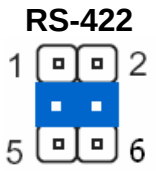
*** Default**

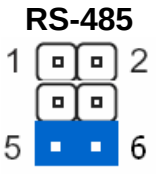
2.3.2 COM2 – RS-232/422/485 Select (J3, J5)

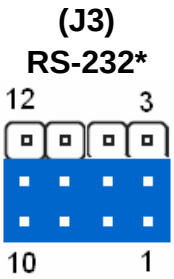


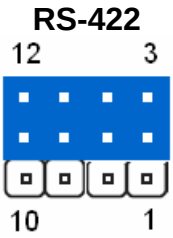
*** Default**

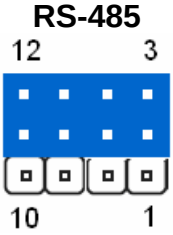










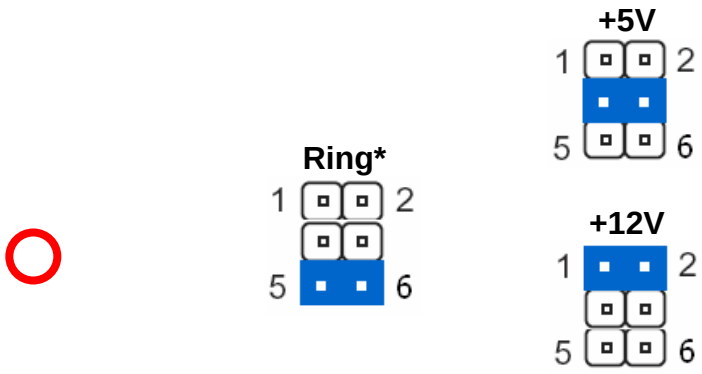


2.3.3 Clear CMOS (J4)

*** Default**

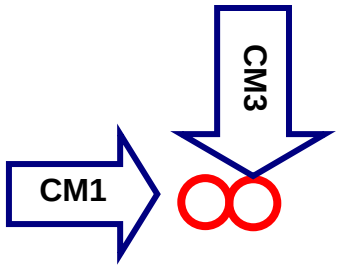
Note: You can use J4 to clear the CMOS data if necessary. To reset the CMOS data, set J4 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed.

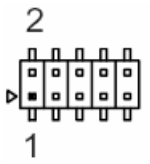
2.3.4 COM1 – Ring, +12V, +5V Select (J6)



*** Default**

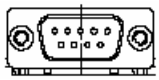
2.3.5 Serial Port 3 / Port 4 Connector in RS-232 Mode (CM1, CM3)





Signal	PIN	PIN	Signal
DCD	1	2	RxD
TxD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI	9	10	NC

2.3.6 Serial Port 1 Connector in RS-232 Mode (CM2)



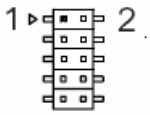
Signal	PIN	PIN	Signal
DCD	1		
		6	DSR
RxD	2		
		7	RTS
TxD	3		
		8	CTS
DTR	4		
		9	RI
GND	5		

2.3.6.1 Signal Description –Serial Port 3/4/1 Connector in RS-232 Mode (CM1, CM3, CM2)

Signal	Signal Description
TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

2.3.7 Serial Port 2 Connector in RS-232/422/485 Mode (CM4)

2.3.7.1 Serial Port 2 Connector in RS-232 Mode

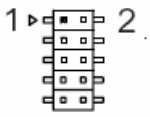


Signal	PIN	PIN	Signal
DCD	1	2	RxD
TxD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI	9	10	NC

2.3.7.1.1 Signal Description – Serial Port 2 Connector in RS-232 Mode (CM4)

Signal	Signal Description
TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

2.3.7.2 Serial Port 2 Connector in RS-422 Mode

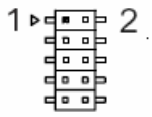


Signal	PIN	PIN	Signal
Tx-	1	2	Rx+
Tx+	3	4	Rx-
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC

2.3.7.2.1 Signal Description – Serial Port 2 Connector in RS-422 Mode (CM4)

Signal	Signal Description
Tx +/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the RTS register of the Serial Port 2 is set to LOW.
Rx +/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.

2.3.7.3 Serial Port 2 Connector in RS-485 Mode

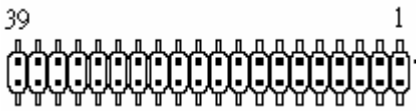


Signal	PIN	PIN	Signal
DATA-	1	2	NC
DATA+	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC

2.2.7.3.1 Signal Description – Serial Port 2 Connector in RS-485 Mode (CM4)

Signal	Signal Description
DATA +/-	This differential signal pair sends and receives serial data to the communication link. The mode of this differential signal pair is controlled through the RTS register of Serial Port 2. Set the RTS register of the Serial Port 2 to LOW for transmitting, HIGH for receiving.

2.3.8 IDE Connector (CN1)



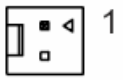
Signal	PIN	PIN	Signal
RESET#	1	2	GND
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
GND	19	20	NC
PDREQ	21	22	GND
PDIOW#	23	24	GND
PDIOR#	25	26	GND
PIORDY	27	28	GND
PDDACK#	29	30	GND
IRQ14	31	32	NC
PDA1	33	34	NC
PDA0	35	36	PDA2
	37	38	PDCS3#
IDEACTP#	39	40	GND

2.3.8.1 Signal Description – IDE Connector (CN1)

The IDE interface supports PIO modes 0 to 4 and Bus Master IDE. Data transfer rates up to 100 MB/Sec is possible.

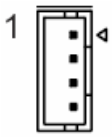
Signal	Signal Description
PDA [2:0]	IDE Address Bits. These address bits are used to access a register or data port in a device on the IDE bus.
PDCS1#, PDCS3#	IDE Chip Selects. The chip select signals are used to select the command block registers in an IDE device. DCS1# selects the primary hard disk.
PDD [15:0]	IDE Data Lines. D [15:0] transfers data to/from the IDE devices.
PIOR#	IDE I/O Read. Signal is asserted on read accesses to the corresponding IDE port addresses.
PIOW#	IDE I/O Write. Each signal is asserted on write accesses to corresponding the IDE port addresses.
PIORDY	When deasserted, these signals extend the transfer cycle of any host register access when the device is not ready to respond to the data transfer request.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14	Interrupt line from hard disk. Connected directly to PC-AT bus.
PDREQ	The DREQ is used to request a DMA transfer from the South Bridge. The direction of the transfers is determined by the IOR#/IOW# signals.
PDACK#	DMA Acknowledge. The DACK# acknowledges the DREQ request to initiate DMA transfers.
IDEACTP#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signal is routed directly to the LED1.

2.3.9 CPU Fan Connector (CN2)



PIN	Signal
1	GND
2	+5V

2.3.10 CD-ROM Audio Input Connector (CN4)

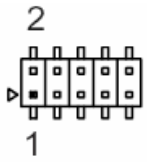


PIN	Signal
1	CD_GND
2	CD_L
3	CD_GND
4	CD_R

2.3.10.1 Signal Description – CD-ROM Audio Input Connector (CN4)

Signal	Signal Description
CD_R	Right CD-IN signal
CD_L	Left CD-IN signal

2.3.11 Audio Connector (CN5)

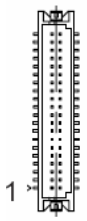


Signal	PIN	PIN	Signal
Line out R	1	2	Line out L
GND	3	4	GND
Line in R	5	6	Line in L
Mic In	7	8	Mic Bias
NC	9	10	NC

2.3.11.1 Signal Description – Audio Connecter (CN5)

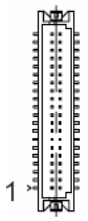
Signal	Signal Description
Mic / Mic Bias	The MIC signal is used for microphone input. This input is fed to the left microphone channel. Mic Bias provides 3.3V supplied through 3.2K Ω with capacitive decoupling to GND. This signal may be used for bias of some microphone types.
Line-In L/R	Left and right line in signals.
Line-Out L/R	Left and right line out signals. Both signals are capacitor coupled and should have GND as return.

2.3.12 Primary LCD Panel Connector (CN6)



Signal	PIN	PIN	Signal
ENBKL	39	40	ENVEE
M	37	38	LP
SHFCLK	35	36	FLM
GND	33	34	GND
P22	31	32	P23
P20	29	30	P21
P18	27	28	P19
P16	25	26	P17
P14	23	24	P15
P12	21	22	P13
P10	19	20	P11
P8	17	18	P9
P6	15	16	P7
P4	13	14	P5
P2	11	12	P3
P0	9	10	P1
Vcon	7	8	GND
3.3V	5	6	3.3V
GND	3	4	GND
5V	1	2	5V

2.3.13 Secondary LCD Panel Connector (CN8)



Signal	PIN	PIN	Signal
Y1P	39	40	Y1M
Z2P	37	38	Z2M
Y0P	35	36	Y0M
GND	33	34	GND
YCP	31	32	YCM
Z0P	29	30	Z0M
ZCP	27	28	ZCM
Z1P	25	26	Z1M
Y2P	23	24	Y2M
GND	21	22	GND
P34	19	20	P35
P32	17	18	P33
P30	15	16	P31
P28	13	14	P29
P26	11	12	P27
P24	9	10	P25
Vcon	7	8	GND
3.3V	5	6	3.3V
GND	3	4	GND
5V	1	2	5V

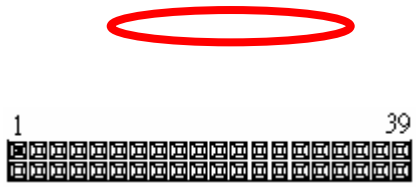
2.3.13.1 Signal Description – Primary & Secondary LCD Panel Connector (CN6, CN8)

Signal	Signal Description
P [35:0]	Flat Panel Data Bit 35 to Bit 0 for panel implementation.
SHFCLK	Shift Clock. Pixel clock for flat panel data
LP	Latch Pulse. Flat panel equivalent of HSYNC (horizontal synchronization)
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronization)
M	Multipurpose signal, function depends on panel type. May be used as AC drive control signal or as BLANK# or Display Enable signal
ENBKL	Enable backlight signal. This signal is controlled as a part of the panel power sequencing
ENVEE	Enable VEE. Signal to control the panel power-on/off sequencing. A high level may turn on the VEE (LCD bias voltage) supply to the panel
Y[2:0]P, Z[2:0]P	1st & 2nd Channel Positive LVDS differential data output
Y[2:0]M, Z[2:0]M	1st & 2nd Channel Negative LVDS differential data output
YCP, ZCP	1st & 2nd Channel Positive LVDS differential clock output
YCM, ZCM	1st & 2nd Channel Negative LVDS differential clock output

2.3.14 PC/104+ Connector (CN7)

Signal	PIN	PIN	Signal
GND	2	1	IOCHCHK#
PC104RST	4	3	SD7
+5V	6	5	SD6
IRQ9	8	7	SD5
-5V	10	9	SD4
DRQ2	12	11	SD3
-12V	14	13	SD2
#OWS	16	15	SD1
+12V	18	17	SD0
GND	20	19	IOCHRDY
SMEMW#	22	21	AEN
SMEMR#	24	23	SA19
IOW#	26	25	SA18
IOR#	28	27	SA17
DACK#3	30	29	SA16
DRQ3	32	31	SA15
DACK#1	34	33	SA14
DRQ1	36	35	SA13
REFRESH#	38	37	SA12
SYSCLK	40	39	SA11
IRQ7	42	41	SA10
IRQ6	44	43	SA9
IRQ5	46	45	SA8
IRQ4	48	47	SA7
IRQ3	50	49	SA6
NC	52	51	SA5
TC	54	53	SA4
BALE	56	55	SA3
+5V	58	57	SA2
OSC	60	59	SA1
GND	62	61	SA0
GND	64	63	GND

2.3.15 PC/104+ Connector (CN10)



Signal	PIN	PIN	Signal
GND	2	1	GND
MEMCS16#	4	3	#SBHE
IOCS16#	6	5	LA23
IRQ10	8	7	LA22
IRQ11	10	9	LA21
IRQ12	12	11	LA20
IRQ15	14	13	LA19
IRQ14	16	15	LA18
DACK#0	18	17	LA17
DRQ0	20	19	MEMR#
DACK#5	22	21	MEMW#
DRQ5	24	23	SD8
DACK#6	26	25	SD9
DRQ6	28	27	SD10
DACK#7	30	29	SD11
DRQ7	32	31	SD12
+5V	34	33	SD13
MASTER#	36	35	SD14
GND	38	37	SD15
GND	40	39	NC

2.3.15.1 Signal Description – PC/104+ Connecter (CN7, CN10)

<table>
<tr><th>Signal</th><th>Signal Description</th></tr>
<tr><td>LA[23:17]</td><td>The address signals LA [23:17] define the selection of a 128KB section of memory space within the 16MB address range of the 16-bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case, the temporary master drives these lines. The LA signals are not defined for I/O accesses.</td></tr>
<tr><td>SA[19:0]</td><td>System address. Address lines for the first one Megabyte of memory. SA [9:0] used for I/O addresses. SA0 is the least significant bit.</td></tr>
<tr><td>SBHE#</td><td>This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD [15:8)) of the 16 bit bus. All bus masters will drive this line with a tri-state driver.</td></tr>
<tr><td>SD[15:8]</td><td>These signals are defined for the high order byte of the 16-bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.</td></tr>
<tr><td>SD[7:0]</td><td>These signals are defined for the low order byte of the 16-bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8-bit operations with even or odd addresses and for 16-bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus:
<table>
<tr><th>SBHE#</th><th>SA0</th><th>SD15-SD8</th><th>SD7-SD0</th><th>Action</th></tr>
<tr><td>0</td><td>0</td><td>ODD</td><td>EVEN</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>ODD</td><td>ODD</td><td>Byte transfer on SD15-SD8</td></tr>
<tr><td>1</td><td>0</td><td>-</td><td>EVEN</td><td>Byte transfer on SD7-SD0</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>ODD</td><td>Byte transfer on SD7</td></tr>
</table></td></tr>
<tr><td>BALE</td><td>This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA, refresh and alternate master cycles, BALE is forced high for the duration of the transfer. BALE is driven by the permanent master with a totem-pole driver.</td></tr>
</table>

Signal	Signal Description
IOR#, IOW#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with DACKn# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#, SMEMW#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#, MEMW#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16-bit device. This open collector signal is driven, based on SA [15:0] only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16-bit device. This open collector signal is driven, based on LA [23:17] only.
OWS#	This signal is an active low open-collector signal asserted by a 16-bit memory mapped device that may cause an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a nonmaskable interrupt.

Signal	Signal Description
SYSCLK	This clock signal may vary in frequency from 2.5 MHz to 25.0 MHz depending on the setup made in the BIOS. Frequencies above 16 MHz are not recommended. The standard states 6 MHz to 8.33 MHz, but most new adapters are able to handle higher frequencies. The PCAT/PC104 bus timing is based on this clock signal.
OSC	This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The signal is driven by the permanent master.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.
IRQ[3:7], IRQ[9:12], IRQ[14:15]	These signals are active high signals, which indicate the presence of an interrupting PCAT/PC104 bus adapter. Due to the use of pull-ups, unused interrupt inputs must be masked.
DRQ[0:3], DRQ[5:7]	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ [0:3] request 8 bit DMA operations, while DRQ [5:7] request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any, are requesting the bus.
DACK[0:3]#, DACK[5:7]#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the address lines are driven by the DMA controller. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active DACKn# should respond.
REFRESH#	This is an active low signal driven by the current master to indicate a memory refresh operation. The current master will drive this line with a tri-state driver.
TC	This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. DACKn# must be presented by the bus adapter to validate the TC signal.
MASTER#	This signal is not supported by the chipset.

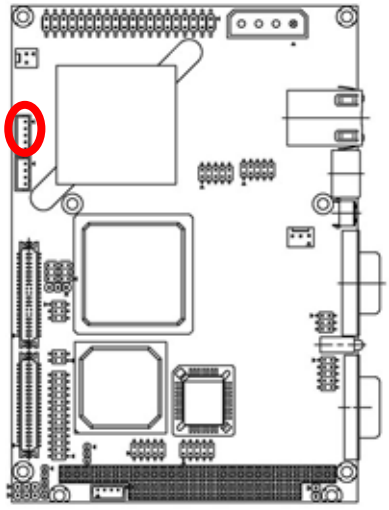
2.3.16 IrDA Connector (CN9)

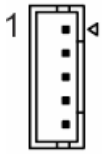
PIN	Signal
1	+5V
2	NC
3	IRRX
4	GND
5	IRTX

2.3.16.1 Signal Description – IrDA Connector (CN9)

Signal	Signal Description
IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

2.3.17 LCD Inverter Connector (J1)





PIN	Signal
1	+12V
2	GND
3	ENBKL
4	VR
5	+5V

Note: For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal (pin 4) controlled by **VR1** Please see the **VR1** section for detailed circuitry information.

2.3.17.1 Signal Description – LCD Inverter Connecter (J1)

Signal	Signal Description
VR	Vadj = 5V ~ 0V.
ENBKL	LCD backlight ON/OFF control signal.

2.3.18 Auxiliary Power Connector (J2)

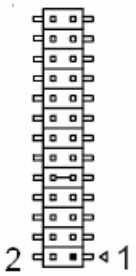
PIN	Signal
3	VCCSB
2	+5V
1	PSON#

Note: To use ATX Power supply, connect pin 3 to ATX power supply VCCSB and pin 1 to ATX power supply PSON. Set J2 to 2-3 closed, If AT power supply is to be used.

2.3.19 ATX Soft-power Connector (J9)

PIN	Signal
1	PWRBTN
2	GND

2.3.20 Parallel Port Connector (PNT1)



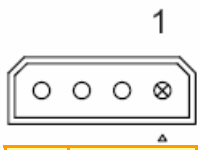
Signal	PIN	PIN	Signal
NC	26	25	SLCT
GND	24	23	PE
GND	22	21	BUSY
GND	20	19	ACK#
GND	18	17	PPD7
GND	16	15	PPD6
GND	14	13	PPD5
GND	12	11	PPD4
GND	10	9	PPD3
SLIN#	8	7	PPD2
INIT#	6	5	PPD1
ERR#	4	3	PPD0
AFD#	2	1	STB#

2.3.20.1 Signal Description – Parallel Port Connecter (PNT1)

The following signal description covers the signal definitions, when the parallel port is operated in standard centronic mode. The parallel port controller also supports the fast EPP and ECP modes.

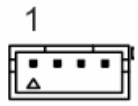
Signal	Signal Description
PD[7:0]	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

2.3.21 Primary Power Connector (PWR1)



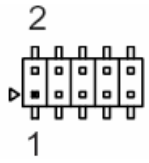
PIN	Signal
4	+5V
3	GND
2	GND
1	+12V

2.3.22 Secondary Power Connector (PWR2)



PIN	Signal
1	-5V
2	GND
3	GND
4	-12V

2.3.23 USB Connector (USB1)

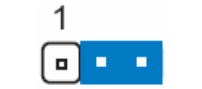


Signal	PIN	PIN	Signal
VCC1	1	2	GND
D1-	3	4	GND
D1+	5	6	D2+
GND	7	8	D2-
GND	9	10	VCC2

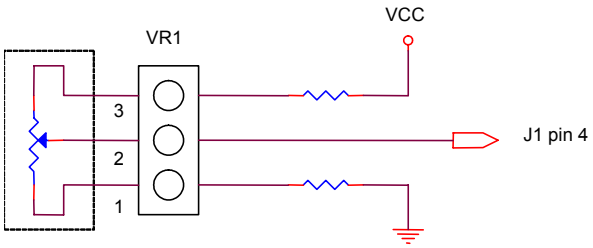
2.3.23.1 Signal Description – USB Connector (USB1)

Signal	Signal Description
D1+ / D1-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D2+ / D2-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
VCC	5 V DC supply for external devices. Maximum load according to USB standard.

2.3.24 LCD Backlight Brightness Adjustment Connector (VR1)

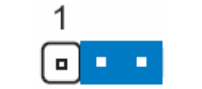


PIN	Signal
1	GND
2	VR
3	VCC



Variation Resistor (Recommended: 4.7KΩ, >1/16W)

2.3.25 STN LCD Contrast Adjustment Connector (VR2)



PIN	Signal
1	GND
2	Vcon
3	VCC3

3. BIOS Setup

3.1 Starting Setup

The AwardBIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 to Continue, DEL to enter SETUP

3.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Button	Description
↑	Move to previous item
↓	Move to next item
←	Move to the item in the left hand
→	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

- **Navigating Through The Menu Bar**

  Use the left and right arrow keys to choose the menu you want to be in.

Note: Some of the navigation keys differ from one screen to another.

- **To Display a Sub Menu**
  Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "➢" pointer marks all sub menus.

3.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

3.4 In Case of Problems

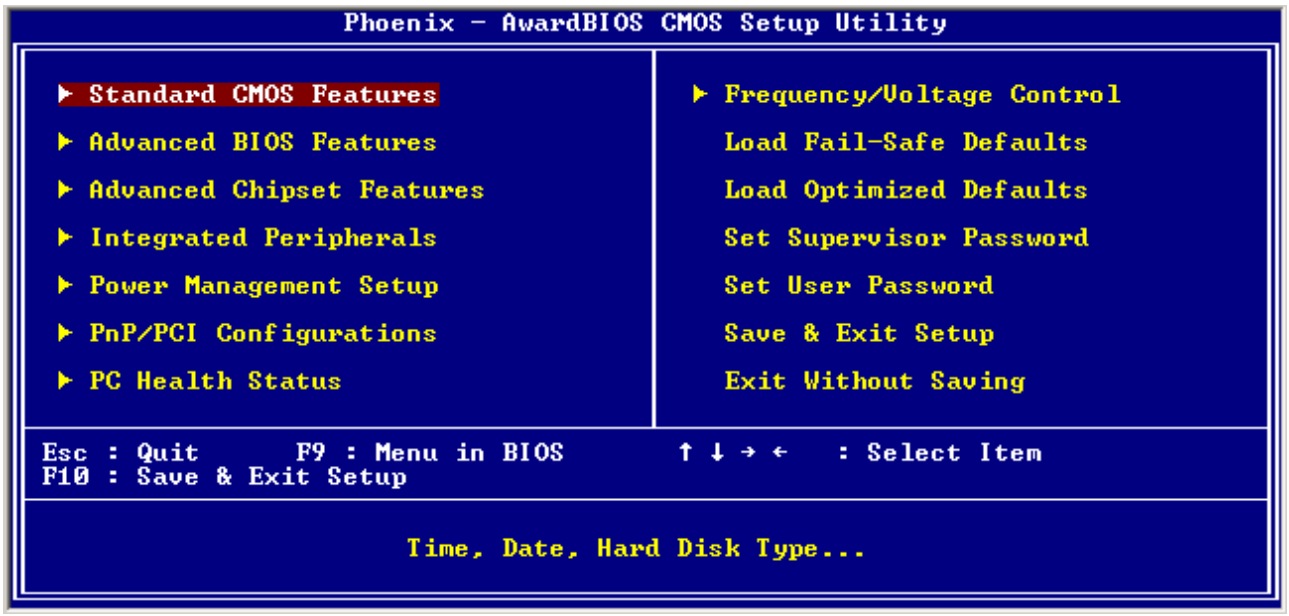
If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

3.5 Main Menu

Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

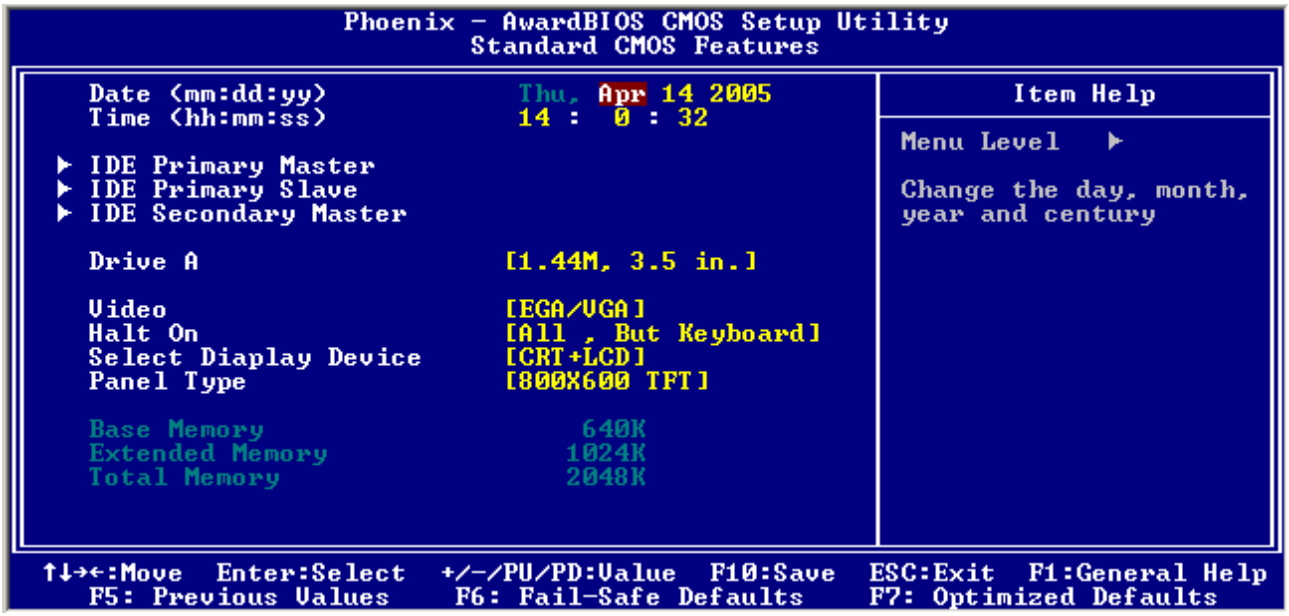
Note that a brief description of each highlighted selection appears at the bottom of the screen.



Note: The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen.
Visit the Evalue website (www.evalue-tech.com) to download the latest product and BIOS information.

3.5.1 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into few categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



3.5.1.1 Main Menu Selection

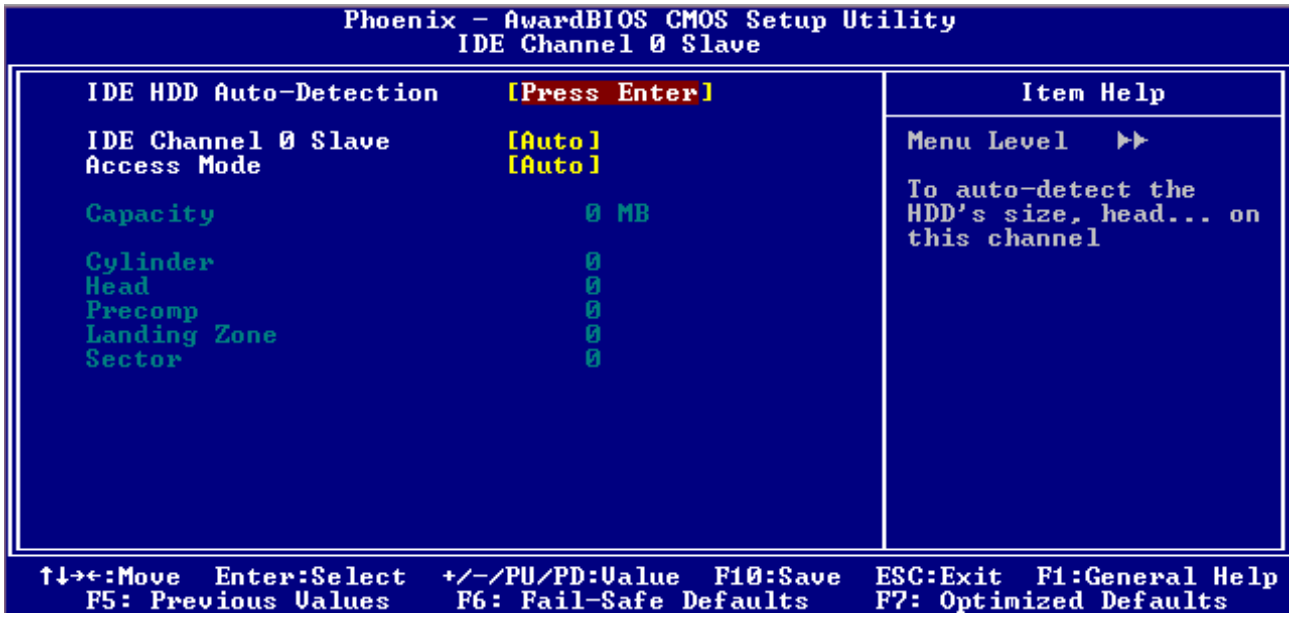
This reference table shows the selections that you may make on the Main Menu.

Item	Options	Description
Date	MM DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Primary Master IDE Primary Slave IDE Secondary Master	Options are in its sub menu	Press <Enter> to enter the sub menu of detailed options
Drive A	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you

Item	Options	Description
Select Display Device	Auto CRT LCD CRT+LCD	Select Display Device that the screen will be shown
Panel Type	640x480 TFT 800x600 TFT LVDS 1024x768 TFT 2P/C32M 1280x1024 TFT 640x480 DSTN 800x600 DSTN 1024x768 DSTN 1024x768 TFT 1P/LVDS 640x480 LVDS 800x600 TFT 1024x768 TFT 1400x1050 TFT 2P/LVDS 1280x1024 DSTN	Select Panel Resolution that will be displayed depending on the LCD Panel (LFP)

3.5.1.2 IDE Adapter Setup

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive. The below Figure will shows the IDE primary master sub menu.

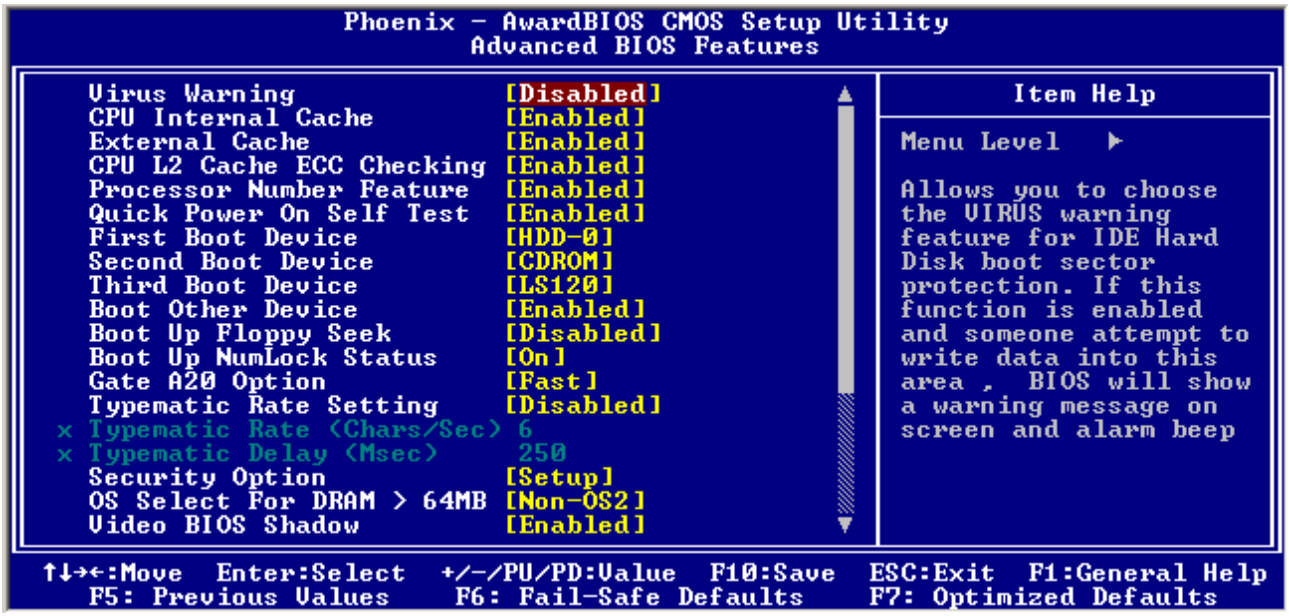


Use the following table to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Channel 0 Master IDE Channel 0 Slave, IDE Channel 1 Master, IDE Channel 1 Slave	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Access Mode	Normal LBA Large Auto	Choose the access mode for this hard disk
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.
The following options are selectable only if the 'IDE Channel …' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

3.5.2 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



3.5.2.1 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Item	Description
Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

3.5.2.2 CPU Internal Cache

This item allows you to enable the CPU internal and external cache to speed up memory access. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.3 External Cache

This item allows you to enable the CPU external cache to speed up memory access. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.4 CPU L2 Cache ECC Checking

This item allows you to enable the CPU external L2 cache use ECC checking method in memory access.

Item	Description
Enabled	Enable ECC checking
Disabled	Disable ECC checking

3.5.2.5 Processor Number Feature

This feature allows to control the use of the processor's embedded unique identification number.

Item	Description
Enabled	Enable to control processor number
Disabled	Disable to control processor number

3.5.2.6 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Item	Description
Enabled	Enable quick POST
Disabled	Normal POST

3.5.2.7 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Item	Description
Floppy	Floppy Device
LS120	LS120 Device
HDD-0	First Hard Disk Device
SCSI	SCSI Device
CDROM	CDROM Device
HDD-1	Secondary Hard Disk Device
HDD-2	Third Hard Disk Device
HDD-3	Fourth Hard Disk Device
ZIP100	ZIP-100 Device
USB-FDD	USB Floppy Device
USB-ZIP	USB ZIP Device
USB-CDROM	USB CDROM Device
USB-HDD	USB Hard Disk Device
LAN	Network Device
Disabled	Disabled any boot device

3.5.2.8 Book Up Floppy Seek

Seeks disk drives during boot up. Disabling seeds boot up.

Item	Description
Enabled	Enable Floppy Seek
Disabled	Disable Floppy Seek

3.5.2.9 Boot Up NumLock Status

Select power on state for NumLock.

Item	Description
Enabled	Enable NumLock
Disabled	Disable NumLock

3.5.2.10 Gate A20 Option

Select if chipset or keyboard controller should control Gate A20.

Item	Description
Normal	A pin in the keyboard controller controls Gate A20
Fast	Lets chipset control Gate A20

3.5.2.11 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

Item	Description
Enabled	Enable typematic rate/delay setting
Disabled	Disable typematic rate/delay setting

3.5.2.12 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

3.5.2.13 Typematic Rate (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

3.5.2.14 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

Item	Description
System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

3.5.2.15 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

Item	Description
Non-OS2	Disable OS for over 64 MB DRAM
OS2	Enable OS for over 64 MB DRAM

3.5.2.16 Video BIOS Shadow

To allow copying Video BIOS into shadow RAM to improve video performance.

Item	Description
Enable	Copy Video BIOS into shadow RAM
Disable	Do not copy Video BIOS into shadow RAM

3.5.2.17 C8000-CBFFF/CC000-CFFFF/D0000-D3FFF/D4000-D7FFF/D8000-DBFFF/DC000-DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of on-board SCSI.

Item	Description
Enable	Optional shadow is enabled
Disable	Optional shadow is disabled

3.5.2.18 Full Screen LOGO Show

If the BIOS had the full screen logo in it, this item could allow enable/ disable the full screen logo show on display.

Item	Description
Enable	Enable full screen logo show
Disable	Disable full screen logo show

3.5.2.19 Small Logo (EPA) Show

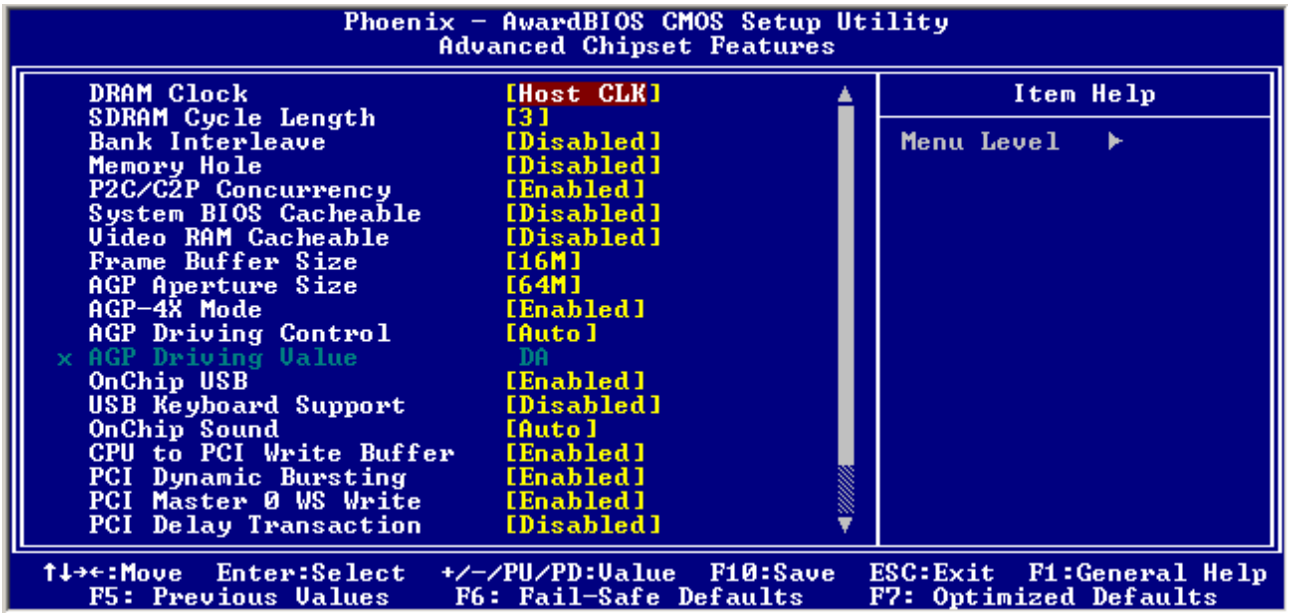
This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

Item	Description
Enabled	EPA Logo show is enabled
Disabled	EPA Logo show is disabled

3.5.3 Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.



3.5.3.1 DRAM Clock

Set the memory bus frequency to operate at various values for the proper memory clock setting.

The choices: Host CLK, HCLK-33M, HCLK+33M.

3.5.3.2 SDRAM Cycle Length

When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer.

The choices: 3, 2.

3.5.3.3 Bank Interleave

Enables to set the interleave mode of the SDRM interface which allows banks of SDRAM to alternate their refresh and access cycles.

The choices: Disabled, 2 Bank, 4 Bank.

3.5.3.4 Memory Hole

When this item is enabled, ISA ROM will be mapped to 15-16M area and also support legacy ISA devices. While this item is disabled and legacy ISA devices are not utilized, the graphic performance will be enhanced.

The choices: Disabled, 512K-640K, 15M-16M, 14M-16M.

3.5.3.5 P2C/C2P Concurrency

CPU bus will be occupied during the entire PCI operation period when disabled.

The choices: Enabled, Disabled.

3.5.3.6 System BIOS Cacheable

This feature is only valid when the system BIOS is shadowed. It enables or disables the caching of the system BIOS ROM at **F0000h-FFFFFh** via the L2 cache. This greatly speeds up accesses to the system BIOS. However, this does **not** translate into better system performance because the OS does not need to access the system BIOS much.

The choice: Enabled, Disabled.

3.5.3.7 Video RAM Cacheable

This feature is only valid when the video BIOS is shadowed. It enables or disables the caching of the video BIOS ROM at **C0000h-C7FFFh** via the L2 cache. This greatly speeds up accesses to the video BIOS. However, this does **not** translate into better system performance because the OS bypasses the BIOS using the graphics driver to access the video card's hardware directly.

The choice: Enabled, Disabled.

3.5.3.8 Frame Buffer Size

Select the size of onboard video controller's frame buffer. The buffer size are share from system memory unit.

The choices: 2MB, 4MB, 8MB, 16MB, 32MB.

3.5.3.9 AGP Aperture Size

Select the size of Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation.

The choices: 4MB,8MB,16MB.32MB, 64MB,128MB.

3.5.3.10 AGP-4X Mode

This item allows you to enable / disable the AGP-4X Mode.

The choices: Enabled, Disabled.

3.5.3.11 AGP Driving Control

This item allows you to select the AGP Driving Control to auto / disable Mode.

The choices: Auto, Manual.

3.5.3.12 AGP Driving Value

This item allows you to set the AGP Driving value.

3.5.3.13 On-Chip USB

This item allows you to set the USB Controller.

The choices: Enabled, Disabled.

3.5.3.14 USB Keyboard Support

This item allows you to set the system's USB keyboard to Enabled/Disabled..

The choices: Enabled, Disabled.

3.5.3.15 On-Chip Sound

Select Enabled to use the audio capabilities of your system. Most of the following fields do not appear when this field is Disabled.

The choices: Auto, Disabled.

3.5.3.16 CPU to PCI Write Buffer

This item controls the PCI write buffer to the PCI bus and prevents the CPU from doing anything else until it has completed sending the data to the PCI bus. The data in the write buffer will be written to the PCI bus when the next PCI bus read cycle starts without stalling the CPU for the entire CPU to PCI transaction.

The choices: Enabled, Disabled.

3.5.3.17 PCI Dynamic Bursting

This item controls the PCI write buffer. Set enabled to write transaction on the PCI bus straightly to the write buffer and burst transactions being sent on their way as soon as there are enough to send in a single burst. Set disabled to make the data go to the write buffer and burst-transferred later and the write buffer is flushed and the data is written to the PCI bus immediately if the write transaction is not a bust transaction.

The choices: Enabled, Disabled.

3.5.3.18 PCI Master 0 WS Write

This item determines whether there's a delay before any writes to the PCI bus.

The choices: Enabled, Disabled.

3.5.3.19 PCI Delayed Transaction

This feature is used to meet the latency of PCI cycles to and from the ISA bus. The ISA bus is much, much slower than the PCI bus. Thus, PCI cycles to and from the ISA bus take a longer time to complete and this slows the PCI bus down.

However, enabling **Delayed Transaction** enables the chipset's embedded 32-bit posted write buffer to support delayed transaction cycles. This means that transactions to and from the ISA bus are buffered and the PCI bus can be freed to perform other transactions while the ISA transaction is underway.

This option should be **enabled** for better performance and to meet PCI 2.1 specifications. Disable it only if your PCI cards cannot work properly or if you are using an ISA card that is not PCI 2.1 compliant.

The choices: Enabled, Disabled.

3.5.3.20 PCI#2 Access #1 Retry

This item is linked to the CPU to PCI write Buffer. All writes to the PCI bus are immediately written into the buffer, instead of the PCI bus. This frees up the CPU from waiting till the PCI bus is free. The data are then written to the PCI bus when the next PCI bus cycle starts.

The choices: Enabled, Disabled.

3.5.3.21 AGP Master 1 WS Write

Enables this item to increase AGP writing.

The Choices: Enabled, Disabled.

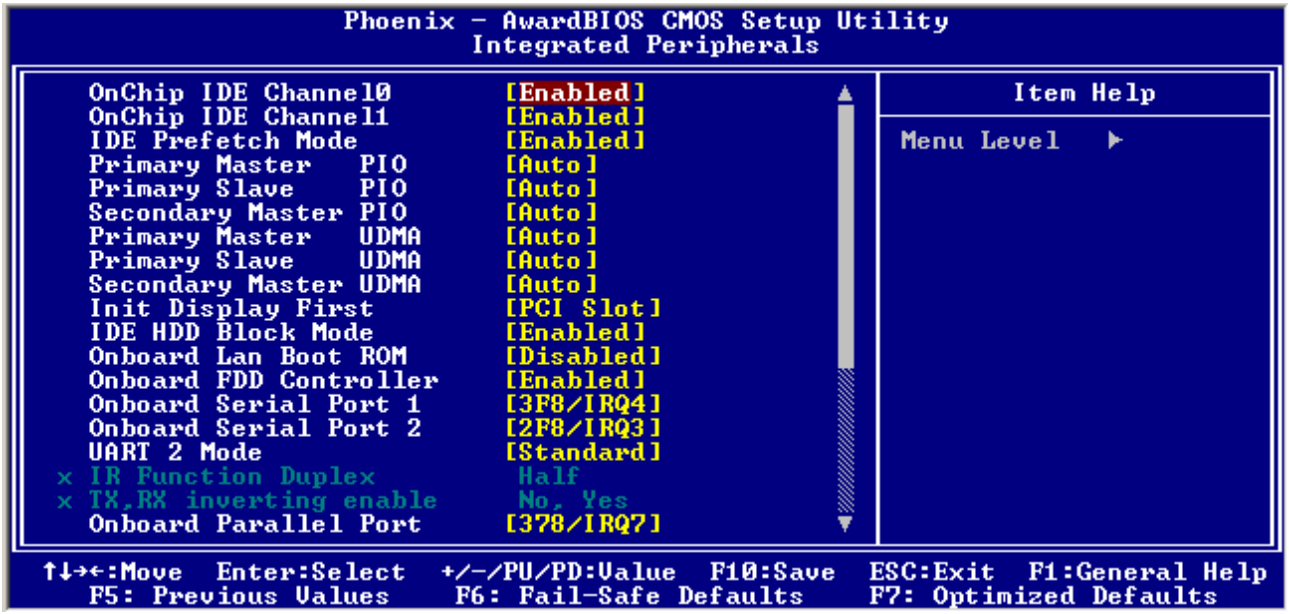
3.5.3.22 AGP Master 1 WS Read

Enables this item to increase AGP reading.

The choices: Enabled, Disabled.

3.5.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.



3.5.4.1 OnChip IDE Channel10/11

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface. Select Disabled to deactivate this interface.

The choices: Enabled, Disabled.

3.5.4.2 IDE Prefetch Mode

For faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to Disabled if the interface does not support prefetching.

The choices: Enabled, Disabled.

3.5.4.3 Primary/Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

The choices: Auto, Mode 0, Mode 1, Mode 2, Mode 3, or Mode 4.

3.5.4.4 Primary/Secondary Master/Slave UDMA

Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.

The choices: Auto, Disabled.

3.5.4.5 Init Display First

This item allows you to decide to active whether PCI Slot or AGP first.

The choices: PCI Slot, AGP.

3.5.4.6 IDE HDD Block Mode

Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

The choices: Enabled, Disabled.

3.5.4.7 Onboard Lan Boot ROM

This item allows to boot over the network when system POST and shorten the booting time by set disabled.

The choices: Enabled, Disabled.

3.5.4.8 Onboard FDD Controller

This item allows to enable/disable the onboard floppy drive controller. If an add-on FDD controller or any floppy drive at all, set to disabled to save an IRQ.

The choices: Enabled, Disabled.

3.5.4.9 Onboard Serial Port 1 / 2

Select an address and corresponding interrupt for the first and second serial ports.

The choices: Disabled, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3.

3.5.4.10 UART 2 Mode

Select UART 2 mode as standard serial port or IR port.

The choices: Standard, HPSIR, ASKIR.

3.5.4.11 IR Function Duplex

Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time.

The choices: Full, Half.

3.5.4.12 TX,RX inverting enable

This item allows you to determine the active of RxD, TxD level.

The choices: No,No, No,Yes, Yes,No, Yes,Yes.

3.5.4.13 Onboard Parallel Port

Select a logical LPT port name and matching address for the physical parallel (printer) port.

The choicse: Floppy, 378H/IRQ7, 278H/IRQ5, 3BCH/IRQ7, Disabled

3.5.4.14 Onboard Parallel Mode

Select an operating mode for the parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode.

The choices: EPP, ECP, ECP/EPP, Normal.

3.5.4.15 ECP Mode Use DMA

Select a DMA channel for the port.

The choices: 3, 1.

3.5.4.16 Parallel Port EPP Type

Select EPP port type 1.7 or 1.9.

The choicse: EPP1.7, EPP1.9.

3.5.4.17 Onboard Serial Port 3 / 4

Select an IO address for the third and forth ports.

The choices: 3F8, 2F8, 3E8, 2E8, Disabled.

3.5.4.18 Serial Port 3 / 4 Use IRQ

Select an IRQ for the third and forth serial ports.

The choices: IRQ5, IRQ10.

3.5.4.19 Onboard Legacy Audio

This item allows you to enable or disable the onboard legacy audio function.

The choices: Enabled, Disabled.

3.5.4.20 Sound Blaster

This item allows you to enable or disable the onboard audio function is compatible with sound blaster mode.

The choices: Enabled, Disabled.

3.5.4.21 SB I/O Base Address

This chipset traps I/O accesses for Sound Blaster compatibility.

The choices: 220H, 240H, 260H, 280H.

3.5.4.22 SB IRQ Select

Select an interrupt for the audio port.

The choices: IRQ5, IRQ7, IRQ9, IRQ10.

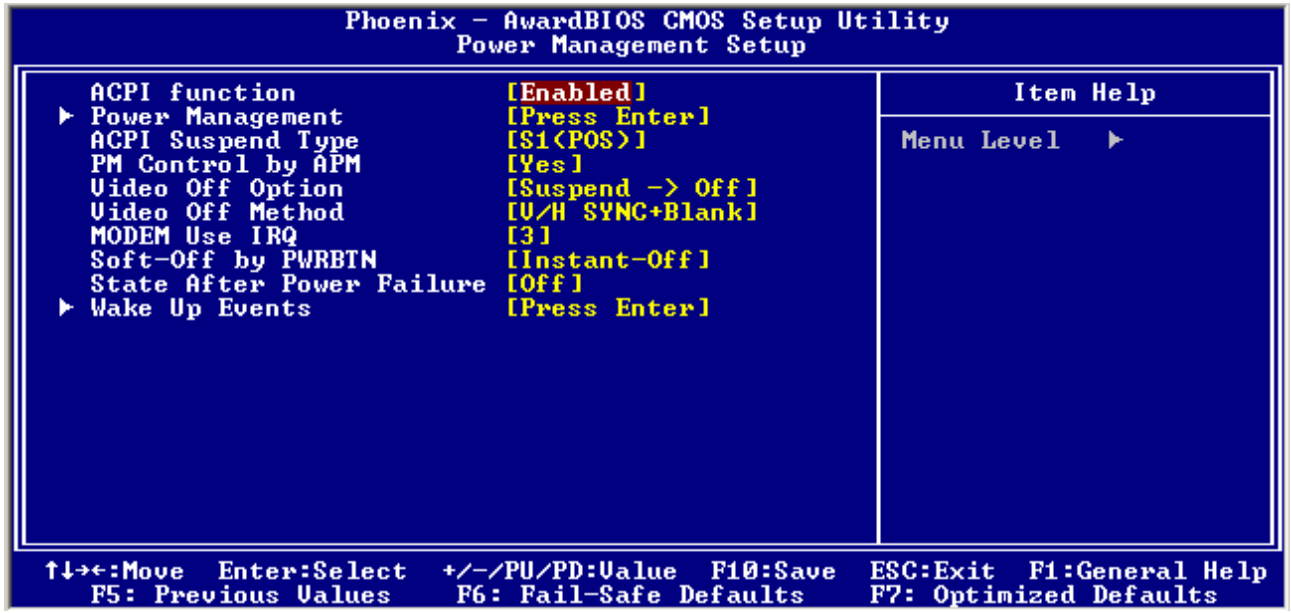
3.5.4.23 SB DMA Select

This chipset supports I/O trapping for DMA accesses and allows you to select the Audio DMA type.

The choices: DMA 0, DMA 1, DMA 2, DMA 3.

3.5.5 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.

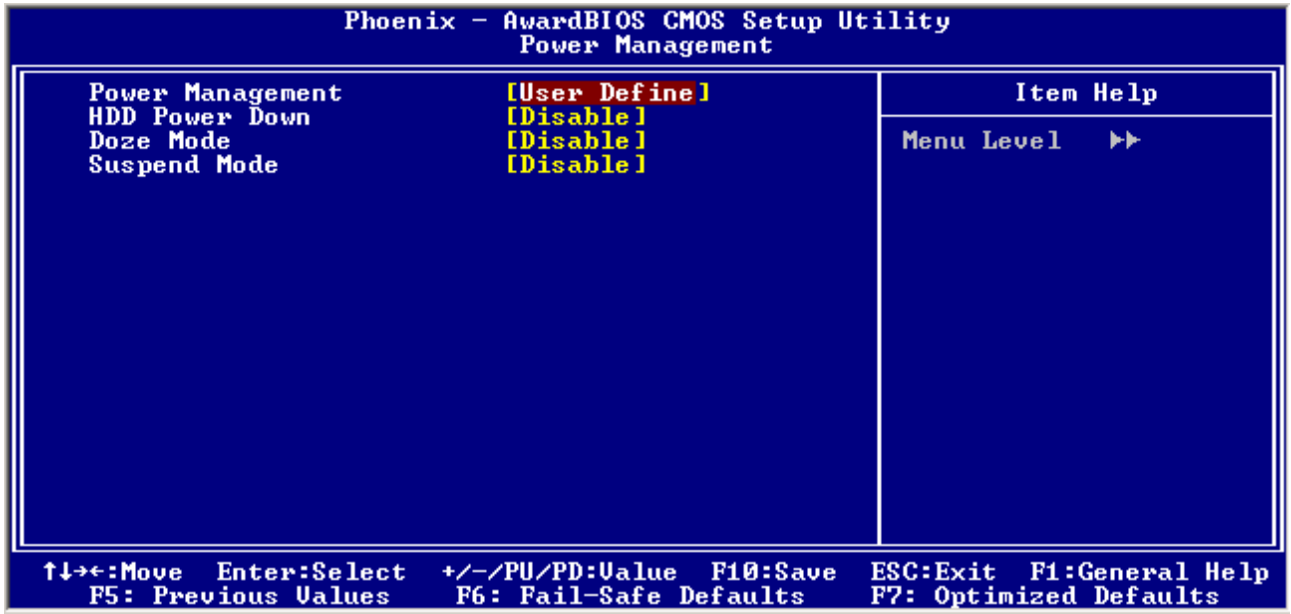


3.5.5.1 ACPI Function

This item allows you to enable/disable the ACPI function.

The choices: Enable, Disable.

3.5.5.2 Power Management



3.5.5.2.1 Power Management

There are three selections for Power Management, and each of them has fixed mode settings.

Item	Description
Min. Power Saving	Minimum power management, HDD Power Down = 15 Min,
Max. Power Saving	Maximum power management, HDD Power Down =1 Min,
User Defined	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

3.5.5.2.2 HDD Power Down

There are three selections for Power Management Option; both of them have fixed mode settings.

The choices: Disabled, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 Min.

3.5.5.2.3 Doze Mode

This field slows down the CPU to a minimal activity level while other parts of the system keep running as normal.

The choices: Disabled, 5, 10, 20, 30, 40 Sec, 1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour.

3.5.5.2.4 Suspend Mode

This setting defines the number of minutes before the system enters "suspend mode", the deepest level of system inactivity shutdown. The exact definition depends on the system, but in general this mode means that all system devices are shutdown (except for any that the BIOS is specifically told to keep running) and the processor is shut down to a trickle mode.

sTT3Mr.1, 2,

3.5.5.7 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choices: NA, 3, 4, 5, 7, 9, 10, 11.

3.5.5.8 Soft-Off by PWR-BTTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".(Only could working on ATX Power supply)

The choices: Delay 4 Sec, Instant-Off.

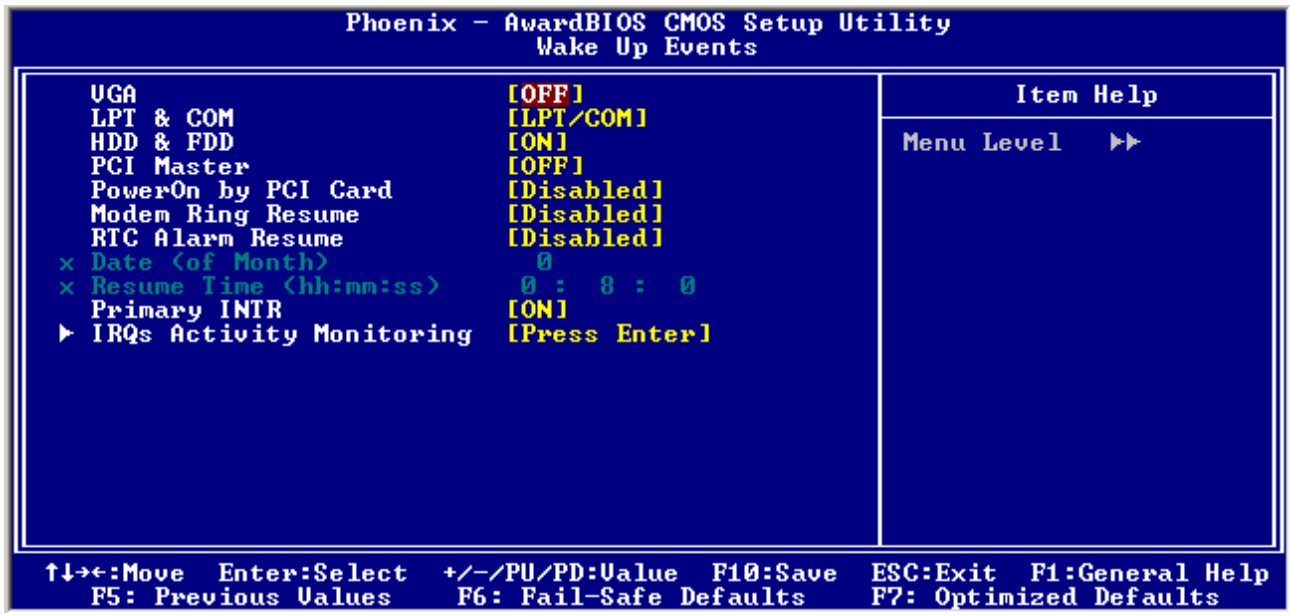
3.5.5.9 State After Power Failure

This item controls the system allowing enough time to save its state in memory. After primary power is restored, the system can reestablish its state during power failure recovery and continue operation.

The choices: Auto, On, Off.

3.5.5.10 Wake Up Events

PM Wake up events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from such a mode. In effect, the system remains alert for anything which occurs to a device which is configured as *On*, even when the system is in a power down mode.



3.5.5.10.1VGA

System can be awaked by VGA monitor.

The choices: On, Off.

3.5.5.10.2LPT & COM

System can be awaked by LPT port, COM port or both.

The choices: NONE, LPT, COM, LPT/COM.

3.5.5.10.3HDD & FDD

System can be awaked by Hard Drive and Floppy Drive.

The choices: On, Off.

3.5.5.10.4PCI Master

System can be awaked by system peripheral devices.

The choices: On, Off.

3.5.5.10.5PowerOn by PCI Card

System can be awaked by PCI devices

The choices: Enabled, Disabled.

3.5.5.10.6Modem Ring Resume

System can be awaked by Modem Ring

The choices: Enabled, Disabled.

3.5.5.10.7RTC Alarm Resume

This function is for setting date and time for your computer to boot up.

The choices: Enabled, Disabled.

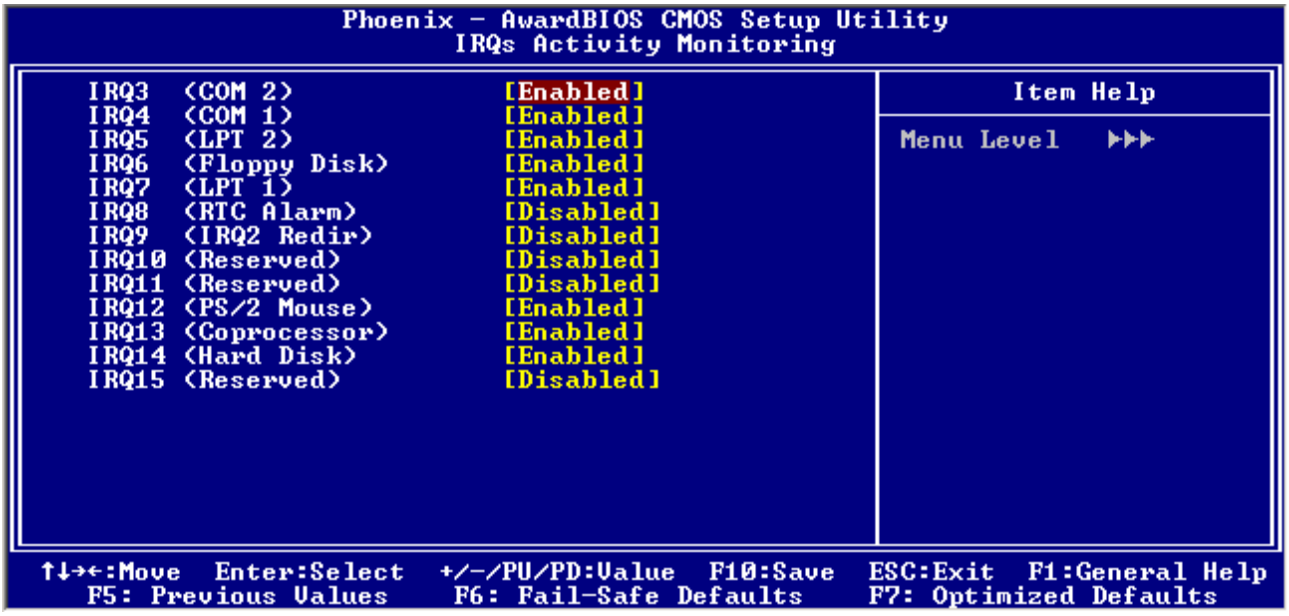
3.5.5.10.8Primary INTR

This item sets the system to wake up from suspend mode if activity is detected from any enabled IRQ channels. Setting this option to off will neither prevent the system from entering power saving mode or cause the system to fully power up.

The choices: On, Off.

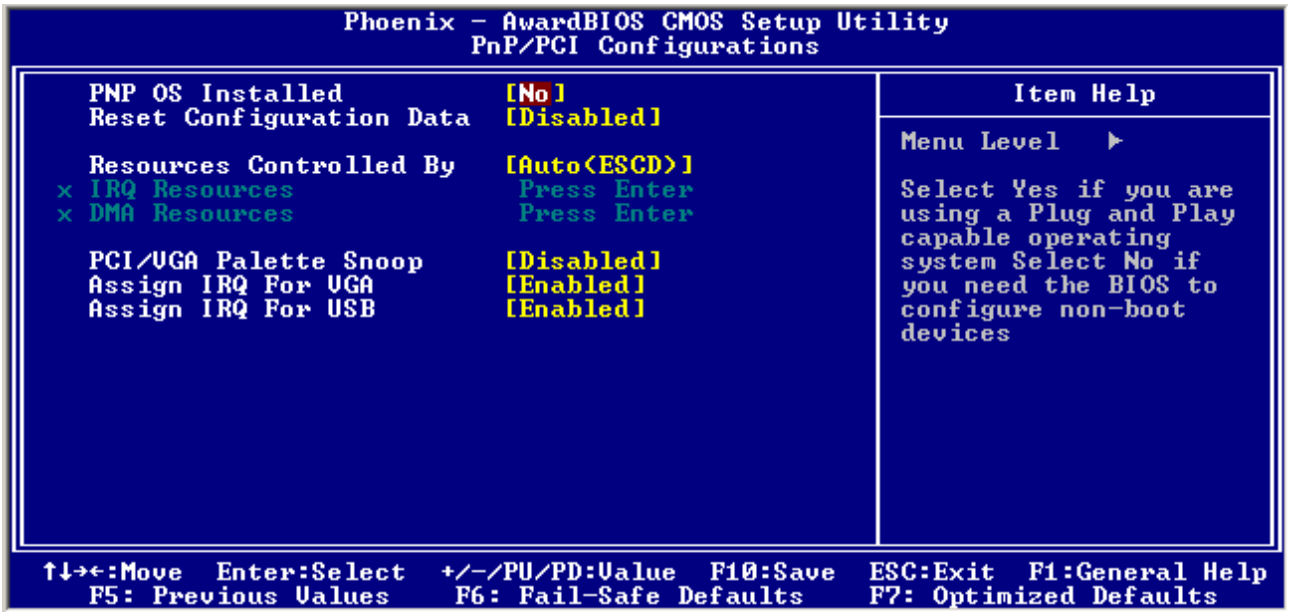
3.5.5.10.9IRQs Activity Monitoring

System can be awaked by IRQs in the list.



3.5.6 PnP / PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



3.5.6.1 PNP OS Installed

The operation system environment is Plug-and-Play aware sets "YES".

The choices: Yes, No.

3.5.6.2 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choices: Enabled, Disabled.

3.5.6.3 Resources Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to "manual" choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a "➢").

The choices: Auto(ESCD), Manual.

3.5.6.4 PCI / VGA Palette Snoop

Leave this field at Disabled.

The choices: Enabled, Disabled.

3.5.6.5 Assign IRQ For VGA

While the system has one VGA controller and more than one VGA devices are connected, then “Enabled” is set. If the system VGA controller is not used, then “Disabled” is set.

The choices: Enabled, Disabled.

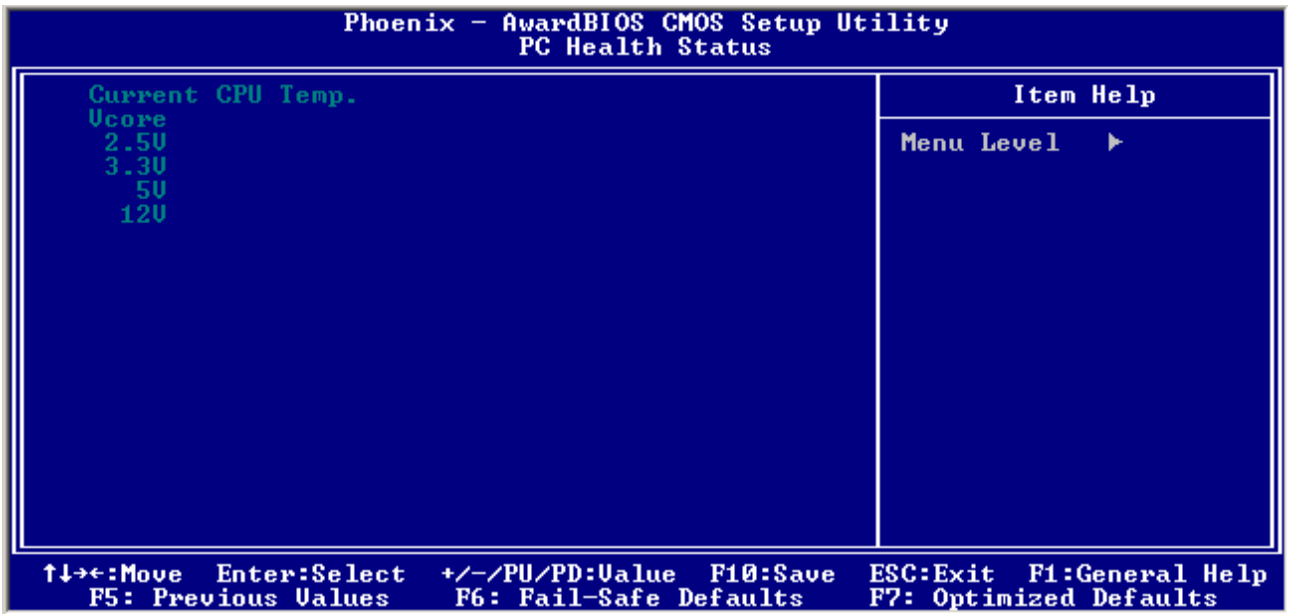
3.5.6.6 Assign IRQ For USB

While the system has one USB controller and more than one USB devices are connected, then “Enabled” is set. If the system USB controller is not used, then “Disabled” is set.

The choices: Enabled, Disabled.

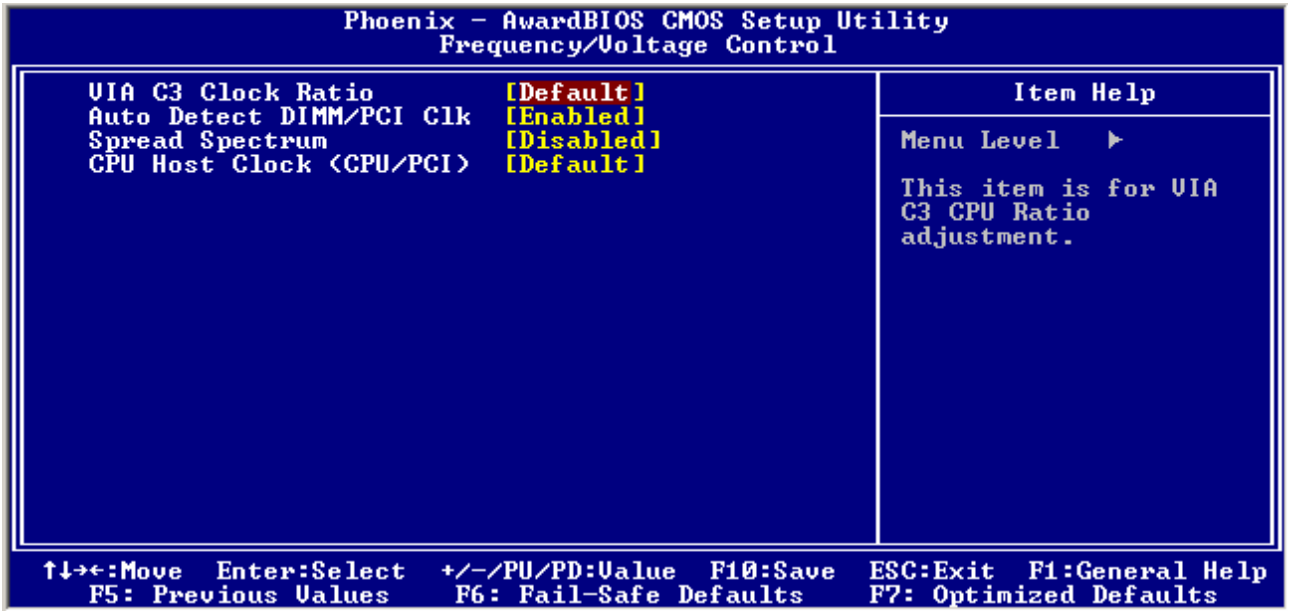
3.5.7 PC Health Status

This section shows the status of your CPU, Fan & System.



3.5.8 Frequency / Voltage Control

This menu specifies your setting for frequency/voltage control.



3.5.8.1 VIA C3 Clock Ratio

This item allows you to select the VIA C3 CPU clock ratio.

The choices: Default, X3, X3.5, X4, X4.5, X5, X5.5, X6, X6.5, X7, X7.5, X8, X8.5, X9, X9.5, X10, X10.5, X11, X12.

3.5.8.2 Auto Detect DIMM/PCI Clk

This item allows you to enable/disable auto detect PCI Clock.

The choice: Enable, Disable.

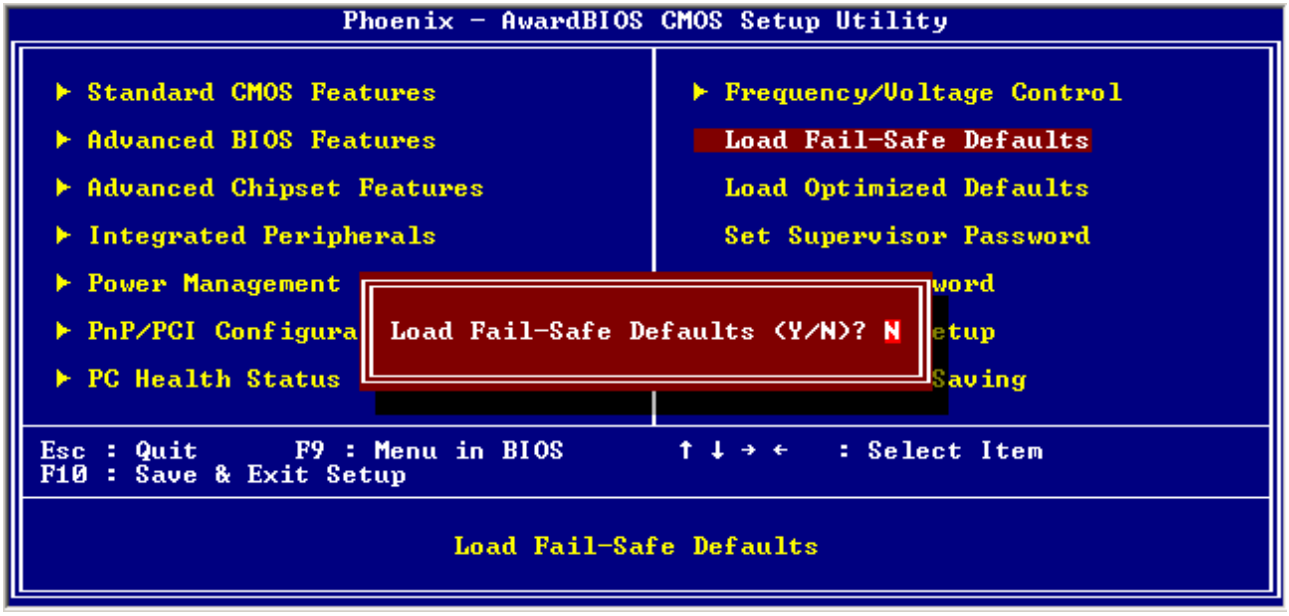
3.5.8.3 Spread Spectrum / CPU Host Clock

These options allow you to set Spread Spectrum and CPU Host/3V66/PCI clock into various types of frequencies.

3.5.9 Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

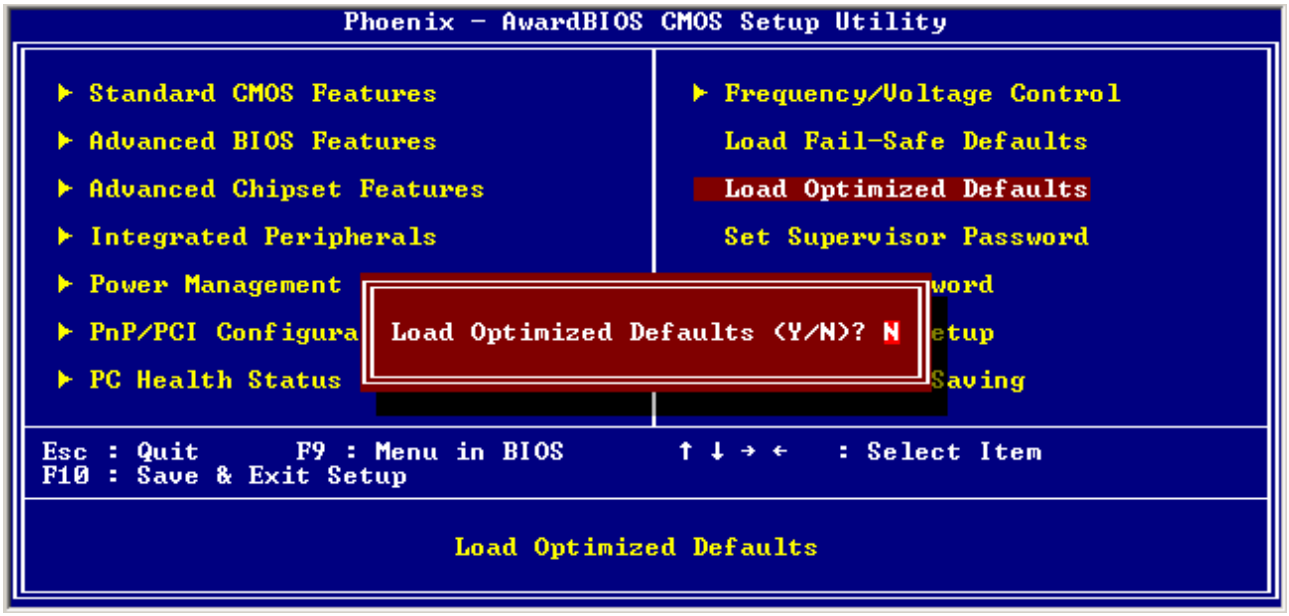
Press <Y> to load the BIOS default values for the most stable, minimal-performance system operations.



3.5.10 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

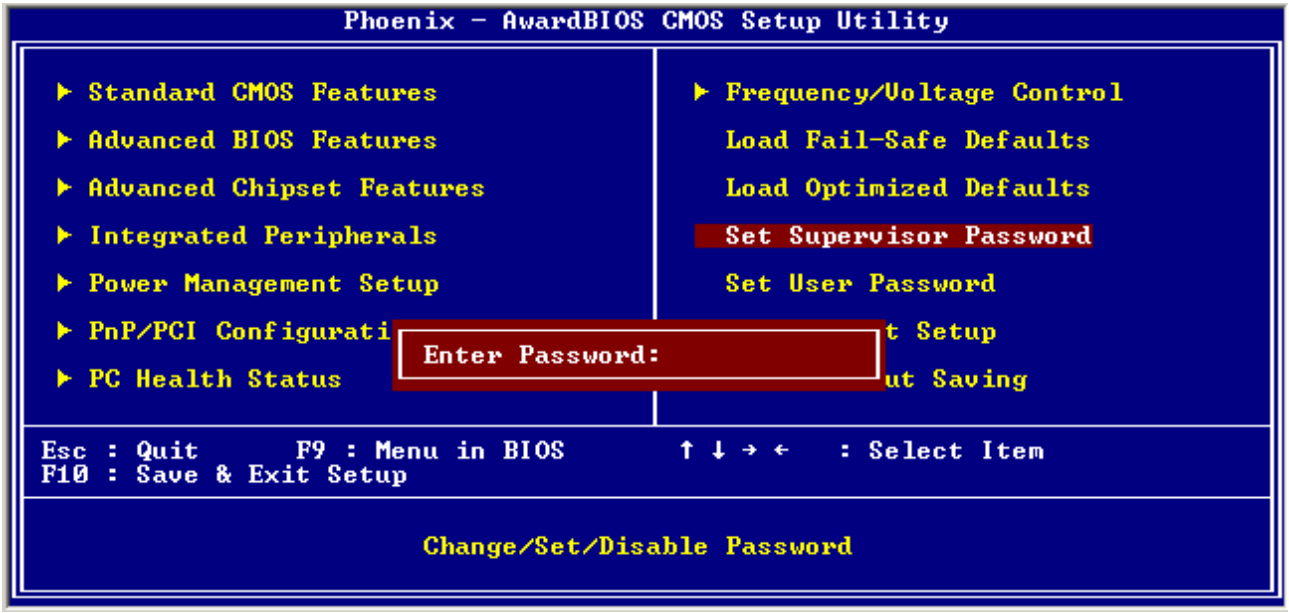
Press <Y> to load the default values setting for optimal performance system operations.



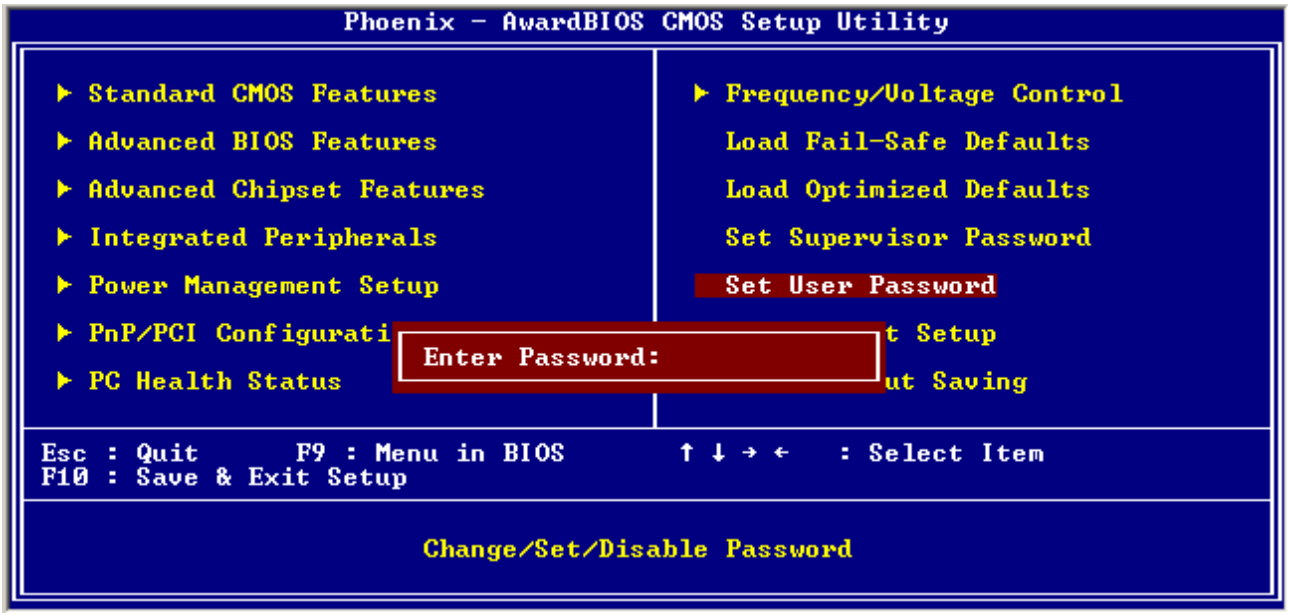
3.5.11 Set Supervisor / User Password

You can set either supervisor or user password, or both of them.

Supervisor Password: able to enter/change the options of setup menus.



User Password: able to enter but no right to change the options of setup menus.



Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

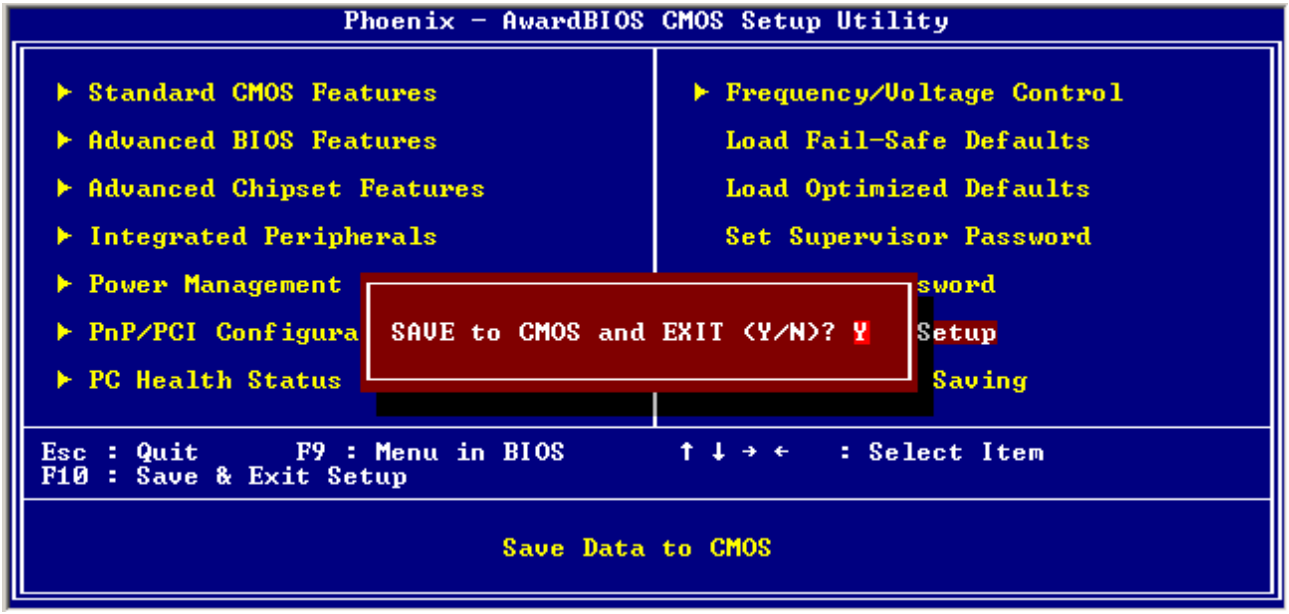
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup

3.5.12 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

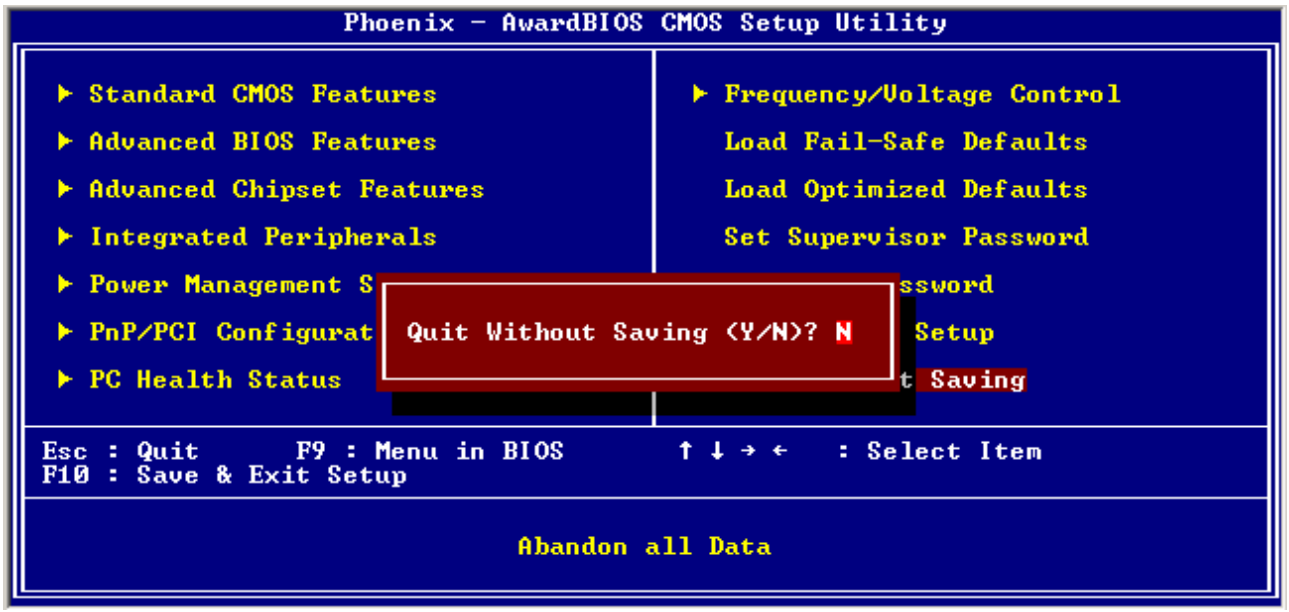
Enter <Y> to store the selection made in the menus in CMOS, a special section in memory that stays on after turning the system off. The BIOS configures the system according to the Setup selection stored in CMOS when boot the computer next time.

The system is restarted after saving the values.



3.5.13 Exit Without Save

Abandon all CMOS value changes and exit setup, and the system is restarted after exiting.



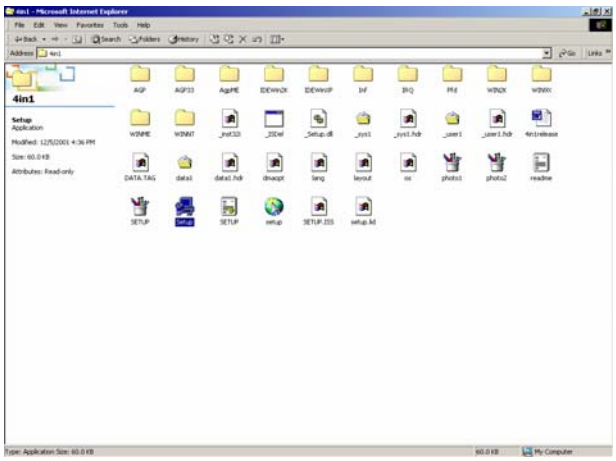
4. Drivers Installation

Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

4.1 Install Chipset Driver (For VIA VT82C686B)

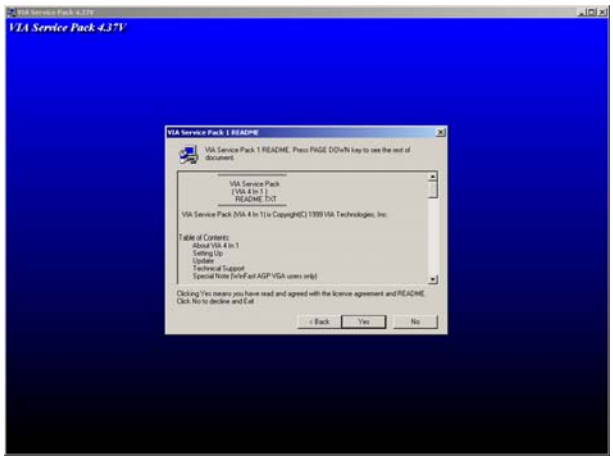
Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Chipset\VIA\ VT82C686B \4in1**.

Note: The installation procedures and screen shots in this section are based on Windows 2000 operation system.

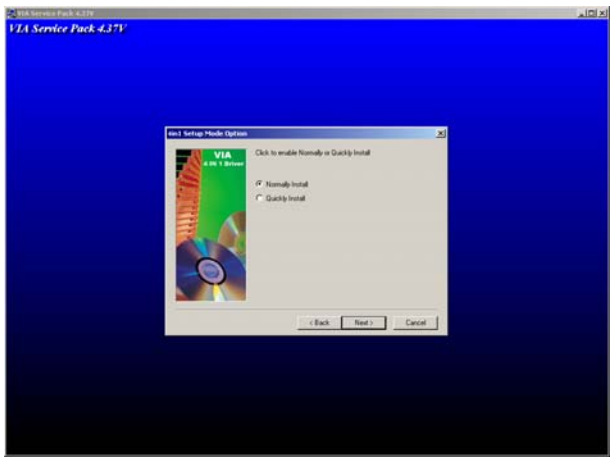


Step1. Locate 「\Driver_Chipset\VIA\ VT82C686B\ 4in1\Setup.exe」.

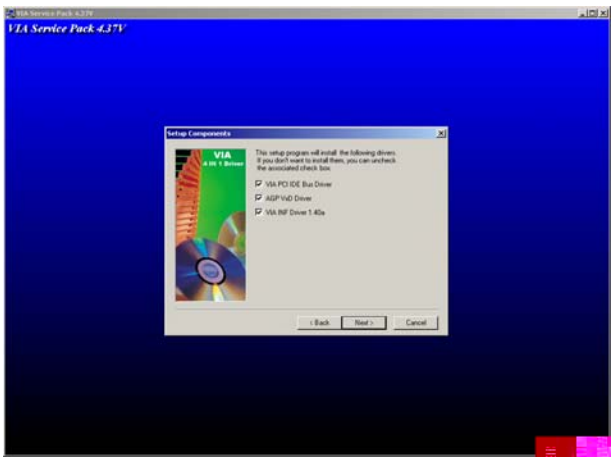
Step 2. Click **Next**.



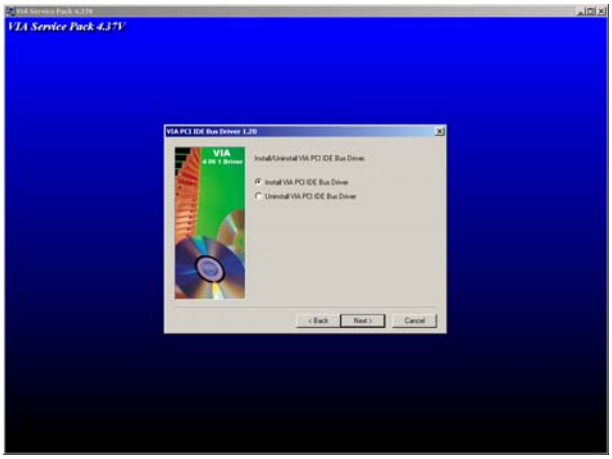
Step 3. Click **Yes**.



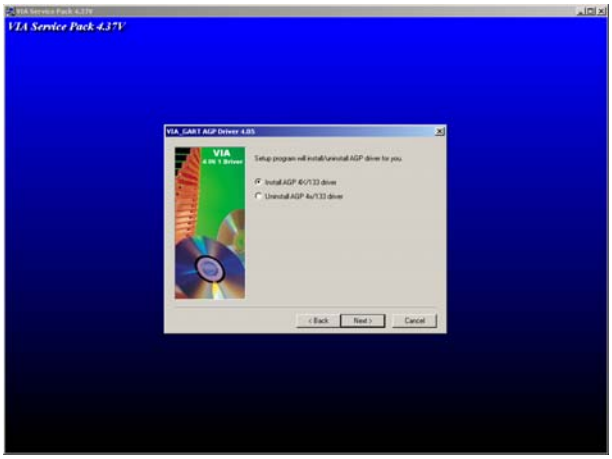
Step 4. Click **Next**.



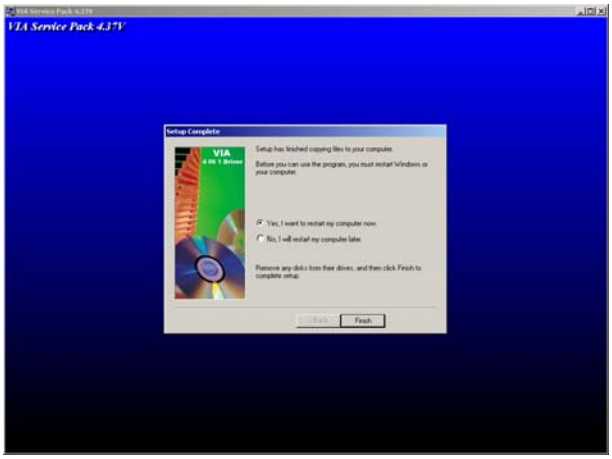
Step 5. Click **Next**.



Step 6. Click **Next**.



Step7. Click **Next**.

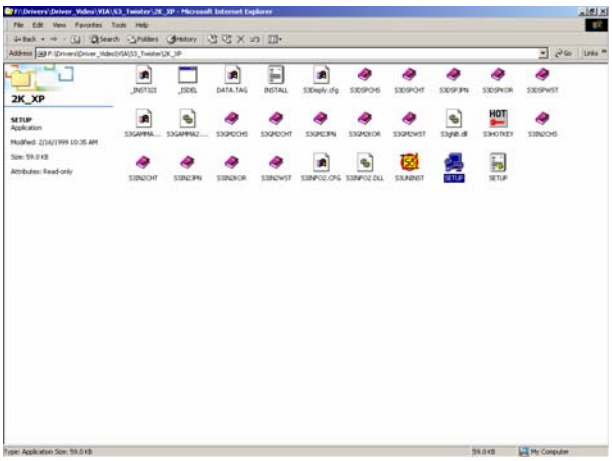


Step 8. Click **Finish** to complete setup and restart the computer.

4.2 Install Display Driver (For VIA TwisterT VT8606)

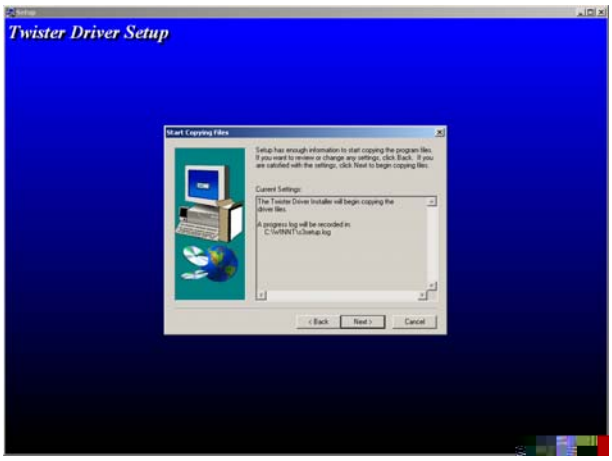
Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Video\VIA\S3_Twister\2K_XP**.

Note: The installation procedures and screen shots in this section are based on Windows 2000 operation system.



Step 1. Locate 「Driver_Video\VIA\S3_Twister\2K_XP\setup.exe」.

Step 2. Click **Next**.



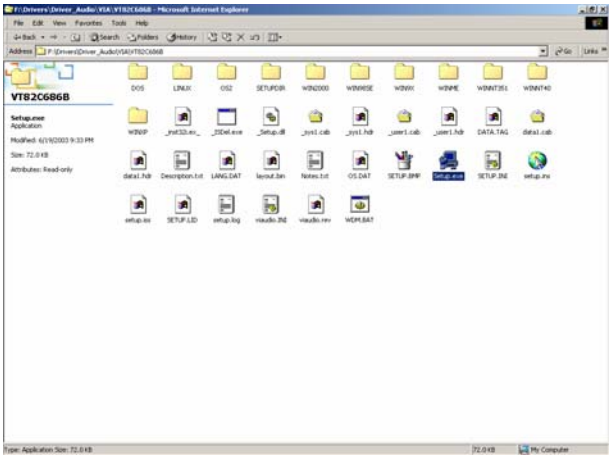
Step 3. Click **Next**.

Step 4. Click **Finish** to complete setup and restart the computer.

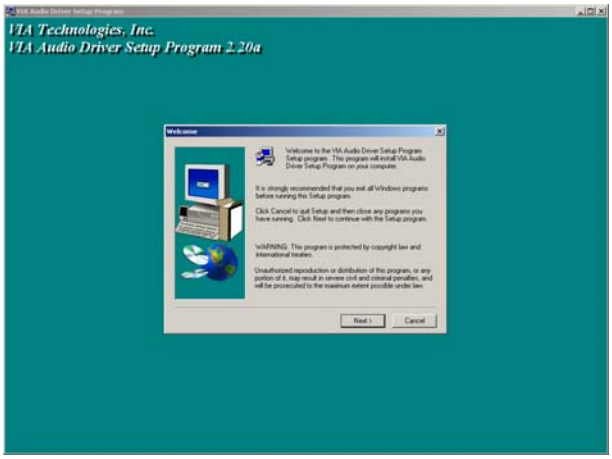
4.3 Install Audio Driver (For VIA VT1612A)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Audio\VIA\VT823X\ VT1612A\A1mu550a.**

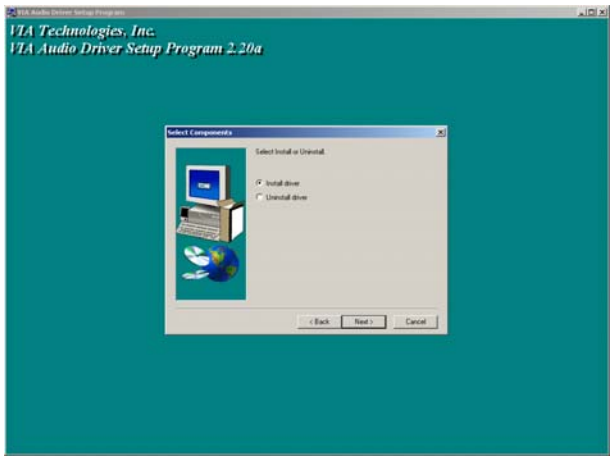
Note: The installation procedures and screen shots in this section are based on Windows 2000 operation system.



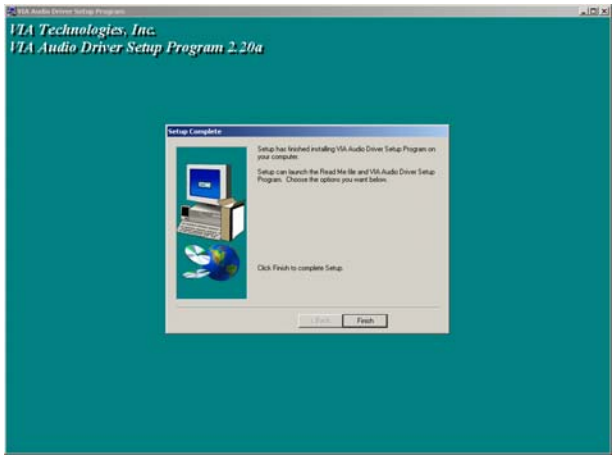
Step 1. Locate 「\ Driver_Audio\VIA\ VT823X\ VT1612A\A1mu550a\setup.exe 」.



Step 2. Click **Next**.



Step 3. Select **Install driver** and click **Next**.

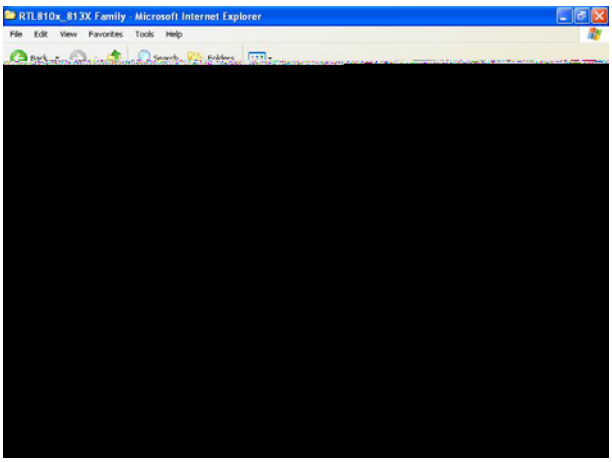


Step 4. Click **Finish** to complete the setup.

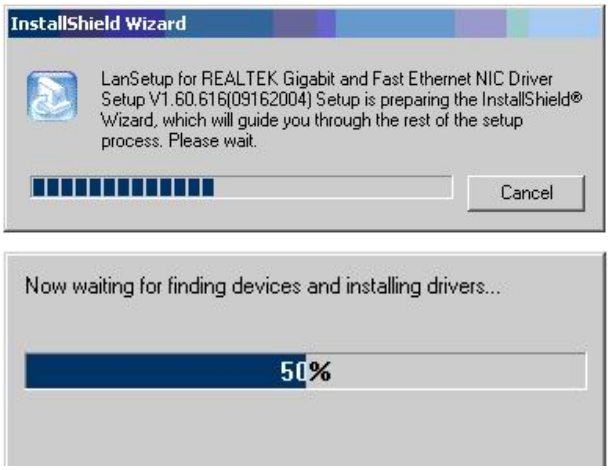
4.4 Install Ethernet Driver (For Realtek RTL810x, RTL813x Family)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Network\Realtek\ RTL810x_813X Family**.

Note: The installation procedures and screen shots in this section are based on Windows XP operation system.

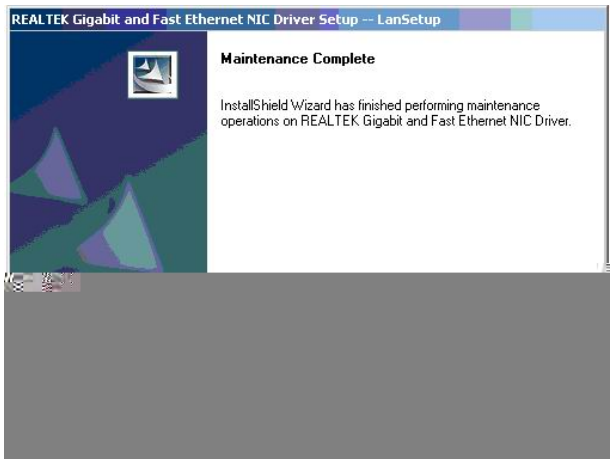


Step 1. Locate 「\Driver_Network\Realtek\ RTL810x_813X Family\Setup.exe」.



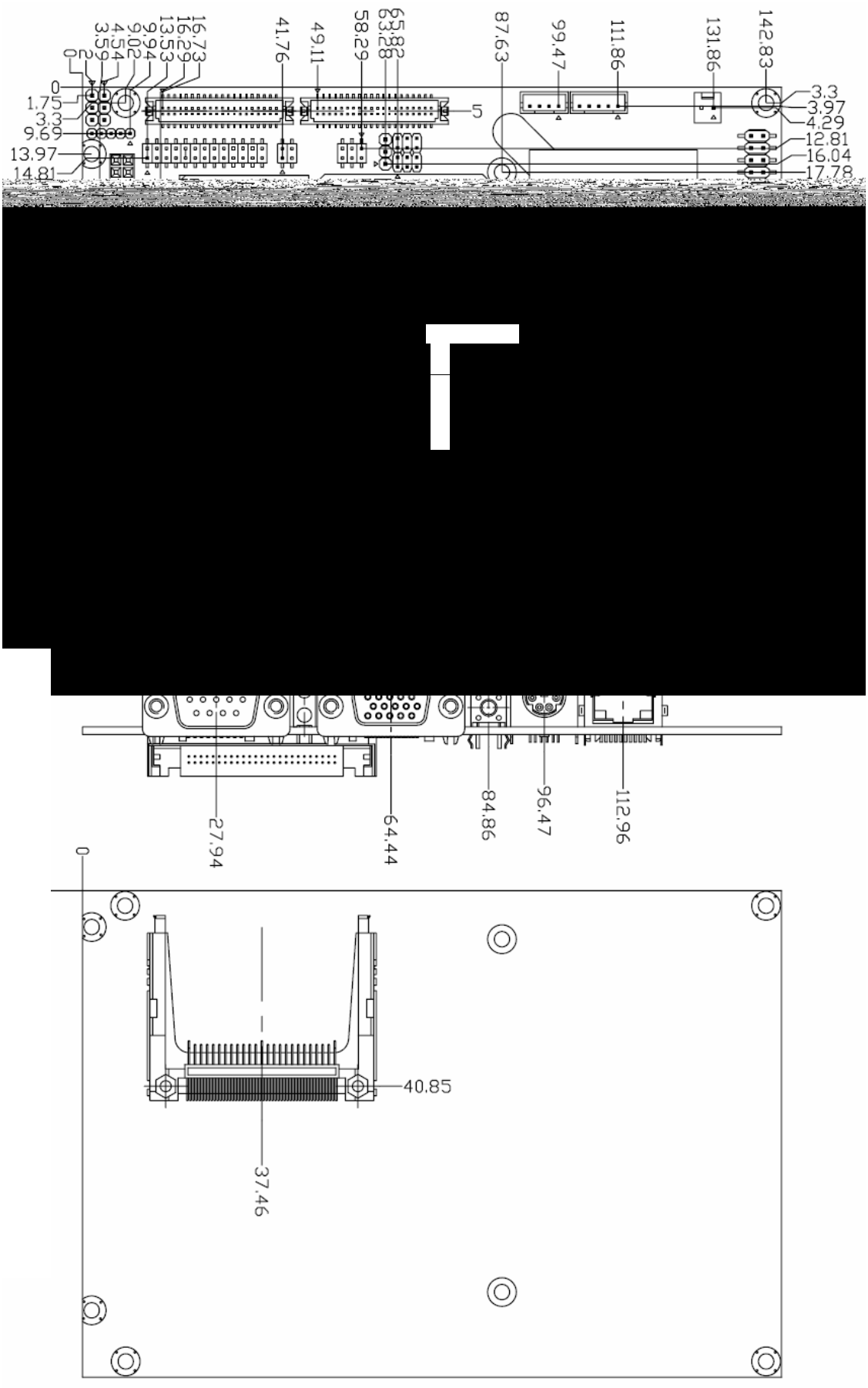
Step 2. Setup executing.

Step 3. Click **Yes** to continue the installation.



Step 4. Click **Finish** to complete the setup.

5. Measurement Drawing


0
2
3.59
4.54
9.02
9.94
13.53
16.29
16.73
41.76
49.11
58.29
63.28
65.82
87.63
99.47
111.86
131.86
142.83
0
1.75
3.3
9.69
13.97
14.81
5
3.3
3.97
4.29
12.81
16.04
17.78
27.94
64.44
84.86
96.47
112.96
0
40.85
37.46

(Unit: mm)

Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: AWARD BIOS POST Messages

Overview

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.
If a message is displayed, it will be accompanied by:
PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

Post Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

1. CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

2. CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

3. DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

4. DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

5. DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

6. DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

7. EISA Configuration Checksum Error
PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

8. EISA Configuration Is Not Complete
PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

9. ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

10. ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

11. FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

12. Invalid EISA Configuration
PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

13. KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

14. Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

15. Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

16. MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

17. Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

18. OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

19. OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

20. PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

21. PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

22. RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

23. Should Be Empty But EISA Board Found
PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

24. Should Have EISA Board But Not Found
PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

25. Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

26. SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

27. Wrong Board In Slot
PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.

Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

28. FLOPPY DISK(S) fail (80) → Unable to reset floppy subsystem.
29. FLOPPY DISK(S) fail (40) → Floppy Type dismatch.
30. Hard Disk(s) fail (80) → HDD reset failed.
31. Hard Disk(s) fail (40) → HDD controller diagnostics failed.
32. Hard Disk(s) fail (20) → HDD initialization error.
33. Hard Disk(s) fail (10) → Unable to recalibrate fixed disk.
34. Hard Disk(s) fail (08) → Sector Verify failed.
35. Keyboard is locked out - Unlock the key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

36. Keyboard error or no keyboard present.

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

37. Manufacturing POST loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

38. BIOS ROM checksum error - System halted.

The checksum of ROM address F0000H-FFFFFH is bad.

39. Memory test fail.

BIOS reports the memory test fail if the onboard memory is tested error.

40. POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.

POST (hex)	Description
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved

POST (hex)	Description
2Dh	1. Initialize multi-language 1. Put information on screen display, including Award title, CPU type, CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB

POST (hex)	Description
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to “AUTO”.
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved

POST (hex)	Description
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: ◆Clear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code

POST (hex)	Description
94h	1. Enable L2 cache 1. Program boot up speed 2. Chipset final initialization. 3. Power management final initialization 4. Clear screen & display summary table 5. Program K6 write allocation 6. Program P6 class write combining
95h	1. Program daylight saving 1. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)