Intel® 820E Chipset

Design Guide

May 2001

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Revision History

Rev.	Description	Date
-001	• Initial Release	June 2000
-002	• Minor edits for clarity	July 2000
-003	• Revised ICH2 sections	May 2001

1. Introduction

The *Intel® 820E Chipset Design Guide* provides design recommendations for systems using the Intel® 820E chipset. This includes motherboard layout, routing guidelines, system design issues, system requirements, debug recommendations, and board schematics. In addition to providing motherboard design recommendations (e.g., layout and routing guidelines), this document also addresses system design issues such as thermal requirements for Intel 820E chipset-based systems. The design recommendations should be used during system design. The guidelines have been developed to provide maximum flexibility to board designers while reducing the risk of board-related issues.

The Intel board schematics in *Appendix A: Reference Design Schematics (Uniprocessor)* implement Intel® PGA370 architecture and are intended for use as references by board designers. While the schematics included cover specific designs, the core schematics for each chipset component remain the same for most Intel 820E chipset platforms. The appendix provides a set of reference schematics for each chipset component, in addition to common motherboard options. Additional flexibility is possible via other permutations of these options and components.

1.1. About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. This design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- *Chapter 1, Introduction* — This chapter introduces the designer to the purpose and organization of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the Intel 820E chipset.
- *Chapter 2, Layout/Routing Guidelines* — This chapter provides a detailed set of motherboard layout and routing guidelines for designing an Intel 820E chipset-based platform. The motherboard's functional units are discussed (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC'97, USB, interrupts, SMBUS, PCD, LPC/FWH Flash BIOS, and RTC).
- *Chapter 4, Advanced System Bus Design* — This chapter discusses the AGTL+ guidelines and theory of operation. It also provides more details about the methodologies used to develop these guidelines.
- *Chapter 4, Clocking* — This chapter provides the motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).
- *Chapter 5, System Manufacturing* — This chapter includes the board stack-up requirements.
- *Chapter 6, System Design Considerations*— This chapter includes the guidelines for power delivery, decoupling, thermal, and power sequencing.
- *Appendix A, Reference Design Schematics (Uniprocessor)* — This appendix provides a set of schematics for uniprocessor designs. It also provides a feature list for board design.

1.2. Reference Documents

- *Intel® 820 Chipset Family: 82820 Memory Controller Hub (MCH) Datasheet* (document number: 290630) http://developer.intel.com/design/chipsets/datashts/290630.htm
- *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket* (document number 298718) http://developer.intel.com/design/chipsets/designex/298178.htm
- *Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet* (document number: 290658) http://developer.intel.com/design/chipsets/datashts/290658.htm
- *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet* (document number: 290687) http://developer.intel.com/design/chipsets/datashts/290687.htm
- *CK97 Clock Synthesizer Design Guidelines* (document number: 243867) http://developer.intel.com/design/PentiumII/applnots/243867.htm
- *VRM 8.4 DC-DC Converter Design Guidelines* (document number 245335) http://developer.intel.com/design/PentiumIII/designgd/245335.htm
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0

Further information regarding the Pentium III processor can be found at http://developer.intel.com/design/PentiumIII/ .

1.3. System Overview

The Intel 820E chipset is designed for Intel® Pentium® III microprocessors and is the first chipset to support the integrated LAN capability and expanded USB capability. It supports the 4× capability of the *AGP 2.0 Interface Specification* and it supports the 400 MHz Direct RDRAM* interface. The 400 MHz, 16-bit, *double-clocked* Direct RDRAM interface provides 1.6-GB/s access to main memory. To provide more efficient communication between chipset components, the hub interface component interconnect is designed into the Intel 820E chipset.

Support of AGP 4×, 400 MHz Direct RDRAM and the hub interface provides a balanced system architecture for the Pentium III processor, minimizing bottlenecks and increasing system performance. By increasing memory bandwidth to 1.6 GB/s by means of 400 MHz Direct RDRAM and by increasing the graphics bandwidth to 1 GB/s by means of AGP 4×, the Intel 820E chipset delivers the data throughput necessary to take advantage of the high performance provided by the powerful Pentium III processors.

In addition, the Intel 820E chipset architecture enables security and manageability infrastructures through the Firmware Hub (FWH)component.

The ACPI-compliant Intel 820E chipset platform can support the Full-On, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the Intel 820E chipset also supports Wake on LAN* for remote administration and troubleshooting.

The Intel 820E chipset architecture eliminates the need for the ISA expansion bus traditionally integrated into the I/O subsystem of Intel chipsets. This eliminates many conflicts experienced when installing hardware and drivers into legacy ISA systems. The elimination of ISA provides true plug and play for the Intel 820E chipset platform. Traditionally, the ISA interface was used for audio and modem devices. The addition of AC'97 allows the OEM to use software-configurable AC'97 audio and modem encoders/decoders (codecs), instead of traditional ISA devices. The 82801BA ICH2 component expands the support of AC'97 to include up to 6-channel audio. The ISA bus can be implemented with a PCI-to-ISA bridge from an external component supplier.

The Intel 820E chipset contains two *core* components: the Memory Controller Hub (MCH) and the I/O Controller Hub 2 (ICH2). The MCH integrates the 133 MHz processor system bus controller, an AGP 2.0 controller, a 400 MHz Direct RDRAM controller, and a high-speed hub interface for communication with the ICH2. The ICH2 integrates an Ultra ATA/100 controller, two USB host controllers, an LPC interface controller, an FWH Flash BIOS interface controller, a PCI interface controller, an AC'97 digital controller, an integrated LAN controller, and a hub interface for communication with the MCH. The Intel 820E chipset provides the data buffering and interface arbitration required to ensure that the system interfaces operate efficiently and provide the system bandwidth necessary to obtain peak performance with the Pentium III processor.

1.3.1. Chipset Components

The Intel 820E chipset consists of the Intel® 82820 Memory Controller Hub (MCH) and the Intel® 82801BA I/O Controller Hub (ICH2). Additional functionality can be provided through the use of a PCI-to-ISA bridge.

Memory Controller Hub (MCH)

The MCH provides the interconnect between the Direct RDRAM and the system logic. It integrates the following functions:

- Support for single or dual Intel PGA370 processors with a 100 MHz or 133 MHz system bus
- 256 MHz, 300 MHz, 356 MHz or 400 MHz Direct RDRAM interface supporting 1 GB of Direct RDRAM
- 4×, 1.5 V AGP interface (3.3 V 1×, 2×, and 1.5 V 1×, 2× devices also supported)
- Downstream hub interface for access to the ICH2

In addition, the MCH provides arbitration, buffering, and coherency management for each of these interfaces. Refer to *Chapter 2 Layout/Routing Guidelines* for more information regarding these interfaces.

I/O Controller Hub 2 (ICH2)

The ICH2 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH2 integrates:

- Upstream hub interface for access to the MCH
- Two-channel Ultra ATA/100 bus master IDE controller
- Two USB controllers (expanded capabilities for 4 ports)
- I/O APIC
- SMBus controller
- FWH interface (FWH Flash BIOS)
- LPC interface
- AC'97 2.1 interface
- PCI 2.2 interface
- Integrated system management controller
- Alert on LAN*
- Integrated LAN controller

The ICH2 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces. Refer to Section 2 for more information on these interfaces.

FWH Flash BIOS

The FWH Flash BIOS component is a key element in providing a new security and manageability infrastructure for the PC platform. The device operates under the FWH Flash BIOS interface and protocol. The hardware features of this device include a unique Random Number Generator (RNG), register-based locking, and hardware-based locking.

ISA Bridge

For legacy needs, ISA support is an optional feature of the Intel 820E chipset. Implementations that require ISA support can benefit from the enhancements of the Intel 820E chipset, while "ISA-less" designs are not burdened with the complexity and cost of the ISA subsystem.

The Intel 820E chipset platform with optional ISA support takes advantage of an external component supplier's ISA bridge, which is a PCI-to-ISA bridge that resides on the PCI bus of the ICH2.

1.3.2. Bandwidth Summary

The following table provides a summary of the bandwidth requirements for the Intel 820E chipset.

Table 1. Intel® 820E Chipset Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (megasamples/s)	Data Width (Bytes)	Bandwidth (MB/s)
Processor bus	100/133	1	100/133	8	800/1066
RDRAM	266/300/356/400	2	533/600/711/800	2	1066/1200/1422/1600
AGP 2.0	66	4	266	4	1066
Hub interface	66	4	266	1	266
PCI 2.2	33	1	33	4	133

1.3.3. System Configuration

The following figures show typical platform configurations using the Intel 820E chipset:

Figure 1. Intel® 820E Chipset Platform Performance Desktop Block Diagram

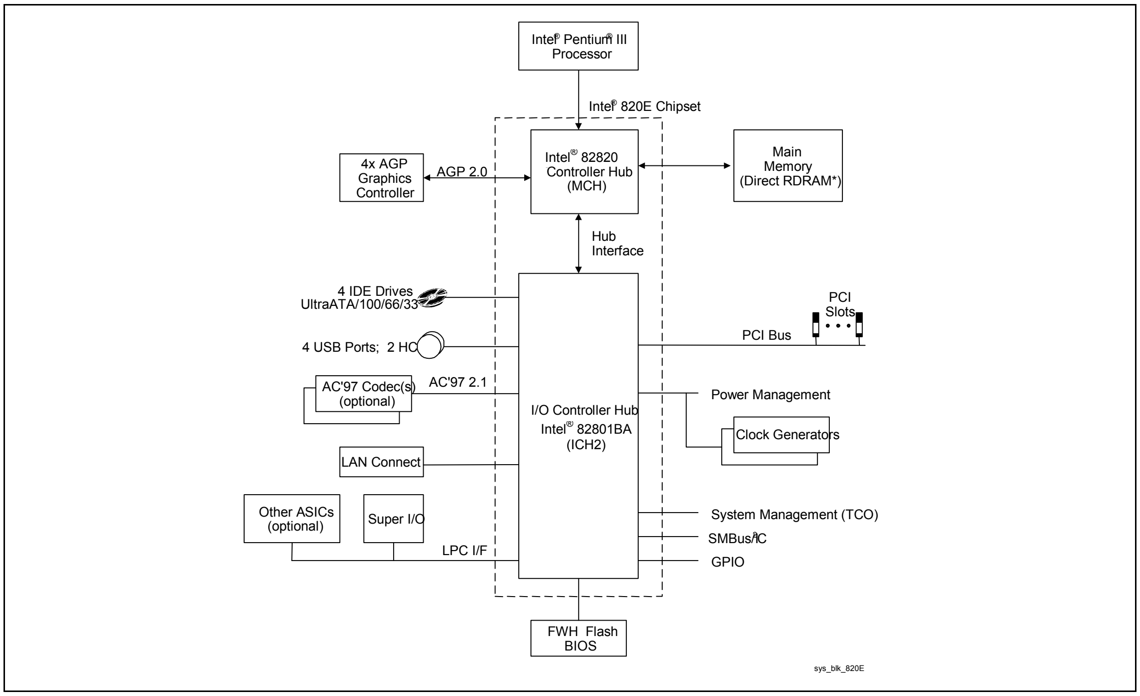


Figure 2. Intel® 820E Chipset Platform Performance Desktop Block Diagram (with ISA Bridge)

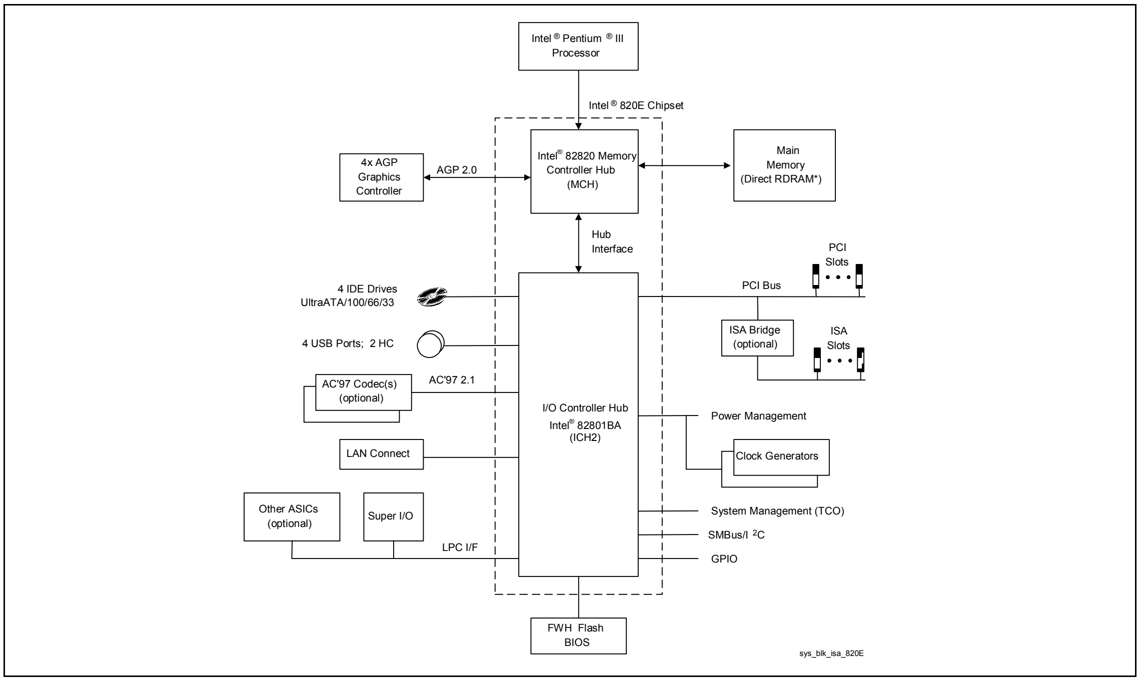
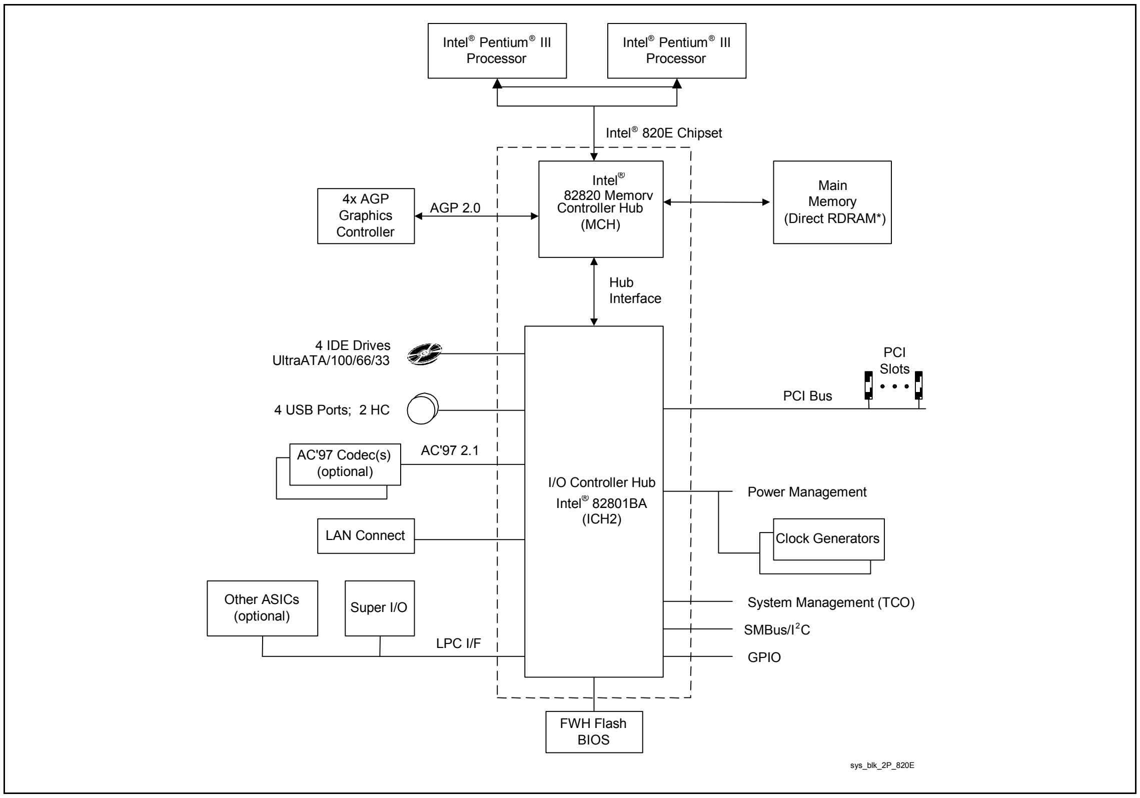


Figure 3. Intel® 820E Chipset Platform Dual-Processor Performance Desktop Block Diagram



1.4. Platform Initiatives

1.4.1. Direct Rambus RAM (RDRAM*)

The Direct Rambus RAM (RDRAM) initiative provides the memory bandwidth necessary to obtain optimal performance from the Pentium III processor as well as a high-performance AGP graphics controller. The MCH RDRAM interface supports 266 MHz, 300 MHz, 356 MHz, and 400 MHz operation. The latter delivers 1.6 GB/s of theoretical memory bandwidth, which is twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the heavily pipelined RDRAM protocol provides substantially more efficient data transfer. The RDRAM memory interface can utilize more than 95% of the 1.6-GB/s theoretical maximum bandwidth.

In addition to the RDRAM's performance features, the new memory architecture provides enhanced power management capabilities. The powerdown mode of operation allows Intel 820E chipset-based systems to provide cost-effective support of Suspend to RAM.

1.4.2. Streaming SIMD Extensions

The Pentium III processor provides 70 new streaming SIMD (single-instruction, multiple-data) extensions. The Pentium III processor's new extensions are floating-point SIMD extensions. Intel® MMX™ technology provides integer SIMD extensions. The Pentium III processor's new extensions complement the Intel MMX technology SIMD extensions and provide a performance boost to floating-point-intensive 3D applications.

1.4.3. AGP 2.0

In combination with Direct RDRAM memory technology, the AGP 2.0 interface allows graphics controllers to access main memory at over 1 GB/s, which is twice the AGP bandwidth of previous AGP platforms. AGP 2.0 provides the infrastructure necessary *for photorealistic 3D. In* conjunction with Direct RDRAM and the Pentium III processor's new streaming SIMD extensions, AGP 2.0 delivers the next level of 3D graphics performance.

1.4.4. Hub Interface

As the I/O speed has increased, the demand placed on the PCI bus by the I/O bridge has become significant. With the addition of AC'97 and ATA/100, coupled with the existing USB, I/O requirements will begin to affect PCI bus performance. The Intel 820E chipset's hub interface architecture ensures that the I/O subsystem—both PCI and the integrated I/O features (IDE, AC'97, USB, etc.)—will receive adequate bandwidth. By placing the I/O bridge on the hub interface instead of the PCI, the hub architecture ensures that both the I/O functions integrated into the ICH2 and the PCI peripherals will obtain the bandwidth necessary for peak performance. In addition, the hub interface's lower pin count allows a smaller package for the MCH and ICH2.

1.4.5. Integrated LAN Controller

The ICH2 component incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high-level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN connect components, allowing the targeting of the desired market segment. The Intel® 82562EH component provides a HomePNA 1-Mbit/sec connection. The Intel® 82562ET component provides a basic Ethernet* 10/100 connection. The Intel® 82562EM component provides an Ethernet 10/100 connection with the added flexibility of Alert on LAN. More advanced LAN solutions can be implemented with the Intel® 82550 or other PCI-based product offerings.

1.4.6. Ultra ATA/100 Support

The ICH2 (82801BA) component supports the IDE controller with two sets of interface signals (primary and secondary) that can be enabled independently, tri-stated or driven low. The component supports UltraATA/100, Ultra ATA/66, UltraATA/33, and multiword p modes for transfers of up to 100 Mbytes/sec.

1.4.7. Expanded USB Support

The ICH2 component contains two USB host controllers. Each host controller includes a root hub with two separate USB ports each, for a total of four USB ports. The addition of a USB host controller expands the functionality of the platform.

1.4.8. Manageability

The Intel 820E chipset platform integrates several functions designed to manage the system and lower the system's total cost of ownership (TCO). These system management functions are designed to report errors, diagnose the system, and recover from system lock-ups, without the aid of an external microcontroller.

TCO Timer

The ICH2 integrates a programmable TCO timer, which is used to detect system locks. The first expiration of the timer generates an SMI#, which the system can use to recover from a software lock. The second expiration of the timer causes a system reset, to recover from a hardware lock.

Processor Present Indicator

The ICH2 looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH2 will reboot the system at the safe-mode frequency multiplier.

ECC Error Reporting

After detecting an ECC error, the MCH can send one of several messages to the ICH2. The MCH can instruct the ICH2 to generate either an SMI#, NMI#, SERR# or TCO interrupt.

Function Disable

The ICH2 provides the ability to disable the following functions: AC’97 Modem, AC’97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory or PCI configuration space. Also, no interrupts or power management events are generated by the disabled functions.

Intruder Detect

The ICH2 provides an input signal (INTRUDER#) that can be attached to a switch that is activated when the system case is opened. The ICH2 can be programmed to generate an SMI# or TCO interrupt resulting from an active INTRUDER# signal.

SMBus

The ICH2 integrates an SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RIMMs and thermal sensors. The slave interface allows an external microcontroller to access system resources.

The Intel 820E chipset platform integrates several functions designed to expand the capability of interfacing several components to the system.

Interrupt Controller

The interrupt capabilities of the Intel 820E chipset platform expands support for up to eight PCI interrupt pins and PCI 2.2 message-based interrupts. In addition, the ICH2 supports system bus interrupt delivery.

FWH Flash BIOS

The Intel 820E chipset-based system platform supports firmware hub BIOS memory sizes up to 8 MB, for increased system flexibility.

Alert on LAN*

The ICH2 supports Alert on LAN. In response to a TCO event (intruder detect, thermal event, processor not booting), the ICH2 sends a message over ALERTCLK and ALERTDATA to alert the network manager.

1.4.9. AC'97

The *Audio Codec '97* (AC'97) specification defines a digital interface that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC) or both an AC and an MC. The AC'97 specification defines the interface between the system logic and the audio or modem codec, known as the AC'97 Digital Link.

The Intel 820E chipset platform's AC'97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC'97 digital link. The use of the ICH2-integrated AC'97 digital link reduces cost and eases migration from ISA.

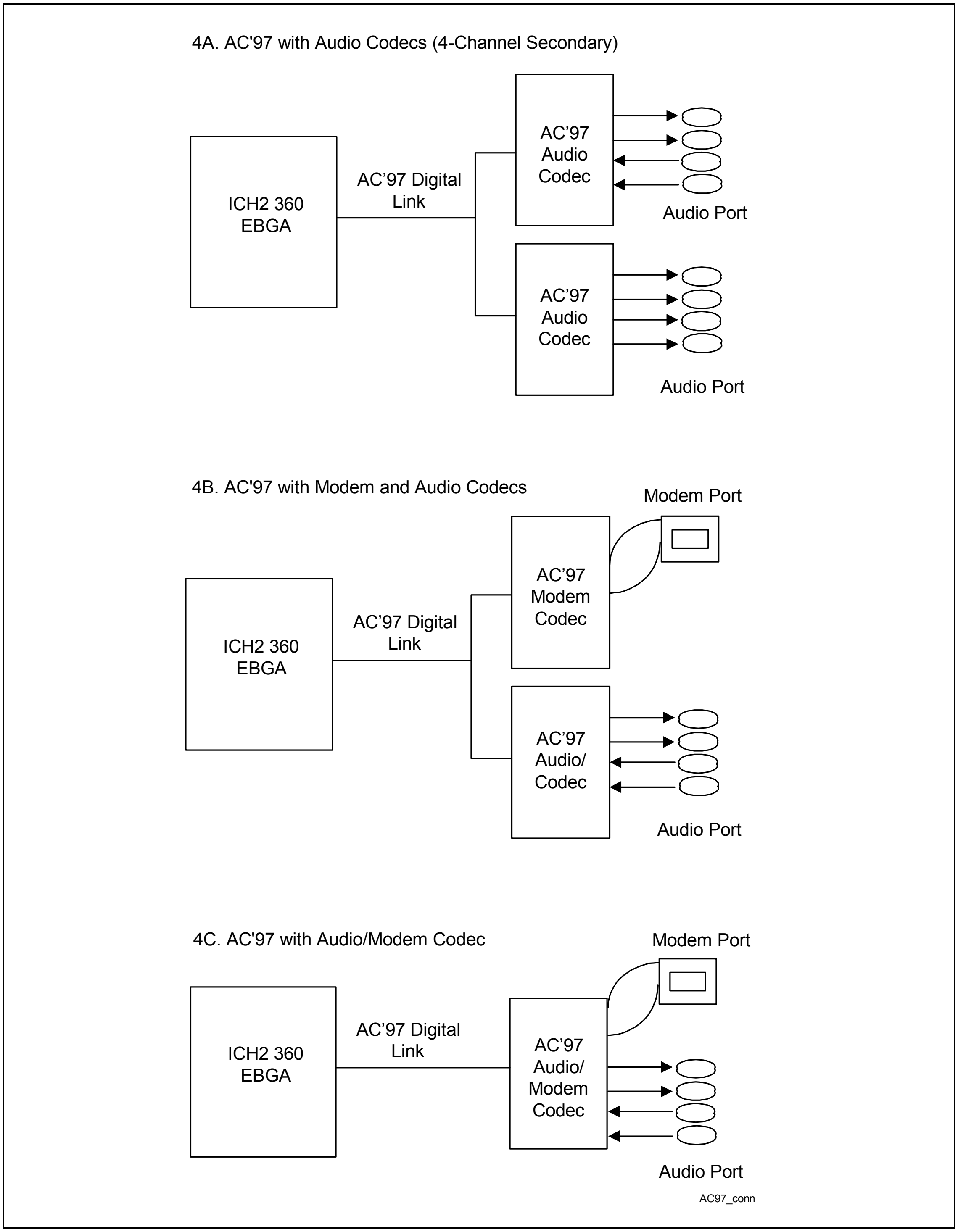
By using an audio codec, the AC'97 digital link allows for cost-effective, high-quality, integrated audio on an Intel 820E chipset-based platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC'97. The ICH2-integrated digital link allows several external codecs to be connected to the ICH2. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 4C). The digital link is expanded to support two audio codecs or a combination of an audio and modem codec (Figures 4A and 4B).

The modem implementations for different countries must be taken into consideration, because telephone systems may vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. Intel is developing an AC'97 digital link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel, where the external ports can be located.

The digital link in the ICH2 is compliant with Revision 2.1 of the AC'97 specification, so it supports two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality, two-speaker audio solution. Wake on Ring from Suspend also is supported with the appropriate modem codec.

The ICH2 expands the audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and Woofer, for a complete surround-sound effect. ICH2 has expanded support for two audio codecs on the AC'97 digital link.

Figure 4. (A-C) AC'97 Connections



1.4.10. Low-Pin-Count (LPC) Interface

In the Intel 820E chipset platform, the super I/O component has migrated to the Low-Pin-Count (LPC) interface. Migration to the LPC interface enables lower-cost super I/O designs. The LPC super I/O component requires the same feature set as traditional super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In systems with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface. Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

In addition, depending on system requirements, a device bay controller and USB hub could be integrated into the LPC super I/O component. For systems requiring ISA support, an ISA-IRQ to serial-IRQ converter is required. This converter could be integrated into the super I/O.

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2. Layout/Routing Guidelines

This chapter documents the motherboard layout and routing guidelines for Intel 820E chipset-based systems. This chapter does not discuss the functional aspects of any bus or the layout guidelines for an add-in device.

Caution: If the guidelines in this document are not followed, it is very important to complete thorough signal integrity and timing simulations for each design. Even if the guidelines are followed, critical signals still should be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented be followed precisely. Any deviation from these guidelines must be simulated!

2.1. General Recommendations

The trace impedance typically noted (i.e., 60 Ω ± 10%) is the "nominal" trace impedance. That is, it is the impedance of a trace when not subjected to the fields created by changing the current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. This trace-to-trace coupling can be minimized by using wider spaces between the traces. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this chapter should be followed. In addition, the PCB should be fabricated as documented in Section 5.1.

Except where noted, all recommendations in this chapter assume 5 mil-wide traces. If the trace width is greater than 5 mils, then the trace spacing requirements must be adjusted accordingly (and linearly). For example, this chapter recommends routing most AGP signals with 5 mil traces on 20 mil spaces (1:4). If 6 mil traces are used, then 24 mil spaces must be used (also 1:4). Using a wider trace—and therefore wider spaces—will make routing more difficult.

Additionally, these routing guidelines are created using the stack-up described in Section 5.1. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

2.2. Component Quadrant Layout

The quadrant layouts shown are approximate and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 5. MCH 324-Ball µBGA* CSP Quadrant Layout (Top View)

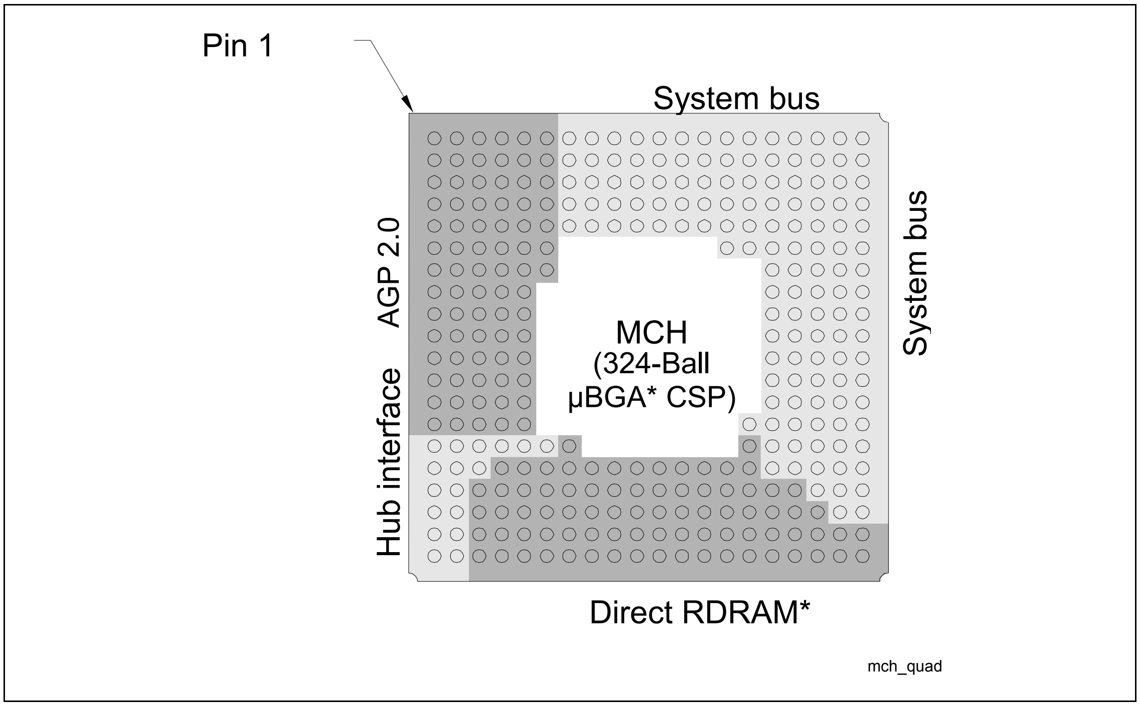
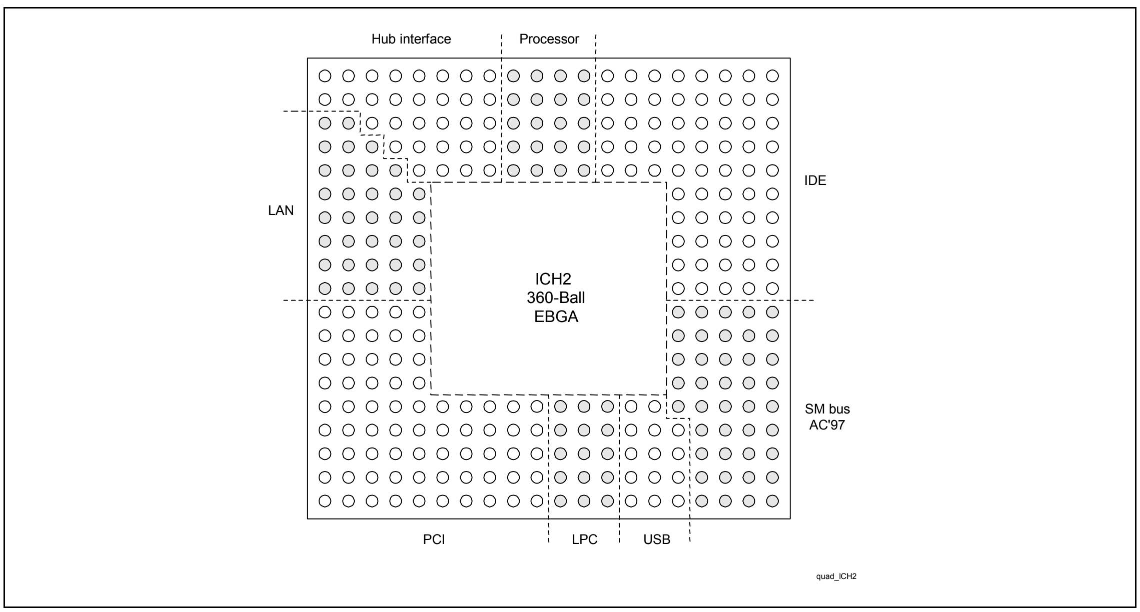


Figure 6. ICH2 360-Ball EBGA Quadrant Layout (Top View)

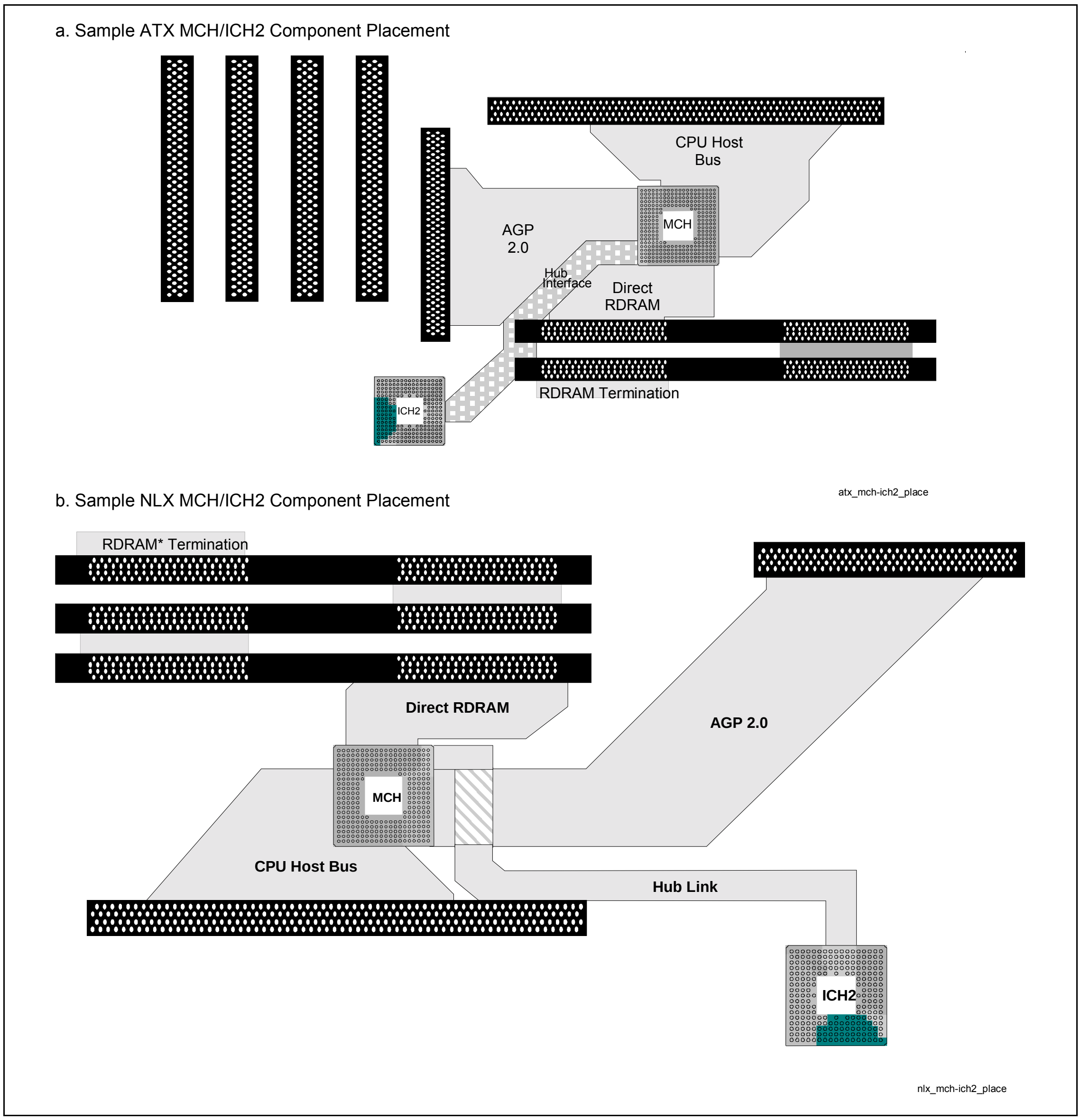


2.3. Intel® 820E Chipset Component Placement

Notes:

1. The ATX and NLX placements and layouts shown in the following figure are recommended for single (UP) Intel 820E chipset-based system design.
2. The trace length limitation between critical connections will be discussed later in this document.
3. The figure is for reference only.

Figure 7. Sample ATX and NLX MCH/ICH2 Component Placement



Note: Actual ICH2 placement may vary.

2.4. Core Chipset Routing Recommendations

The following two figures show MCH core routing examples:

Figure 8. Primary-Side MCH Core Routing Example (ATX)

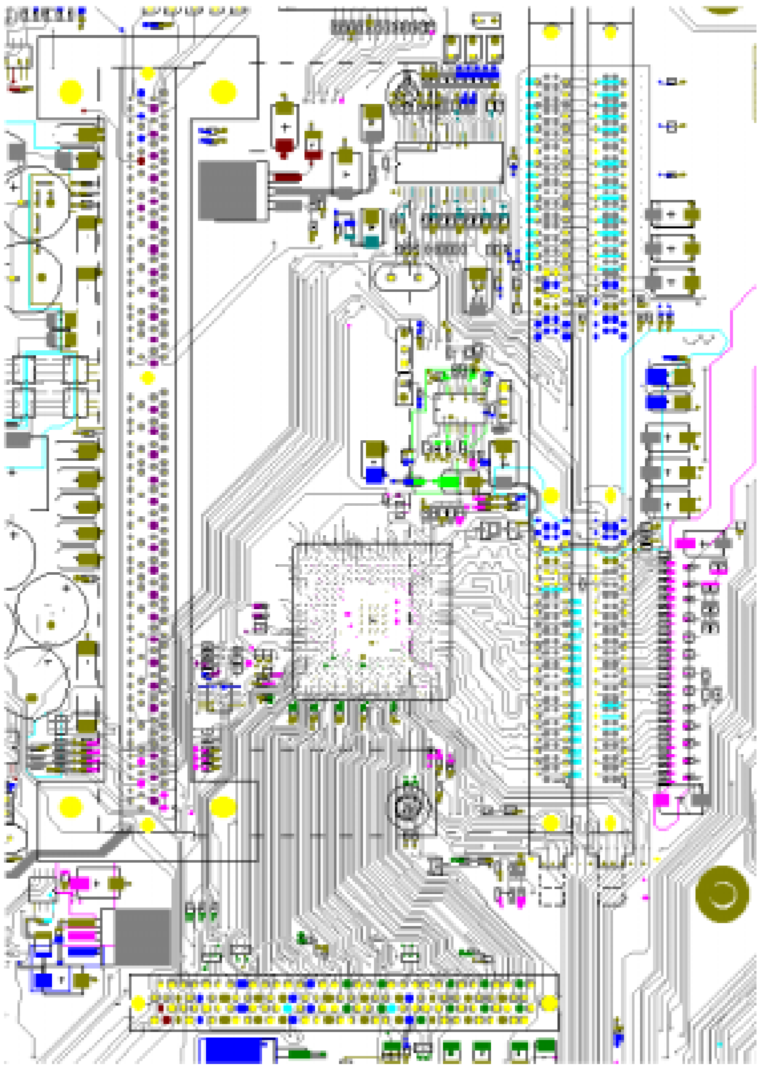
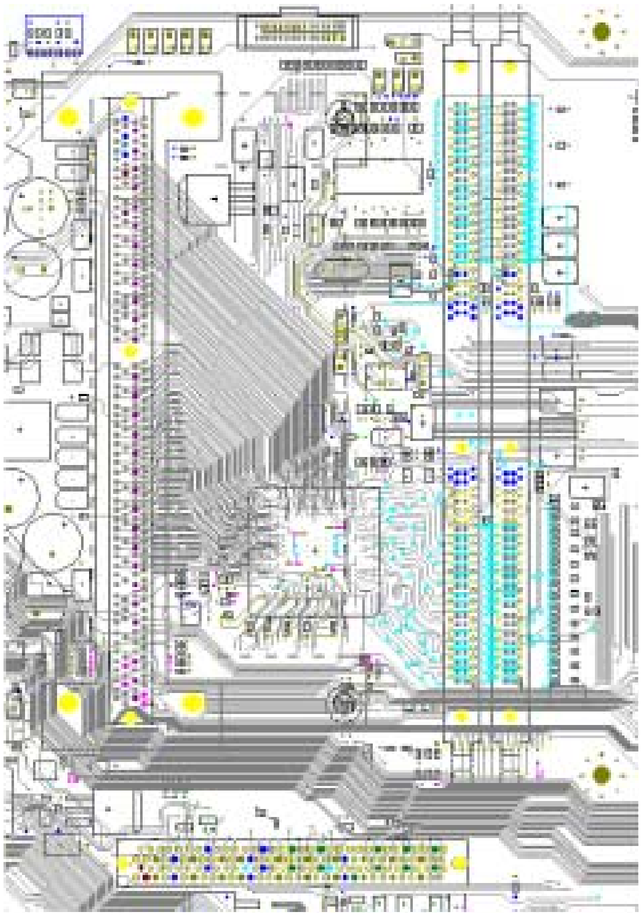


Figure 9. Secondary-Side MCH Core Routing Example (ATX)

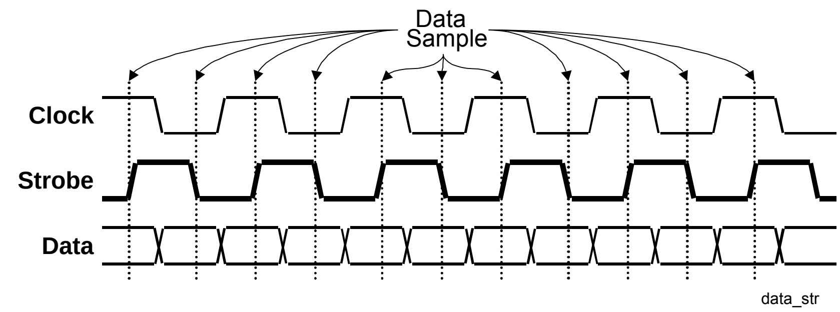


2.5. Source-Synchronous Strobing

A technology used in AGP 4×, Direct RDRAM and the hub interface, source-synchronous strobing allows very high data transfer rates. As buses become faster and cycle times become shorter, the propagation delay becomes a limiting factor in the bus speed. Source-synchronous strobing is used to minimize the effect of propagation delay (T_{PROP}) on maximum bus frequency.

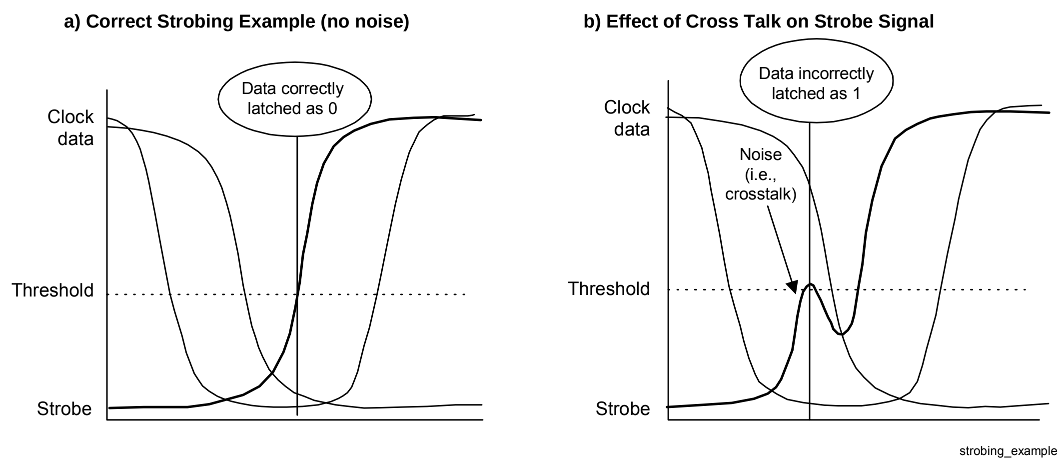
A source-synchronous-strobed interface uses strobe signals, instead of the clock, to indicate that data is valid. Refer to the following example figure:

Figure 10. Data Strobing Example



For a source-synchronous-strobed interface, it is **very important** that the strobe signals be routed carefully. These signals must be very clean (i.e., free of noise). Data signals typically are latched on the rising or falling edge of the strobe signal (or both). If there is noise on these signals, it could cause an extra "edge" to be detected, thus latching incorrect data. Refer to the following example figures.

Figure 11. Effect of Crosstalk on Strobe Signal



Some buses have more than one strobe (i.e., AGP). The AGP 1.0 specification (1× and 2× modes) employs three strobe signals, each of which is used to strobe different data signals (i.e., each strobe has an associated set of data signals). The associations for AGP 1.0 (AGP 2×) are listed in the following table. Refer to Section 2.8 for more information on AGP 2.0 (AGP 4×, 1.5 V).

Table 2. AGP 2× Data/Strobe Association

Data	Associated Strobe
AD[15:0] and C/BE[1:0]#	AD_STB0
AD[31:16] and C/BE[3:2]#	AD_STB1
SBA[7:0]	SB_STB

In this example, the lower address signals (AD[15:0]) are sampled on the rising and falling edges of AD_STB0, while the upper address signals (AD[31:16]) are sampled on the rising and falling edges of AD_STB1.

When routing strobes and their associated data lines, trace length mismatch is very important, in addition to noise immunity. The primary benefit of source-synchronous strobing is that the data and the strobe arrive simultaneously at the receiver. Thus, a strobe and its associated data signals have very critical length mismatch requirements. With well matched trace lengths (as well as matched impedance), the propagation delays for the strobe and the data will be very close. Hence, the strobe and the data arrive simultaneously at the receiver. For some interfaces, the trace length mismatch requirement is less than 0.25 inch.

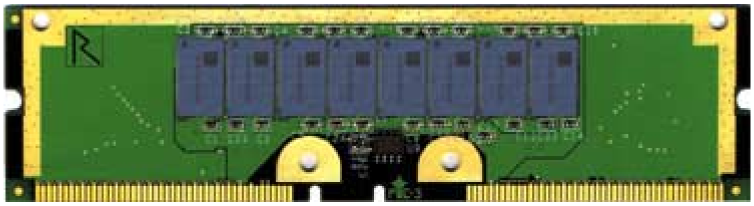
2.6. Differential Clocking/Strobing

AGP 2× timings are referenced at a particular level on the rising or falling strobe edge, while 4× timings are referenced to the crossover point of the differential strobes. The crossover is targeted to be at 0.5 V_{DDQ}.

2.7. Direct RDRAM* Interface

The Direct RDRAM channel is a multi-symbol interconnect. Because of the length of the interconnect and the frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. The driving device sends the next data out before the previous data has left the bus.

Figure 12. RIMM Diagram



The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in reflected voltage levels is required. The interconnect transmission lines must be terminated at their characteristic impedance, or the reflected voltage resulting from an impedance mismatch will degrade the signal quality. These reflections will reduce noise and timing margins and will reduce the maximum operating frequency of the bus. The reflections could create data errors.

Because of the tolerances of components such as PCBs, connectors, and termination resistors, there will be some reflected voltage on the interconnect. In this multi-symbol interconnect, timings are pattern dependent because the reflections interfere with the next transfer.

Additionally, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source-synchronous designs, the odd- and even-mode propagation velocity change creates a skew between the clock and data or command lines, which reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease the crosstalk, as well as the other sources of skew.

To achieve these bus requirements, the Direct RDRAM channel is designed to operate as a transmission line. All components, including the individual RDRAMs, are incorporated into the design to create a uniform bus structure that can support up to 33 devices (including the MCH), running at 800 megatransfers/second (MT/s).

2.7.1. Stack-Up

The perfect matching of transmission line impedance and a uniform trace length is essential for the Direct RDRAM interface to work properly. Maintaining a 28 Ω (± 10%) loaded impedance for every RSL (Direct RDRAM Signaling Level) signal has changed the requirements for trace width and prepreg thickness for the Intel 820E chipset platform. (Refer to Section 5.1.)

Achieving a 28 Ω nominal impedance with a traditional 7 mil prepreg requires 28 mil-wide traces. These traces are too wide to break out of the two rows of RSL balls on the MCH. To reduce the trace width, a 4.5 mil-thick prepreg is required. This thinner prepreg allows 18 mil-wide traces to meet the 28 Ω (± 10%) nominal impedance requirement. (Refer to Section 5.1, for detailed stack-up requirements.)

2.7.2. Direct RDRAM* Layout Guidelines

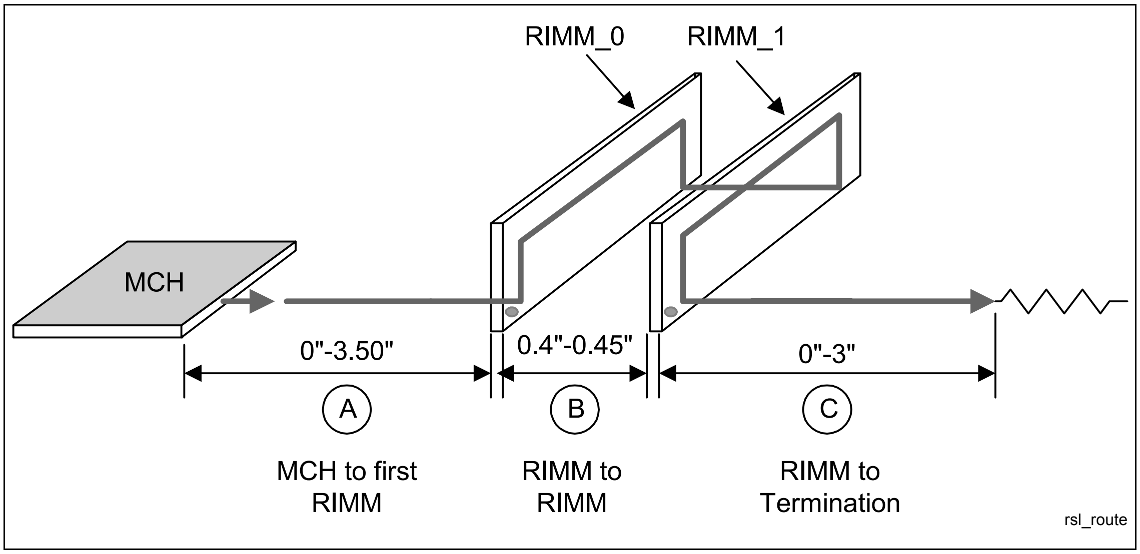
The signals on the Direct RDRAM channel are broken into three groups: RSL signals, CMOS signals, and clocking signals as follows:

- RSL signals
  - DQA[8:0]
  - DQB[8:0]
  - RQ[7:0]
- CMOS signals
  - CMD (high-speed CMOS signal)
  - SCK (high-speed CMOS signal)
  - SIO
- Clocking signals
  - CTM, CTM#
  - CFM, CFM#

2.7.2.1. RSL Routing

The RSL signals enter the first RIMM on the left side, propagate through the RIMM, and exit on the right. The signal continues through the rest of the existing RIMMs until it is terminated at V_{TERM}. All unpopulated slots must have continuity modules in place to ensure that the signals propagate to the termination.

Figure 13. RSL Routing Dimensions



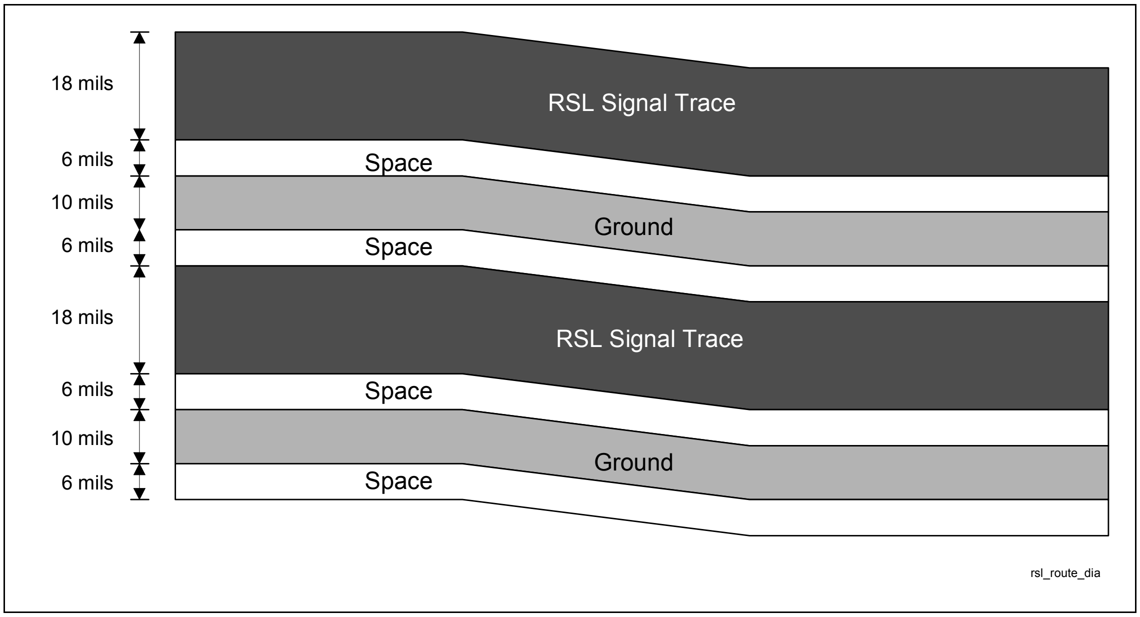
To maintain a nominal 28 Ω trace impedance, the RSL signals must be 18 mils wide. To control crosstalk and odd/even-mode velocity deltas, there must be a 10 mil ground isolation trace routed between adjacent RSL signals. The 10 mil ground isolation traces must be connected to ground with a via every 1 inch. A 6 mil gap is required between the RSL signals and the ground isolation trace. These signals must be length-matched to ±10 mils in line section A and to ±2 mils in line section B, using the trace length matching methods in Section 2.7.2.6. To ensure uniform trace lines, trace width variation must be uniform on all RSL signals at every neckdown for each line section. All RSL signals must have the same number of vias. It may be necessary to place vias on RSL signals where they are not necessary to meet this via loading requirement (i.e., dummy vias).

Table 3. Placement Guidelines for Motherboard Routing Lengths

Reference	Trace Description	Maximum Trace Length (in.)
A	MCH to first RIMM connector	0 to 3.50
B	RIMM to RIMM	0.4 to 0.45
C	RIMM to termination	0 to 3

The following figure shows a top view of the trace width/spacing requirements for the RSL signals.

Figure 14. RSL Routing Diagram



The following two figures show the top view of an example RSL breakout and route.

Figure 15. Primary-Side RSL Breakout Example

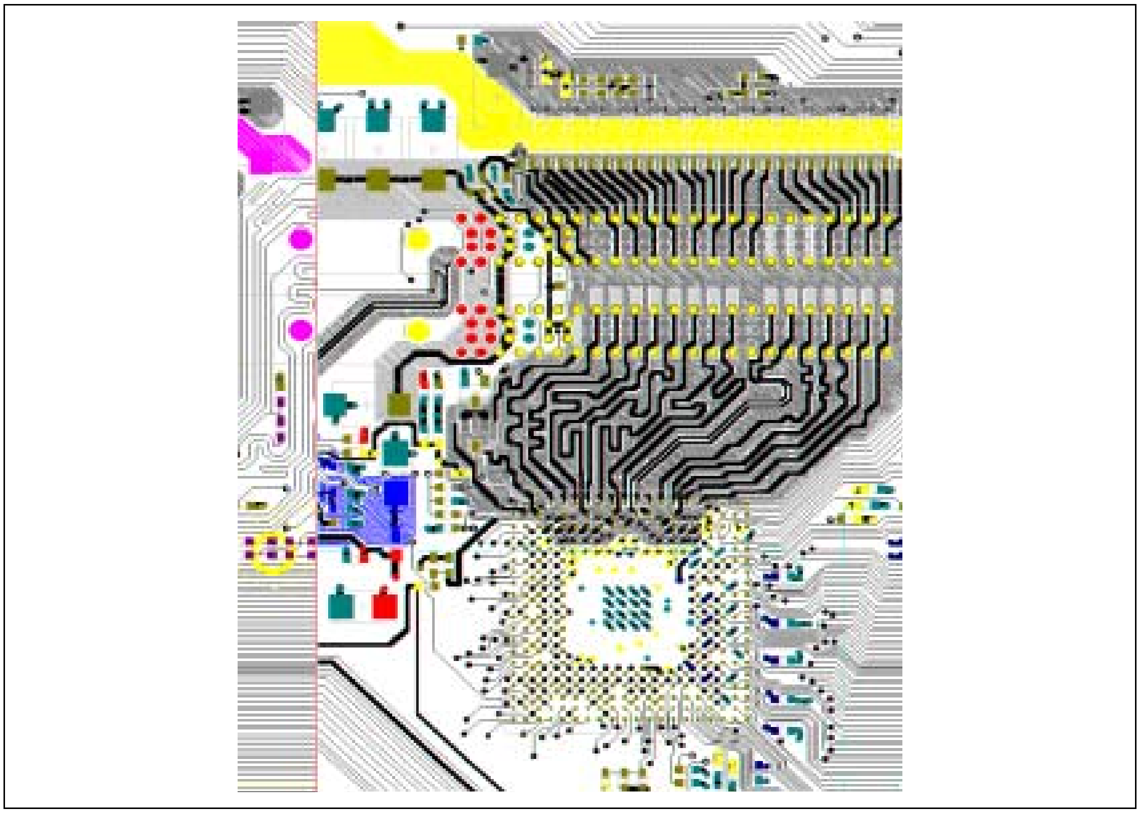
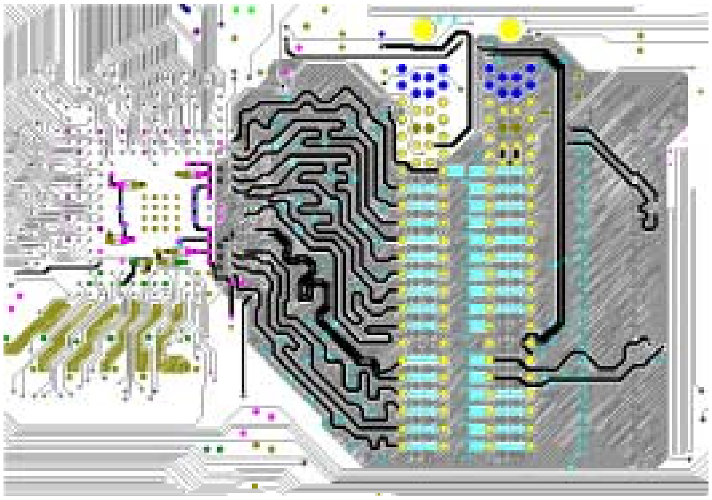


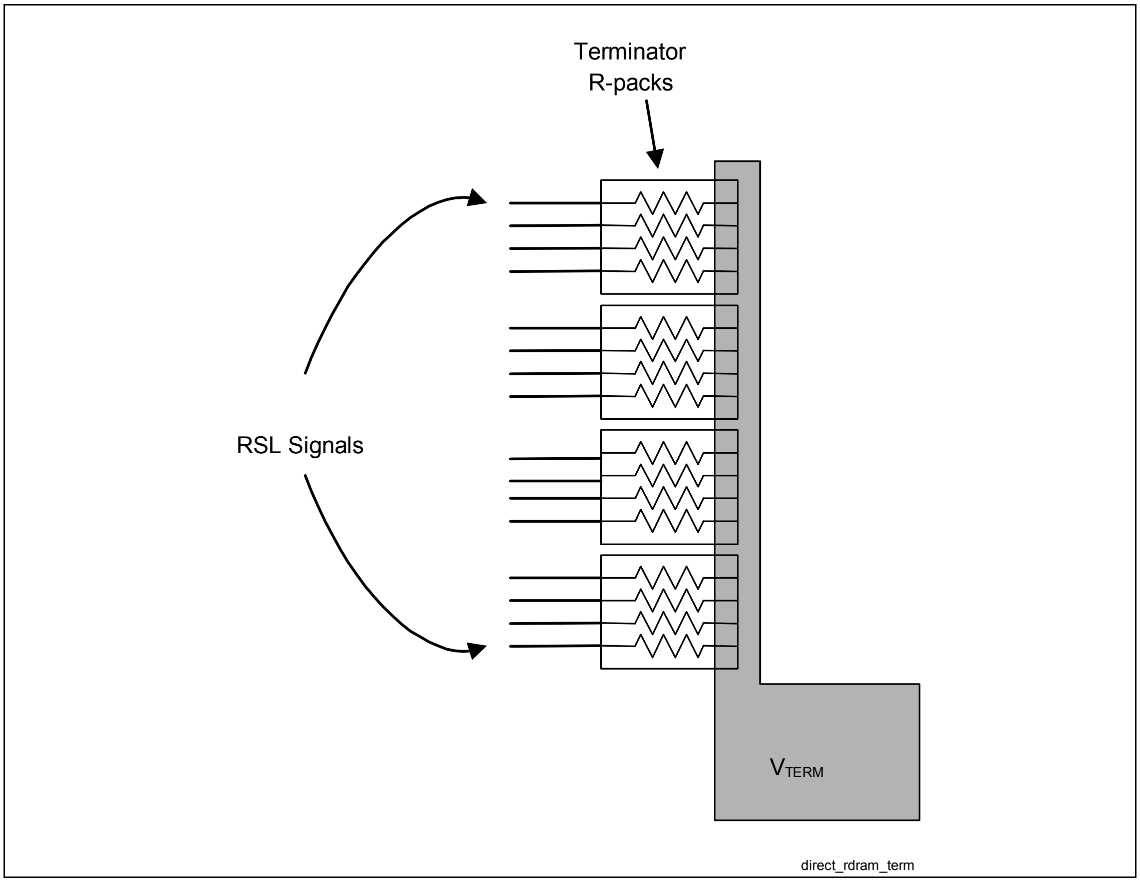
Figure 16. Secondary-Side RSL Breakout Example



2.7.2.2. RSL Termination

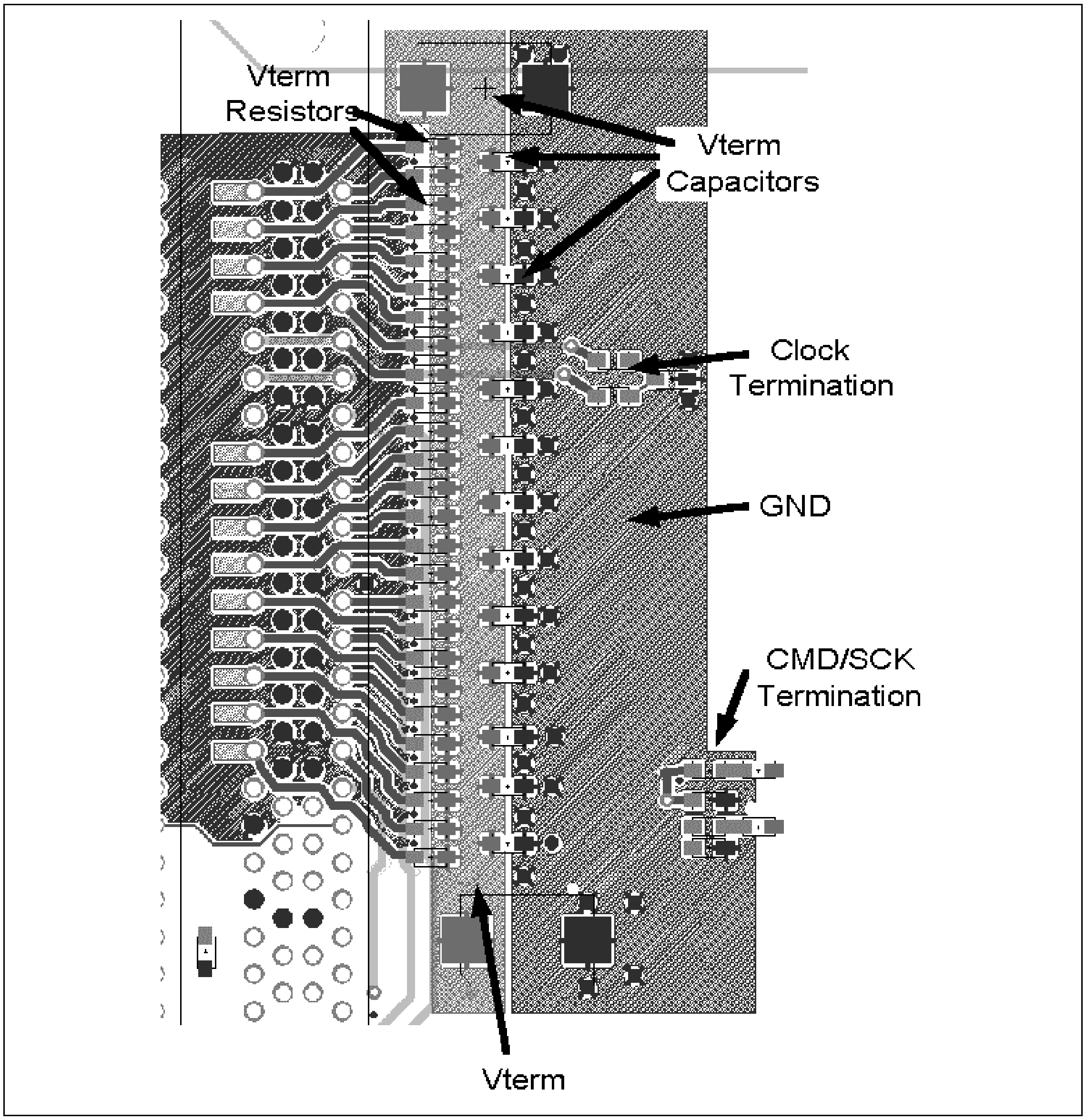
All RSL signals must be terminated to 1.8 V (V_{TERM}) using 27-Ω 1% or 28 Ω 2% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable. V_{TERM} must be decoupled using high-speed bypass capacitors—one 0.1 µF ceramic chip capacitor per two RSL lines—near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with an approximately 20 ms response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM and the termination resistors should be less than 3 inches. Length matching in this section of the channel is not required. The V_{TERM} power island should be **at least** 50 mils wide. This voltage need not be supplied during Suspend to RAM.

Figure 17. Direct RDRAM Termination



Note: It is necessary to compensate for the slight difference in electrical characteristics between a dummy via and a real via. Refer to Section 2.7.2.7 for more information on via compensation.

Figure 18. Direct RDRAM* Termination Example



2.7.2.3. Direct RDRAM* Ground Plane Reference

All RSL signals must be referenced to GND to provide the optimal current return path. The Direct RDRAM ground plane reference must be continuous to the V_{TERM} capacitors. The ground reference island under the RSL signals must be continuous from the last RIMM to the back of the termination capacitors. Choose a reference island shape that does not compromise power delivery to the components. The return current will flow through the V_{TERM} capacitors into the ground island and under the RSL traces. Any split in the ground island will provide a suboptimal return path. In a four-layer board, this will require the V_{TERM} island to be on an outer layer. The V_{TERM} island should **always** be placed on the top layer.

Figure 19. Incorrect Direct RDRAM* Ground Plane Referencing

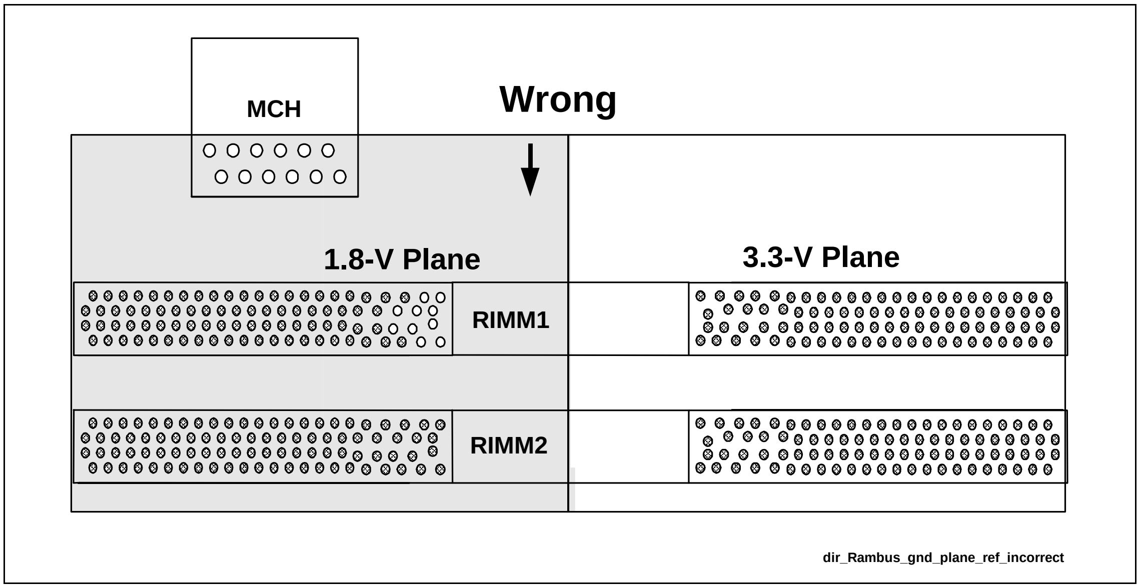
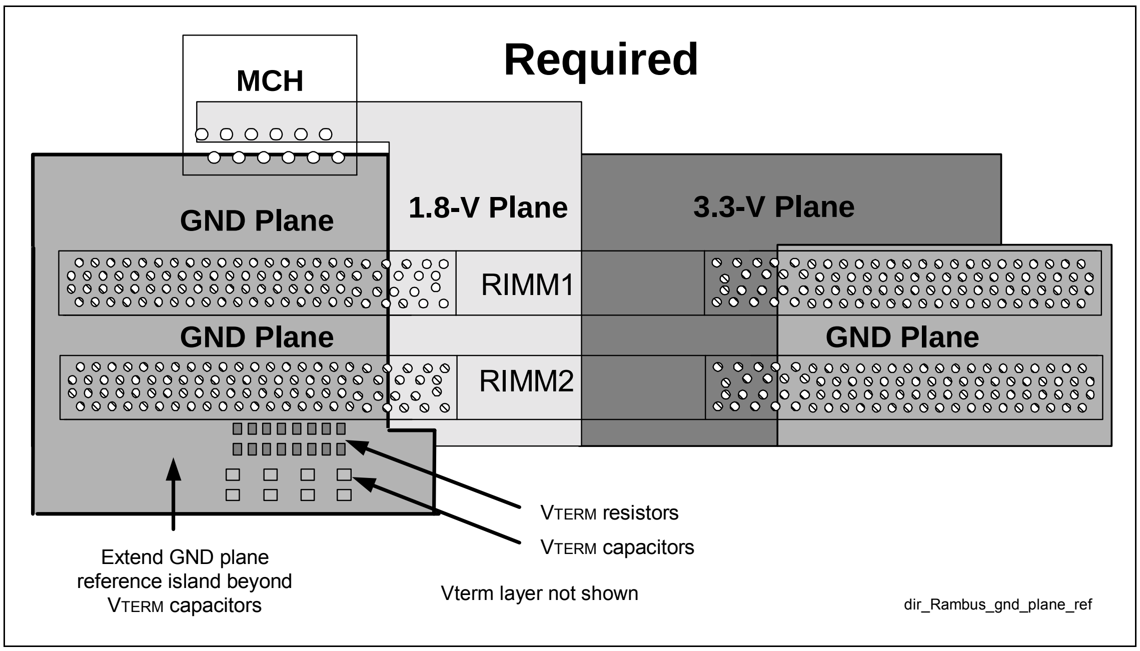


Figure 20. Direct RDRAM* Ground Plane Reference



The ground reference island under the RSL signals MUST be connected to the ground pins on the RIMM connector and the ground vias used to connect the ground isolation on the first and fourth layers.

All four layers of the motherboard require correct grounding between the RSL signals on the motherboard, as follows:

- Layer 1 = Ground isolation
- Layer 2 = Ground plane
- Layer 3 = Ground reference in the power plane
- Layer 4 = Ground isolation

All ground vias and pins MUST be connected to all 4 layers.

2.7.2.4. Direct RDRAM* Connector Compensation

The RIMM connector inductance causes an impedance discontinuity on the Direct RDRAM channel. This may reduce the voltage and timing margin.

To compensate for the inductance of the connector, an approximately 0.65 pF to 0.85 pF compensating capacitive tab (C-TAB) is required on each RSL connector pin. This compensating capacitance must be added to the following connector pins at each connector:

LCTM	LCTM#
RCTM	RCTM#
LCFM	LCFM#
RCFM	RCFM#
LROW[2:0]	RROW[2:0]
LCOL[4:0]	RCOL[4:0]
RDQA[8:0]	LDQA[8:0]
RDQB[8:0]	LDQB[8:0]
SCK	CMD

This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector. The target value is approximately 0.65 pF – 0.85 pF. The copper tab area for the recommended stack-up was determined by means of simulation. The copper tabs can be placed on any signal layer, independently of the layer on which the RSL signal is routed.

The following equation is an approximation usable for calculating the copper tab area on an outer layer.

Equation 1. Approximate Copper Tab Area Calculation

$$\text{Length} \times \text{Width} = \text{Area} = C_{PLATE} \times \text{Thickness of prepreg} / [(\varepsilon_0)(\varepsilon_r)(1.1)]$$

Where:

- — $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil
- — ε_r = Relative dielectric constant of prepreg material
- — Thickness of prepreg (stack-up dependent)
- — Length, Width = Dimensions (in mils) of copper plate to be added
- — Factor of 1.1 accounts for fringe capacitance.

Based on the stack-up requirement in Section 5.1, the copper tab area should be 2800 to 3600 square mils. Different stack-ups require different copper tab areas. The following table lists example copper tab areas.

Table 4. Copper Tab Area Calculation

Dielectric Thickness (D)	Separation between Signal Trace and Copper Tab	Min. Ground Flood	Air Gap between Signal and GND Flood	Compensating Capacitance (pF)	Copper Tab (C-TAB) Area (A) (sq. mils)	C-TAB Shape (mils)
4.5	6	10	6	0.65	2800	140 L x 20 W 70 L x 40 W

Based on Equation 1, the tab area is 2800 sq. mils, where ε_r is 4.2 and D is 4.5. These values are based on 2116 prepreg material.

Note that more than one copper tab shape may be used. The tab dimensions are based on the copper area over the ground plane. The actual length and width of the tabs may differ as a result of routing constraints (e.g., if the tab must extend to center of hole, or antipad). However, each copper tab should have the equivalent area. For example, the copper tabs in Figure 21 have the following dimensions, when measured tangentially to the antipad:

Inner C-TAB = 140 (length) × 20 (width)

Outer C-TAB = 70 (length) × 40 (width)

Figures 21 through 25 show a routing example of tab compensation capacitors. Note that ground floods around the RIMM pins must not be interrupted by the capacitor tabs, and they must be connected to avoid discontinuity in the ground plane, as shown.

Figure 21. Connector Compensation Example

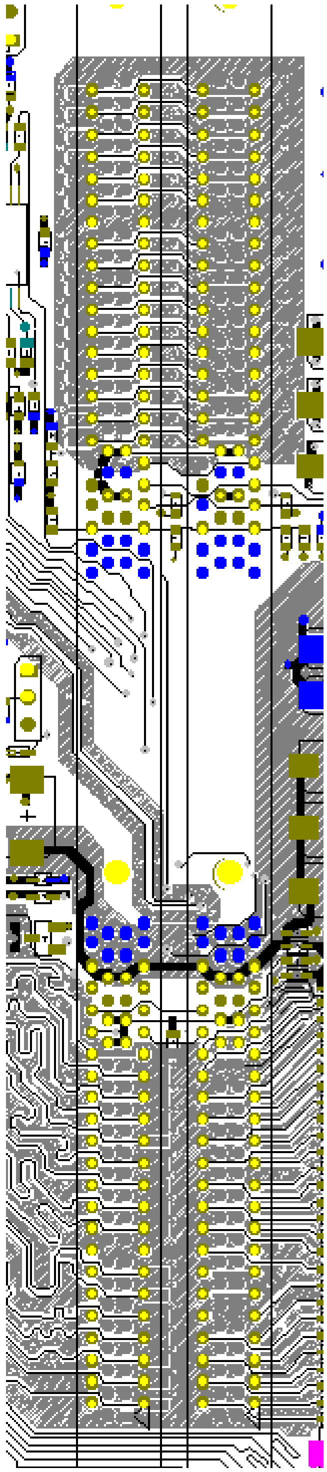
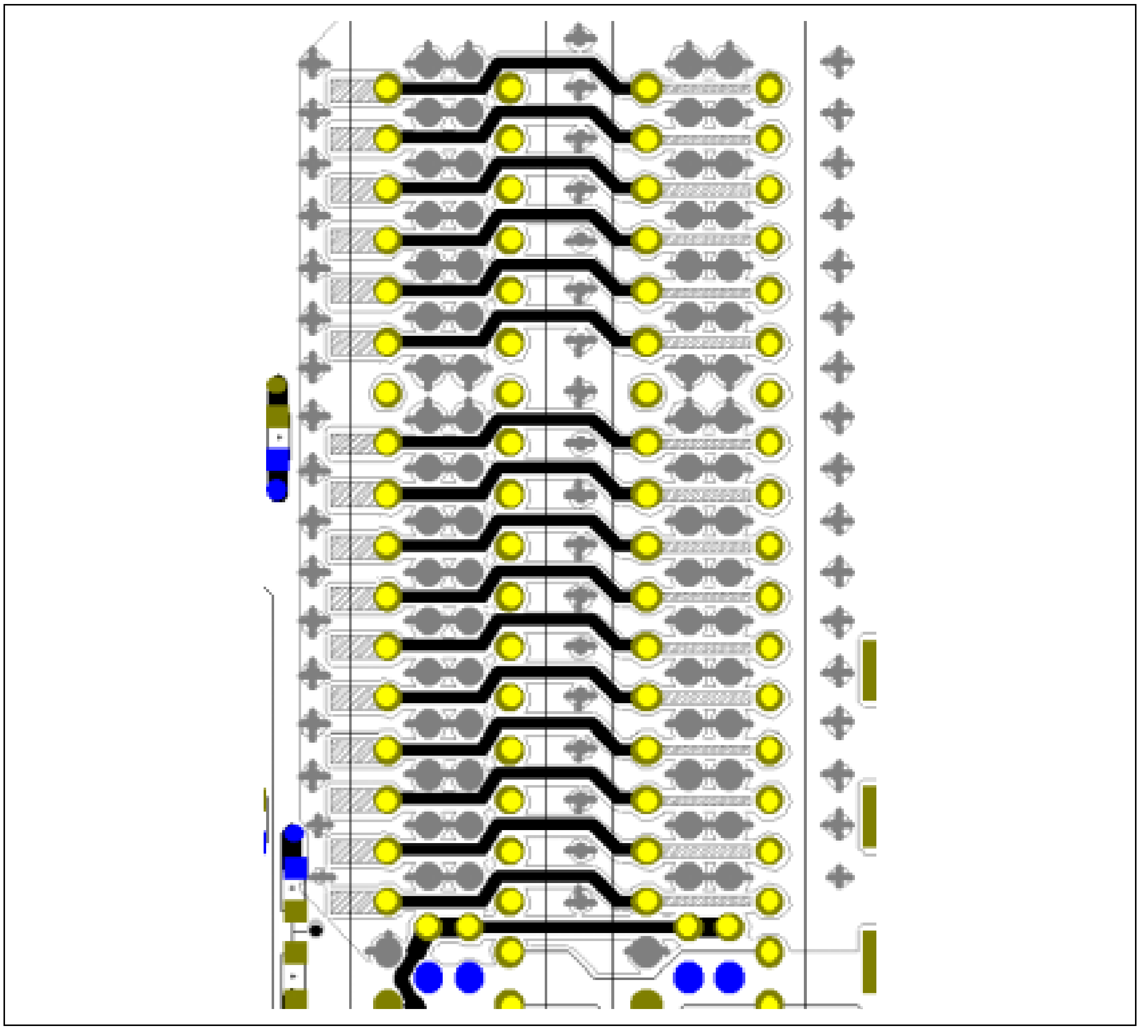
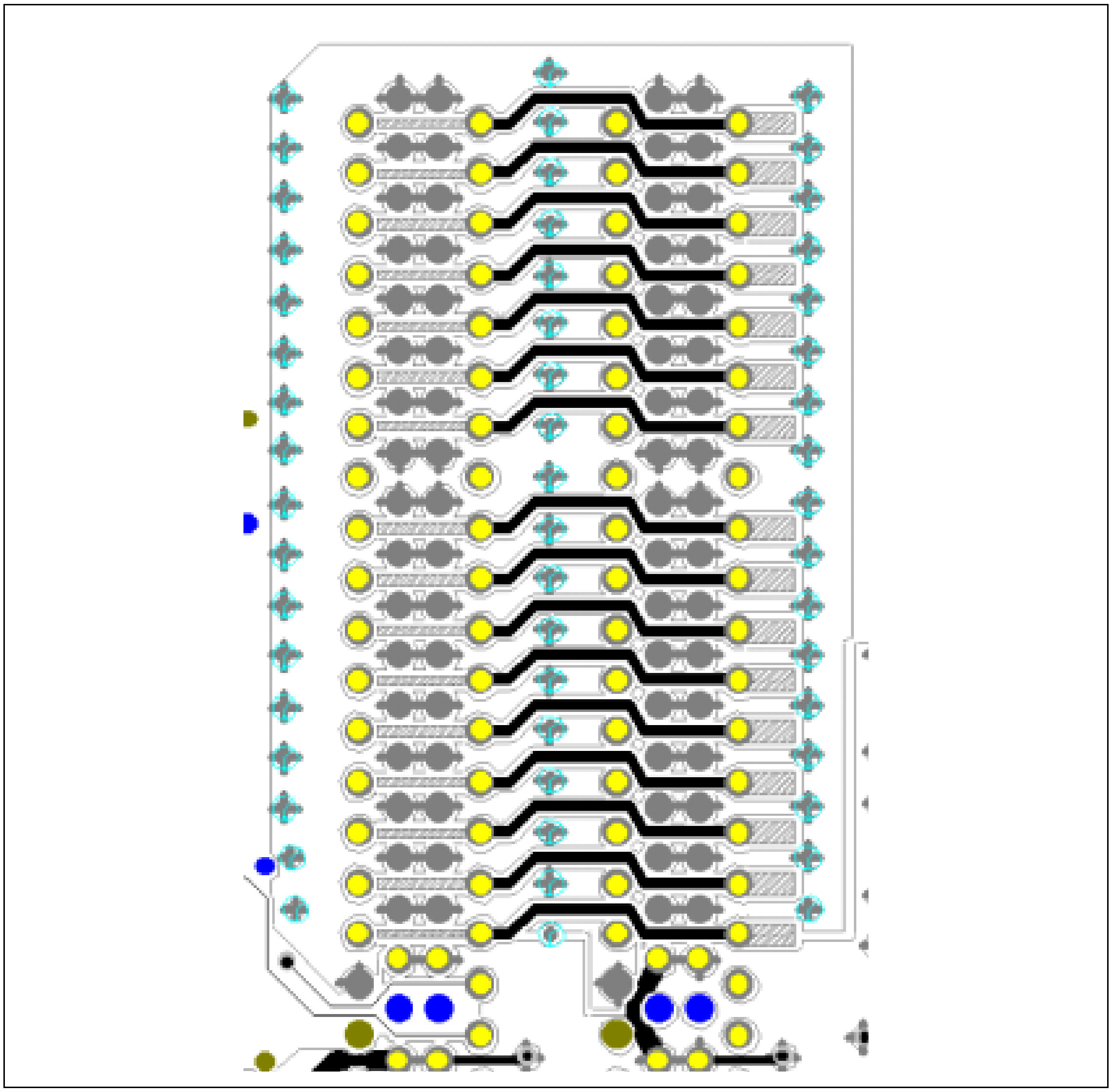


Figure 22. Section A (See Note), Top Layer



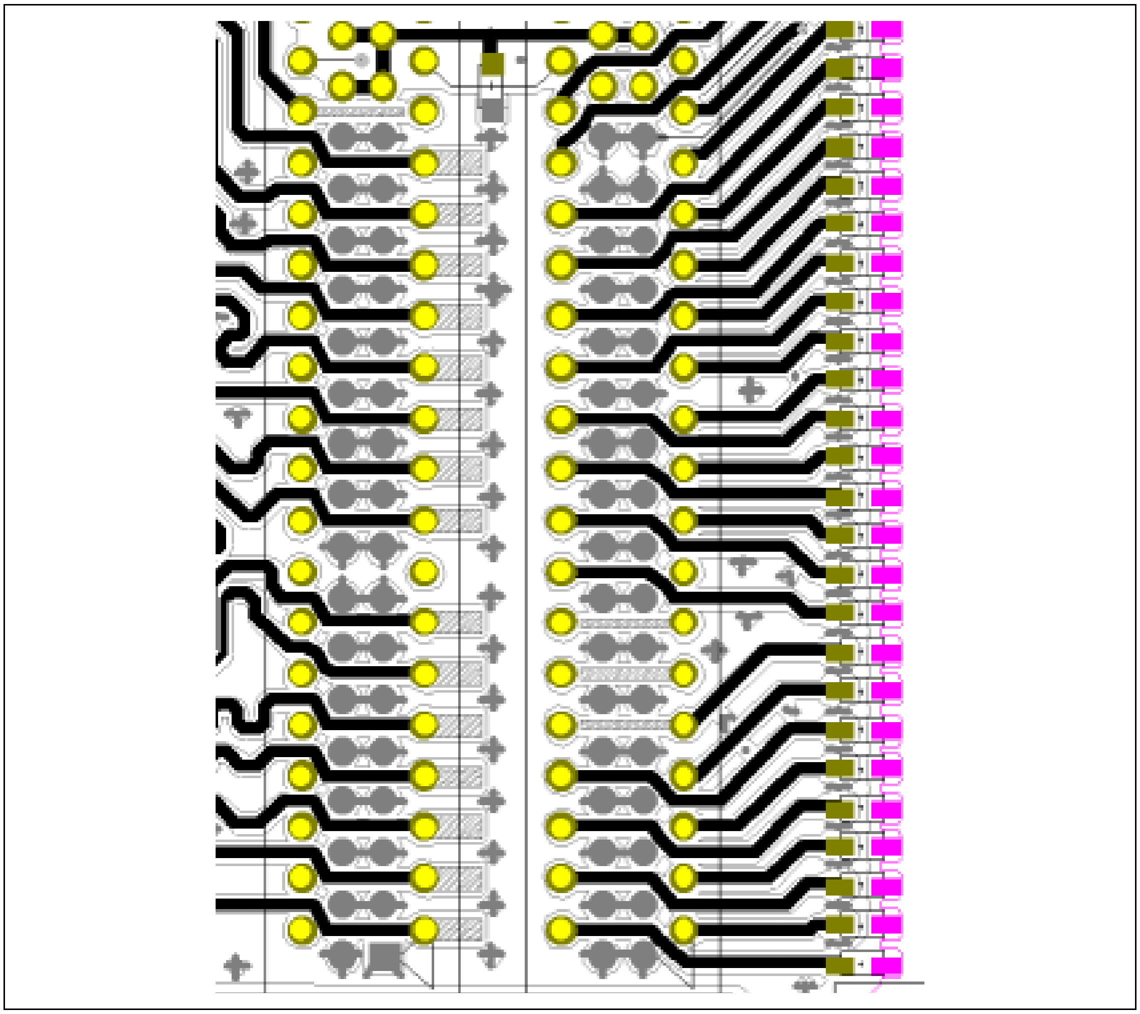
Note: Refer to Figure 21. For clarity, the ground flood was removed from the picture.

Figure 23. Section A (See Note), Bottom Layer



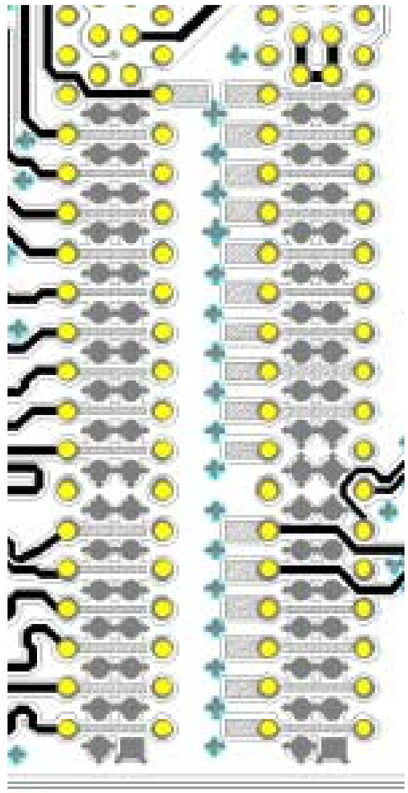
Note: Refer to Figure 21. For clarity, the ground flood was removed from the picture.

Figure 24. Section B (See Note), Top Layer



Note: Refer to Figure 21. For clarity, the ground flood was removed from the picture.

Figure 25. Section B (See Note), Bottom Layer



Note: Refer to Figure 21. For clarity, the ground flood was removed from the picture.

2.7.2.4.1. Direct RDRAM* Channel Connector Compensation Enhancement Recommendation

From further analysis, it was determined that the amount of capacitance needed for RSL traces depends on the lengths that the signals have to travel though the RIMM connector pin. (i.e., a signal on the bottom layer has to travel through more of the RIMM connector pin than a signal on the top layer). As a result of the travel through the pin, signals routed on the bottom layer have a larger inductance at the connector, which causes a larger impedance discontinuity, resulting in a possible reduction of voltage and timing margin on those signals. As a result, RSL traces on the bottom layer need more capacitive compensation than RSL traces routed on the top layer. RSL signals routed on the bottom layer need 0.55 pF more compensation than signals routed on the top layer. To compensate for the inductance of the connector, approximately 0.65 pF to 0.85 pF compensating capacitive tabs (C-TAB) are required for each topside RSL trace, and approximately 1.20 pF – 1.4 pF is required for each bottom-side RSL trace.

Table 5. RSL and Clocking Signal RIMM Connector Capacitance Recommendations

RSL and Clocking Signal Routing Layer	Capacitance (pF)
Top	0.65 – 0.85
Bottom	1.20 – 1.40

The copper tab area for the recommended stack-up was determined by means of simulation. The amount of capacitance required is determined by the layer on which the RSL or clocking signal is routed. The copper tabs can be placed on any signal layer, independently of the layer on which the RSL signal is routed.

The following example calculation uses Equation 1. Approximate Copper Tab Area Calculation for a board with an ε_r of 4.2 and a prepreg thickness of 4.5 mils. Note that these numbers vary with the difference in prepreg thickness.

Table 6. Copper Tab Area Calculation

Layer	Dielectric Thickness	Separation Between Signal Traces & Copper Tab	Min. Ground Flood	Air Gap between Signal & GND Flood	Compensating Capacitance in Cplate (pF)	CTAB Area (sq. mils)
Top	4.5	6	10	6	0.65 – 0.85	~2810 – 3680
Bottom	4.5	6	10	6	1.20 – 1.40	~5194 – 6060

Note that more than one copper tab shape may be used, as shown in Figure 26. The dimensions are based on the copper area over the ground plane. The actual length and width of the tabs may differ due to routing constraints (e.g., if tab must extend to center of hole or anti-pad). Figures 26 through 28 show a tab compensation capacitor routing example. Note that the capacitor tabs must not interrupt ground floods around the RIMM pins, and they must be connected, to avoid discontinuity in the ground plane, as shown.

Figure 26. Top-Layer CTAB with RSL Signal Routed on the Same Layer (C_{EFF} = 0.8 pF)

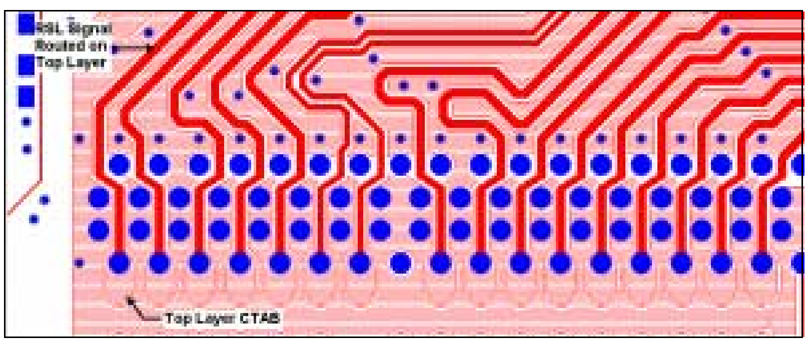
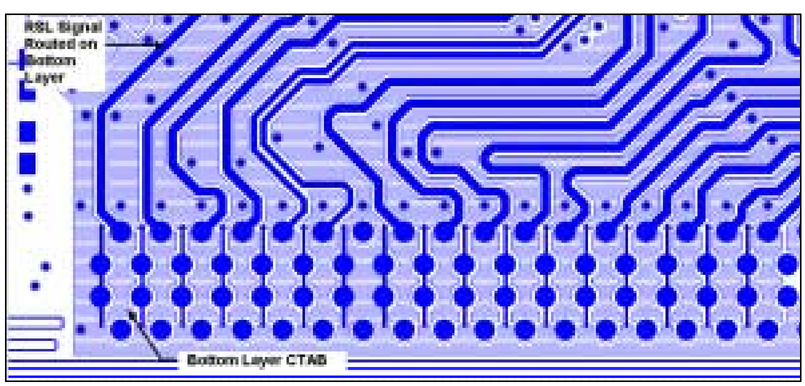
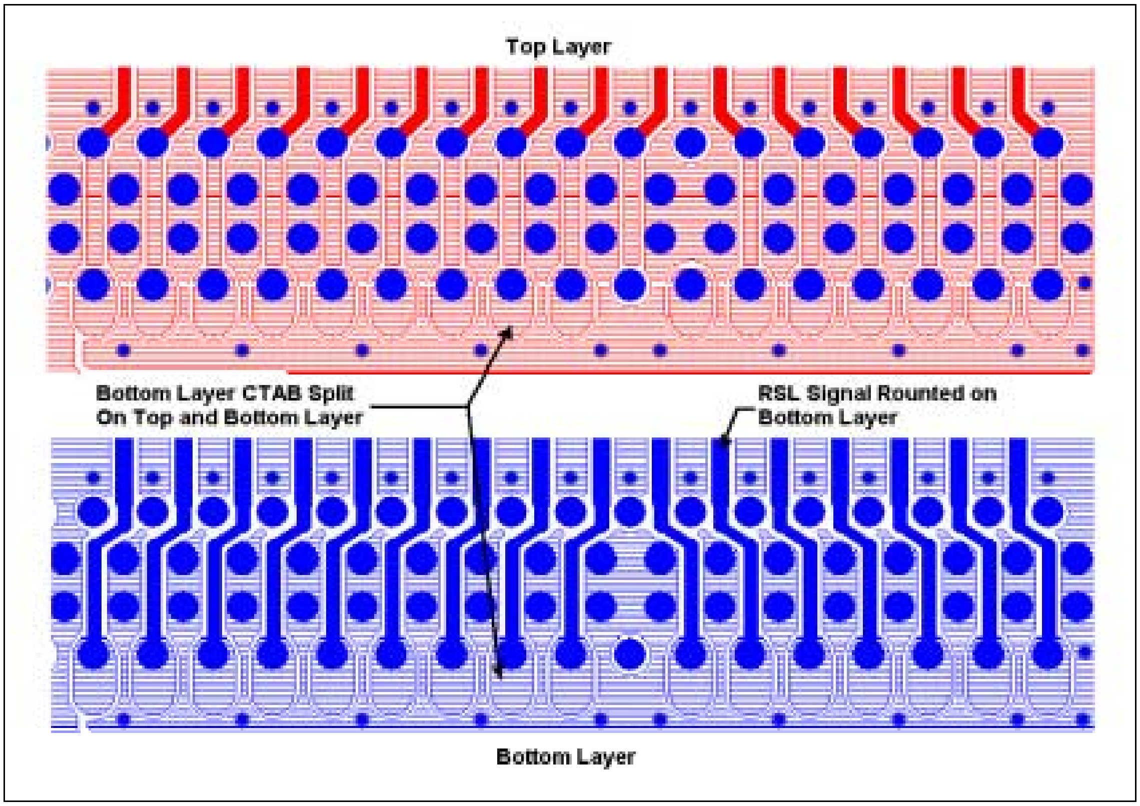


Figure 27. Bottom-Layer CTAB with RSL Signal Routed on the Same Layer (C_{EFF} = 1.35 pF)



The CTAB can be implemented on the multiple layers to minimize routing and space constraints. Figure 28 shows the use of CTABs on the top and bottom layer for bottom-layer RSL and clocking signals routed between RIMMs.

Figure 28. Bottom-Layer CTABs Split across the Top and Bottom Layer to Achieve an Effect C_{EFF} ~1.35 pF



2.7.2.5. RSL Signal Layer Alternation

RSL signals must alternate layers as they are routed through the channel. If a signal is routed on the primary layer from the MCH to the first RIMM socket, it must be routed on the secondary layer from the first RIMM to the second RIMM, as shown in Figure 29 (signal B). If a signal is routed on the secondary layer from the MCH to the first RIMM socket, it must be routed on the primary side from the first RIMM to the second RIMM, as shown in Figure 29 (signal A). Signals can be routed on either layer from the last RIMM to the termination resistors.

Figure 29. RSL Signal Layer Alternation

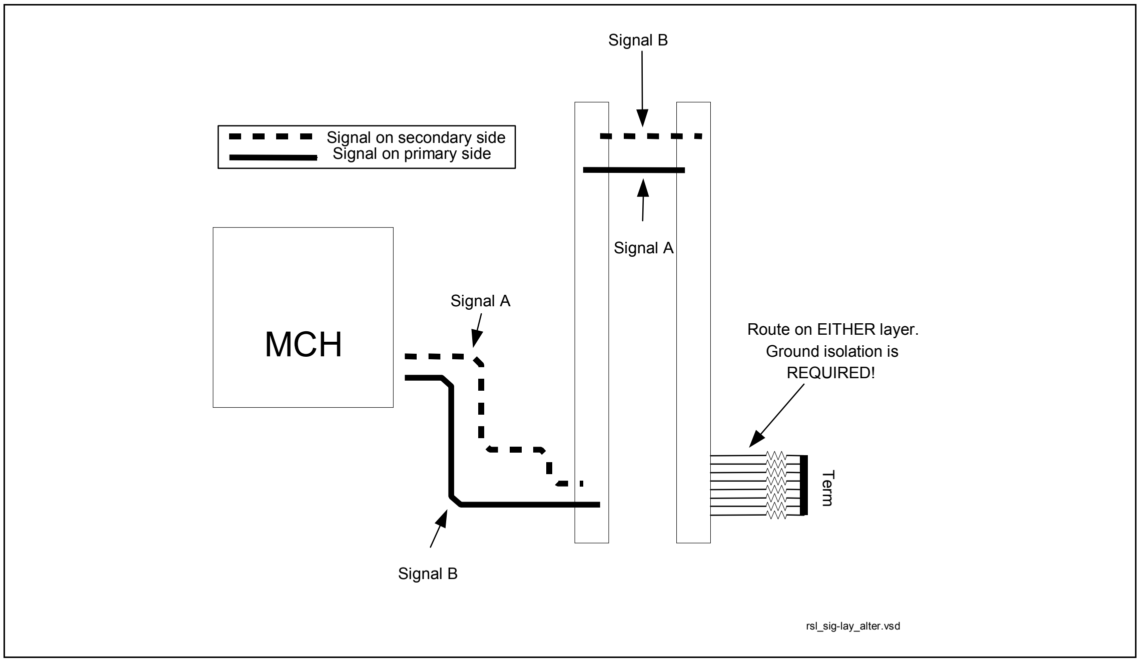


Table 7. RSL Routing Layer Requirements

	MCH to 1st RIMM	1st RIMM to 2nd RIMM
Method 1	Primary side	Secondary side
Method 2	Secondary side	Primary side

2.7.2.6. Length Matching Methods

To allow for greater routing flexibility, the RSL signals require pad-to-pin length matching between the MCH and the first connector. If the trace lengths are matched between the balls of the MCH and the pin of the RIMM connector, the length mismatch between the pad (on the die) and the ball has not been taken into account. However, given the package dimension, which represents the length from the pad to the ball, the routing can compensate for this package mismatch. Therefore, the board length mismatch can be increased.

The RSL channel requires the matching of the trace lengths from pad to pin within ±10 mils.

Given the following definitions:

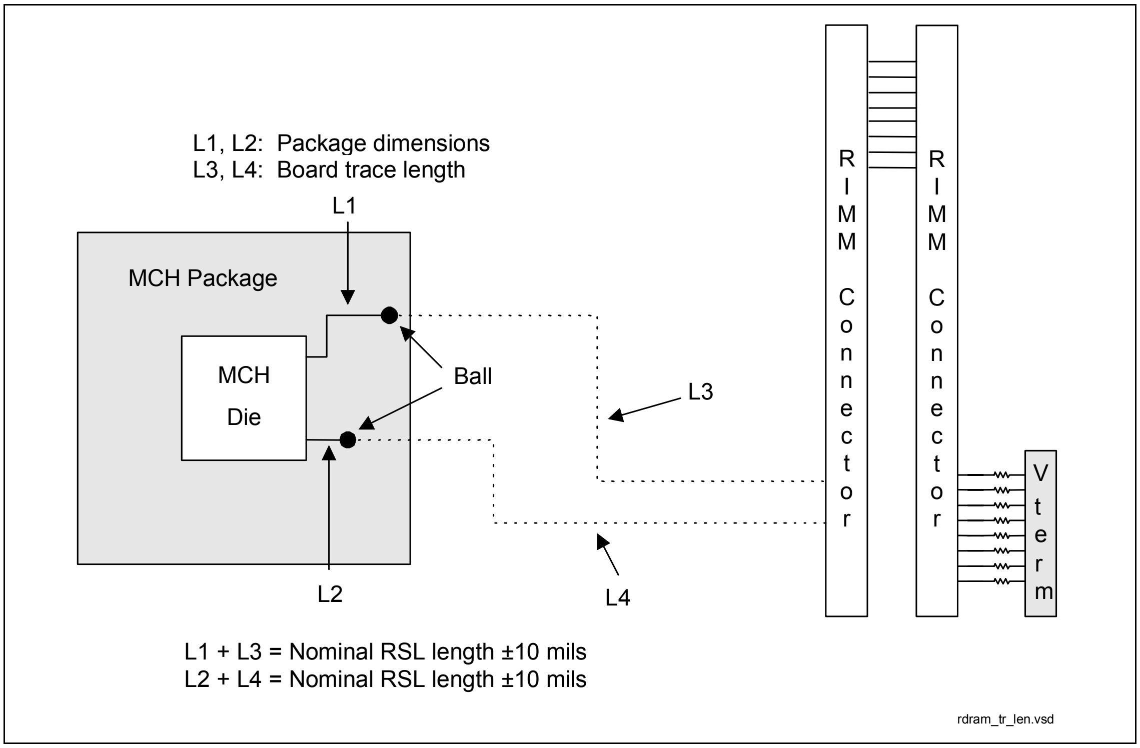
- Package dimension: Representation of length from pad to ball
- Board trace length: Trace length on board
- Nominal RSL length: Length to which all signals are matched. (Note: There is not necessarily a trace that is **exactly** to nominal length, but all RSL signals must be matched to within ±10 mils of the nominal length.) The nominal RSL length is an arbitrary length, within the limits of the routing guidelines, to which all the RSL signals will be matched (within 10 mils).

All RSL signals must satisfy the following equation:

Equation 2. RDRAM RSL Signal Trace Length Calculation

Package dimension + board trace length = Nominal RSL length ± 10 mils

Figure 30. Example of RDRAM Trace Length Matching



Note: Refer to the *Intel® 820 Chipset Family: 82820 Memory Controller Hub (MCH) Datasheet* for the component package dimensions.

The RDRAM clocks (CTM, CTM#, CFM, and CFM#) must be longer than the RDRAM signals, due to their increased trace velocity (because they are routed as a differential pair). To calculate the length for each clock, the following formula should be used:

Equation 3. RDRAM Clock Signal Trace Length Calculation

Clock length = Nominal RSL signal length (package + board) $\times$ 1.021

This formula yields clock signals 21 mils/inch longer than the nominal length. The lengthening of the clock signals to compensate for their trace velocity change *only* applies to routing between the MCH and the first RIMM. The clock signal lengths should be matched to the RSL signals between RIMMs. For more detailed clock routing guidelines, refer to *Chapter 4 Clocking*.

The high-speed CMOS signals must be length-matched to the RSL signals within 1200 mils (1.2 inches), as the result of a timing requirement between the CMOS and RSL signals during NAP Exit and PDN Exit.

It is necessary to compensate for the slight difference in electrical characteristics between a dummy via and a real via. Refer to the following section for more information on via compensation.

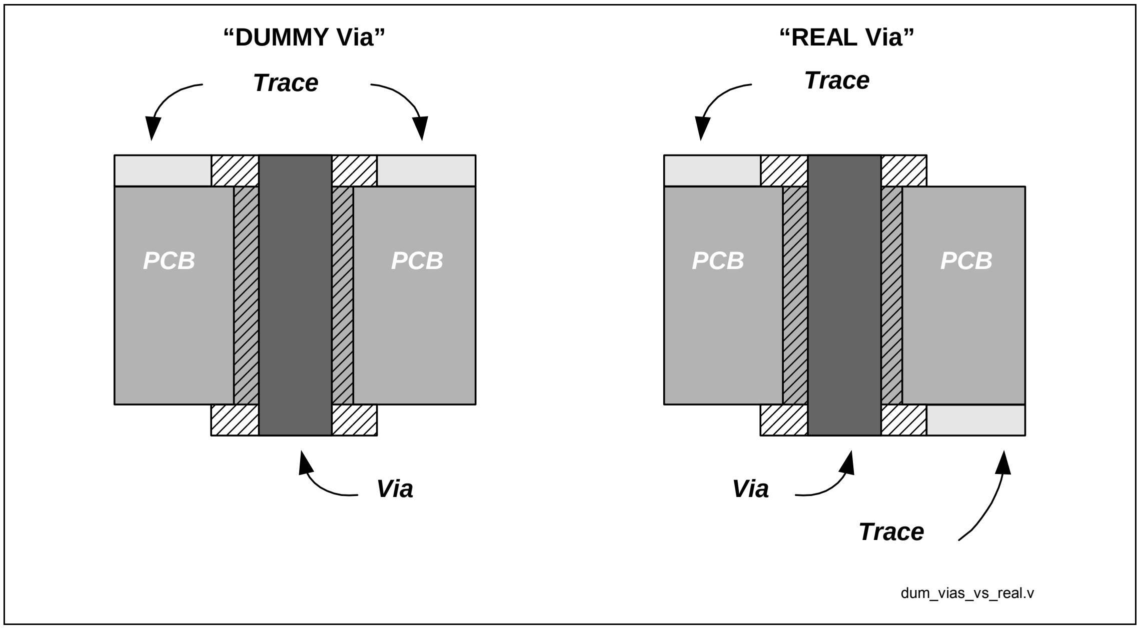
2.7.2.7. Via Compensation

As described in Section 2.7.2.1, all signals must have the same number of vias. As a result, each trace will have one via (near the BGA pad) because some RSL signals must be routed on the bottom of the motherboard. Therefore, it is necessary to place a dummy via on all signals that are routed on the top layer. Because the electrical characteristics of a dummy via do not exactly match the electrical characteristics of a real via, additional compensation must be performed for each signal that has a dummy via. Each signal with a dummy via must have 25 mils of additional trace length. That is:

Real via = Dummy via + 25 mils of trace length

This 25 mils of additional trace length must be added to each signal routed on the top layer after length matching, as documented in Section 2.7.2.6.

Figure 31. "Dummy" Via vs. "Real" Via



2.7.2.8. Length Matching and Via Compensation Example

Table 8 can be used to ensure that the RSL signals are the correct length.

Note: 2000 mils was chosen as an *example* nominal RSL length.

Table 8. Line Matching and Via Compensation Example[1,2,3,4,5,6,7,8,9,10]

Signal	Ball on MCH	Nominal RSL Length (mils)	Package Dimension (mils)	Motherboard Trace Length When Routed on Bottom (i.e., Real Via)		Motherboard Trace Length When Routed on Top (i.e., Dummy Via)		Recommended Routing
				Min. (mils)	Max. (mils)	Min. (mils)	Max. (mils)	
				Formula A		Formula B		
DQA0	A13	2000	138.14	1851.86	1871.86	1876.86	1896.86	Top
DQA1	C13	2000	19.11	1970.89	1990.89	1995.89	2015.89	Bottom
DQA2	A14	2000	163.16	1826.84	1846.84	1851.84	1871.84	Top
DQA3	C14	2000	39.87	1950.13	1970.13	1975.13	1995.13	Bottom
DQA4	B14	2000	97.54	1892.46	1912.46	1917.46	1937.46	Top
DQA5	C15	2000	62.67	1927.33	1947.33	1952.33	1972.33	Bottom
DQA6	A15	2000	186.11	1803.90	1823.90	1828.90	1848.90	Top
DQA7	C16	2000	95.70	1894.30	1914.30	1919.30	1939.30	Bottom
DQA8	A16	2000	230.20	1759.81	1779.81	1784.81	1804.81	Top
DQB0	C7	2000	39.56	1950.44	1970.44	1975.44	1995.44	Bottom
DQB1	B7	2000	95.83	1894.17	1914.17	1919.17	1939.17	Top
DQB2	C6	2000	63.49	1926.51	1946.51	1951.51	1971.51	Bottom
DQB3	A6	2000	153.69	1836.31	1856.31	1861.31	1881.31	Top
DQB4	C5	2000	97.33	1892.67	1912.67	1917.67	1937.67	Bottom
DQB5	A5	2000	191.43	1798.57	1818.57	1823.57	1843.57	Top
DQB6	B5	2000	152.47	1837.53	1857.53	1862.53	1882.53	Bottom
DQB7	A4	2000	237.71	1752.29	1772.29	1777.29	1797.29	Top
DQB8	C4	2000	138.29	1851.71	1871.71	1876.71	1896.71	Bottom
RQ0	A7	2000	179.49	1810.51	1830.51	1835.51	1855.51	Top
RQ1	C8	2000	27.12	1962.88	1982.88	1987.88	2007.88	Bottom
RQ2	A8	2000	162.21	1827.79	1847.79	1852.79	1872.79	Top
RQ3	C9	2000	5.80	1984.20	2004.20	2009.20	2029.20	Bottom
RQ4	B9	2000	71.70	1918.30	1938.30	1943.30	1963.30	Top
RQ5	A9	2000	133.88	1856.12	1876.12	1881.12	1901.12	Bottom
RQ6	A10	2000	122.20	1867.81	1887.81	1892.81	1912.81	Top
RQ7	C10	2000	0.00	1990.00	2010.00	2015.00	2035.00	Bottom
				FORMULA C		FORMULA D		
CFM	A12	2000	132.37	1906.85		1932.37		Bottom
CFM#	B12	2000	64.63	1976.02		2001.54		Bottom
CTM	B11	2000	56.06	1984.76		2010.29		Top
CTM#	A11	2000	126.34	1913.01		1938.53		Top

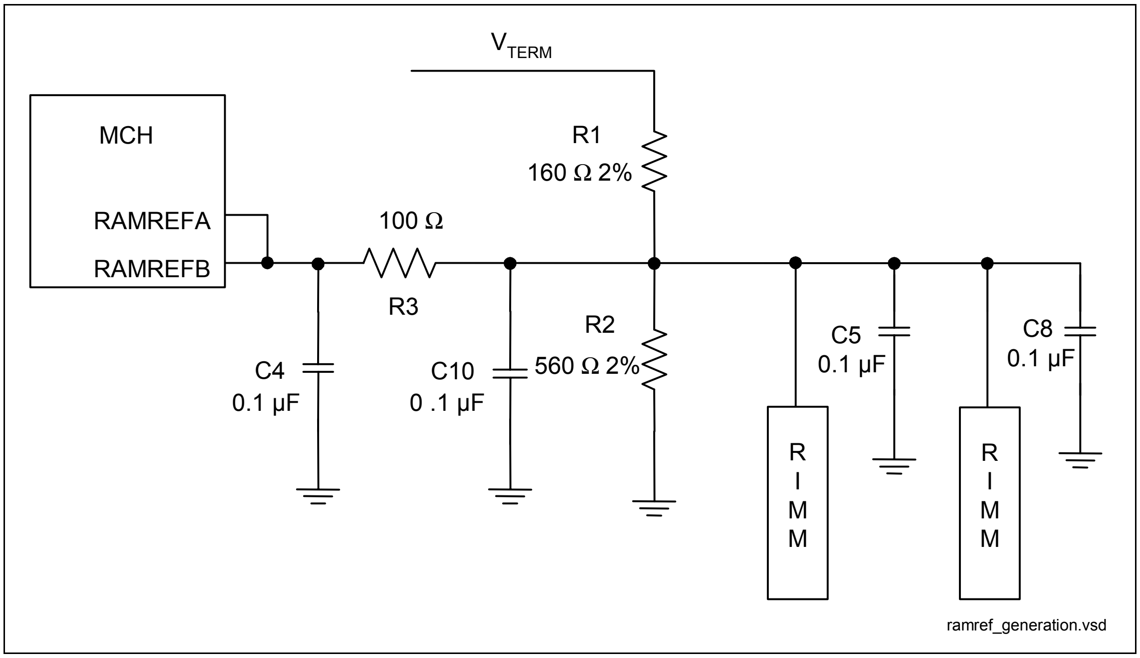
NOTES:

1. Signals connecting to side A of the RIMM connector (i.e., A1, A2, A3, etc.) should be routed on the top (primary side) of the motherboard.
2. Signals connecting to side B of the RIMM connector should be routed on the bottom (solder side).
3. These trace lengths apply **only** from the MCH to the first RIMM. All signals must match **exactly** from RIMM to RIMM.
4. Clock trace lengths include the 1.021 trace velocity factor.
5. Formula A min.: Motherboard trace = (Nominal RSL length – package dimension) – 10 mils
6. Formula A max.: Motherboard trace = (Nominal RSL length – package dimension) + 10 mils
7. Formula B min.: Motherboard trace = (Nominal RSL length – package dimension) – 10 mils + 25 mil
8. Formula B max.: Motherboard trace = (Nominal RSL length – package dimension) + 10 mils + 25 mils
9. Formula C: Motherboard trace = (Nominal RSL length – package dimension) × 1.021
10. Formula D: Motherboard trace = (Nominal RSL length – package dimension + 25 mils) × 1.021

2.7.3. Direct RDRAM* Reference Voltage

The Direct RDRAM reference voltage (RAMREF) must be generated as shown in Figure 32. The RAMREF should be generated from a typical resistor divider using 2%-tolerance resistors. Additionally, the RAMREF must be decoupled locally at **each** RIMM connector, at the resistor divider, and at the MCH. Finally, as shown in Figure 32, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with a 10 mil-wide trace.

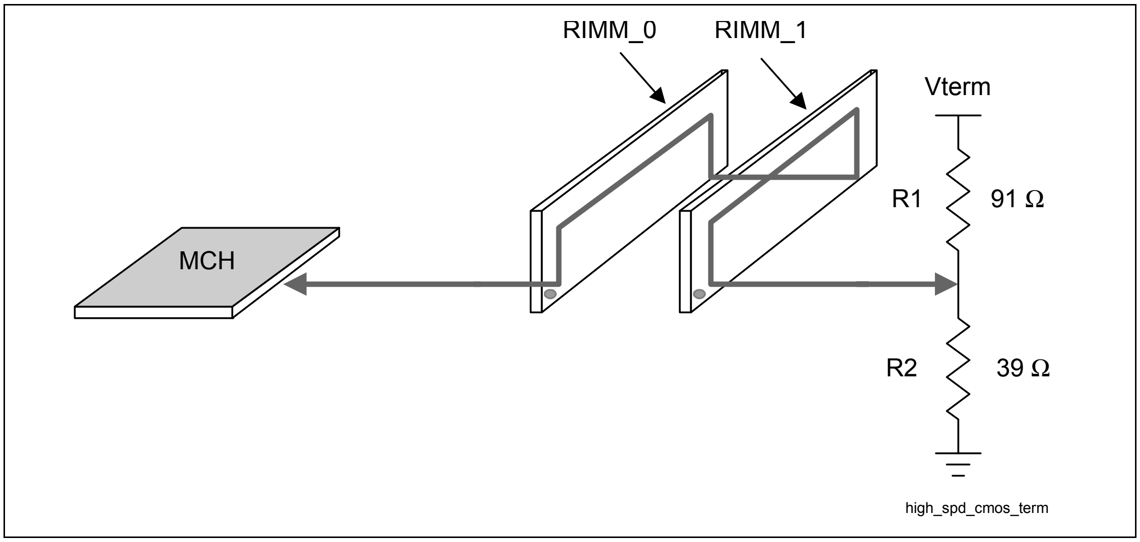
Figure 32. RAMREF Generation Example Circuit



2.7.4. High-Speed CMOS Routing

- The high-speed CMOS signals (CMD & SCK) must be routed using 28 Ω traces. Using the recommended stack-up, these signals will be 18 mils wide.
- The high-speed CMOS signals must be length-matched to the RSL signals within 1200 mils (1.2 inches), because of a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit.
- The high-speed CMOS signals require termination as shown in Figure 33, as a result of the buffer strengths in the MCH.
- The resistors must be 91 Ω pull-up and 39 Ω pull-down, and they must be 2% or better for S3 mode reliability. The trace impedances remain 28 Ω.

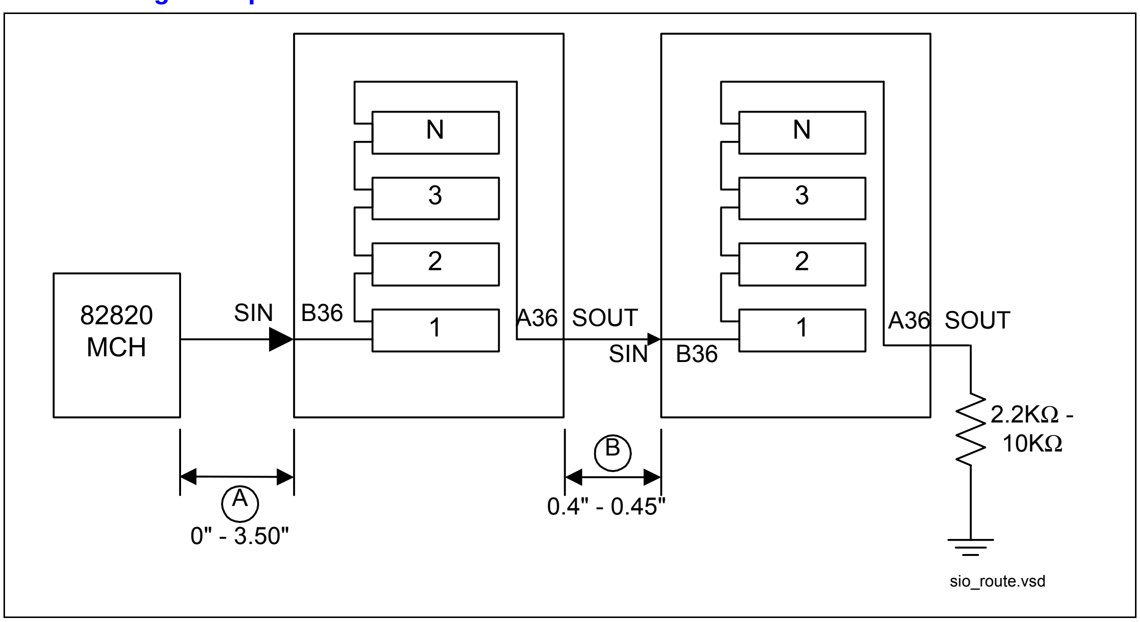
Figure 33. High-Speed CMOS Termination



2.7.4.1. SIO Routing

The SIO signal must be routed from RIMM to RIMM, as shown in Figure 34. The SIO signal requires a 2.2 kΩ to 10 kΩ terminating resistor on the SOUT pin of the last RIMM. SIO is routed with a standard 5 mil-wide, 60 Ω trace. The motherboard routing lengths for the SIO signal are the same as those for RSL signals. (See Figure 34.)

Figure 34. SIO Routing Example



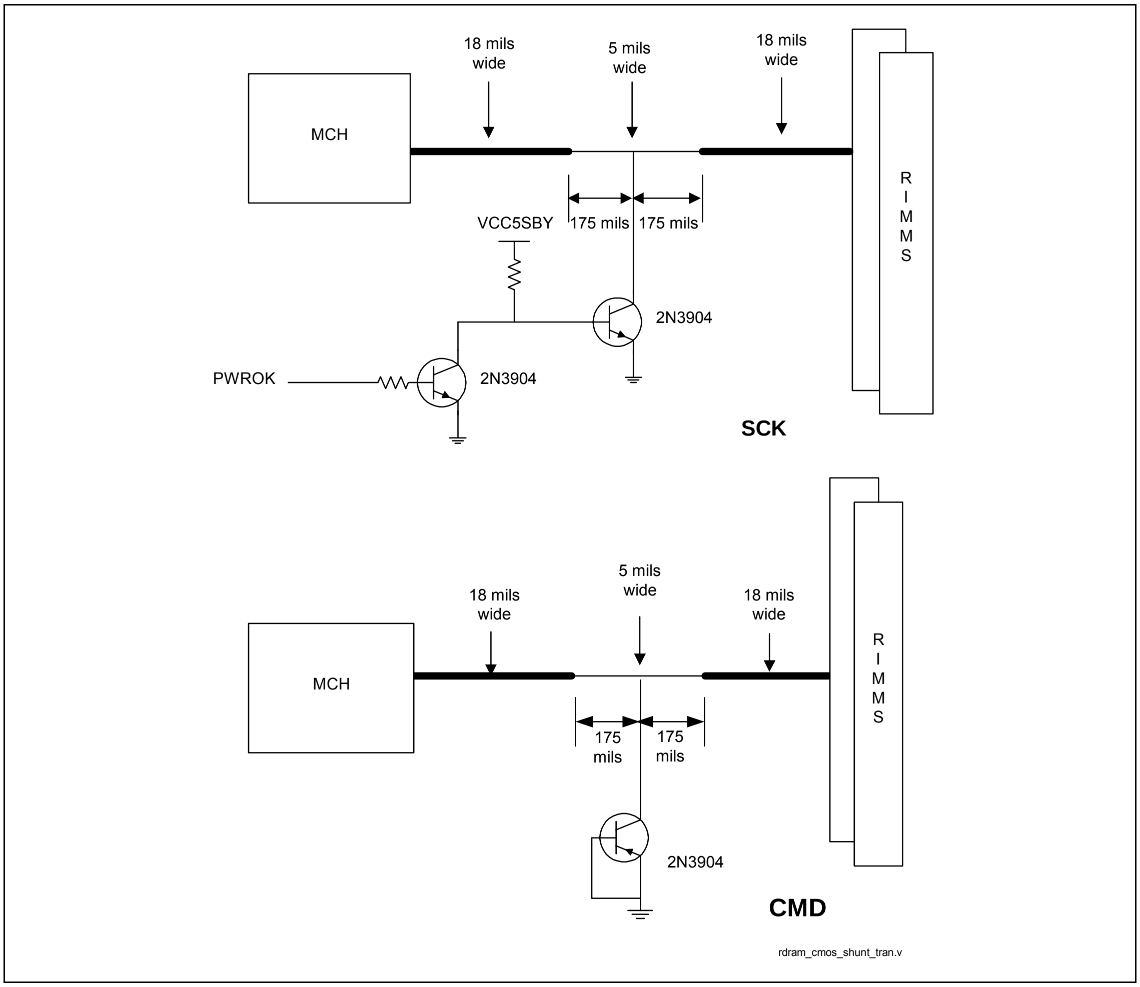
2.7.4.2. Suspend-to-RAM Shunt Transistor

When an Intel 820E chipset system enters or exits Suspend to RAM, power will be ramping to the MCH (i.e., it will be powering up or powering down). While power is ramping, the states of the MCH outputs are not guaranteed. Therefore, the MCH could drive the CMOS signals and issue CMOS commands. One of the commands—the only one the RDRAMs will respond to—is the power-down exit command. To avoid the MCH inadvertently taking the RDRAMs out of power-down because the CMOS interface is driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the MCH is entering and exiting Suspend to RAM. This shunting can be accomplished using the NPN transistor shown in the circuit in Figure 35. The transistor should have a C_{OBO} of 4 pF or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signal, the CMD signal needs a dummy transistor. This transistor's base should be tied to ground (i.e., always turned off).

To minimize impedance discontinuities, the traces for CMD and SCK must have a neckdown from 18 mil traces to 5 mil traces, for 175 mils on either side of the SCK/CMD attach point, as shown in Figure 35.

Figure 35. RDRAM CMOS Shunt Transistor



2.7.5. Direct RDRAM* Clock Routing

Refer to *Chapter 4 Clocking* for the Intel 820E chipset platform's Direct RDRAM clock routing guidelines.

2.7.6. Direct RDRAM* Design Checklist

Use the following checklist as a final check to ensure that the motherboard incorporates solid design practices. This list is only a reference. For correct operation, all of the design guidelines within this document must be followed.

Table 9. Signal List

RSL Signals	High-Speed CMOS Signals	Serial CMOS Signal	Clocks
• DQA[8:0] • DQB[8:0] • RQ[7:0]	• CMD • SCK	• SIO	• CTM • CTM# • CFM • CFM#

- Ground isolation well grounded.
  - Via to ground every 0.5 inch around edge of isolation island
  - Via to ground every 0.5 inch between RIMMs
  - Via to ground every 0.5 inch between signals (from MCH to first RIMM)
  - Via between every signal within 100 mils of the MCH edge and the connector edge
  - No unconnected ground floods
  - All ground isolation at least 10 mils wide.
  - Ground isolation fills between serpentines
  - Ground isolation not broken by C-TABs.
  - Ground isolation connects to the ground pins in the middle of the RIMM connectors.
  - Ground isolation vias connect on all 4 layers and should **not** have thermal reliefs.
  - Ground pins in RIMM connector connect on all 4 layers.

- V_{TERM} layout yields low noise.
  - Solid V_{TERM} island is on top layer. Do not split this plane.
  - Ground island (for ground side of V_{TERM} caps) is on top.
  - Termination resistors connect **directly** to the V_{TERM} island on the top layer (without vias).
  - Decoupling V_{TERM} is **critical!**
  - Decoupling capacitors connect directly to top-layer V_{TERM} island and top-layer ground island. (See the layout example.)
  - Use **at least** 2 vias per decoupling capacitor in the top-layer ground island.
  - Use 2 × 100 µF tantalum capacitors to decouple V_{TERM}. (Aluminum/electrolytic capacitors are too slow!)
  - High-frequency decoupling capacitors **must** be spread out across the termination island so that all termination resistors are near high-frequency capacitors.
  - 100 µF tantalum capacitors should be at each end of the V_{TERM} island.
  - 100 µF tantalum capacitors must be connected directly to V_{TERM} island.
  - 100 µF tantalum capacitors must have at least 2 vias/cap to ground.
  - V_{TERM} island should be 50–75 mils wide.
  - V_{TERM} island should not be broken.

- If any RSL signals are routed, even for a short distance, out of the last RIMM (towards termination) on the bottom side, ensure that the ground reference plane (on the third layer) is continuous under the termination resistors/capacitors.
- Ensure that the current path for power delivery to the MCH does not go through the V_{TERM} island.

• CTM/CTM# routed properly
  - CTM/CTM# are routed differentially from DRCG to last RIMM.
  - CTM/CTM# are ground-isolated from DRCG to last RIMM.
  - CTM/CTM# are ground-referenced from DRCG to last RIMM.
  - Vias are placed in ground isolation and ground reference every 0.5 inch.
  - When CTM/CTM# serpentine together, they MUST maintain **exactly** 6 mils of spacing.

• Clean DRCG power supply
  - The 3.3 V DRCG power flood on the top layer should connect to each high-frequency (0.1 µF) capacitor, to the 10 µF bulk tantalum capacitor, and to the ferrite bead.
  - High-frequency (0.1 µF) capacitors are near the DRCG power pins, with one capacitor next to each power pin.
  - 10 µF bulk tantalum capacitor near DRCG connected directly to the 3.3 V DRCG power flood on the top layer
  - The ferrite bead isolating the DRCG power flood from the 3.3 V main power also connects directly to the 3.3 V DRCG power flood on the top layer.
  - Use 2 vias on the ground side of each.

• Good DRCG output network layout
  - Series resistors (39 Ω) should be *very* near CTM/CTM# pins.
  - Parallel resistors (51 Ω) should be very near series resistors.
  - CTM/CTM# should be 18 mils wide, from the CTM/CTM# pins to the resistors.
  - CTM/CTM# should be 14-on-6 routed differentially as close as possible after the resistor network.
  - When not 14 on 6, the clocks should be 18 mils wide.
  - Ensure that CTM/CTM# are ground-referenced and the ground reference is connected to the ground plane every 0.5 inch to 1 inch.
  - Ensure that CTM/CTM# are ground-isolated and the ground isolation is connected to the ground plane every 0.5 inch to 1 inch.
  - Ensure that 15 pF EMI capacitors to ground are removed. (The pads are not necessary, and removing the pads provides more space for better placement of other components.)
  - Ensure the that 4 pF-EMI capacitor is implemented (but do not assemble the capacitor).

• Good RSL transmission lines
  - RSL traces are 18 mils wide.
  - When RSL traces neck down to exit the MCH BGA, the minimum width is 15 mils and the neckdown is no longer than 25 mils in length.
  - RSL traces do **not** neck down when routing into the RIMM connector.
  - If tight serpentining is necessary, 10 mil ground isolation **must** be between serpentine segments. (i.e., an RSL signal **cannot** serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines.)
  - RSL traces do not cross power plane splits. RSL signals also **must not** be routed next to a power plane split. (For example, the RSL signals on the 4th layer cannot be routed directly below the ground isolation split on the 3rd layer.)
  - At all times, uniform ground isolation flood is exactly 6 mils from the RSL signals.
  - ALL RSL, CMD/SCK, and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin.

- All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the last RIMM to the termination. If signals are routed on the bottom from the last RIMM to the termination, the ground reference plane on the 3rd layer **must** extend under these signals **and** include the ground side of the V_{TERM} decoupling capacitors.
- CTABs must not cross (or be on top of) power plane splits. They must be **entirely** referenced to ground.
- At least 10 mils of ground flood isolation is required around **all** RSL signals. (Ground isolation must be exactly 6 mils from RSL signals.) Ground flood is recommended for isolation. This ground flood should be as close as possible to the MCH (and the first RIMM). If possible, connect the flood to the ground balls/pins on the MCH/connector.

* Clean V_{REF} routing
  - Ensure a 1 × 0.1 µF capacitor on V_{REF} at each connector.
  - Use a 10 mil-wide trace (6 mils minimum).
  - Do not route V_{REF} near high-speed signals.
* RSL routing
  - All signals must be length-matched within ±10 mils of the nominal RSL length. (Note: Use the table in the *Intel® 820 Chipset Family: 82820 Memory Controller Hub (MCH) Datasheet* to verify the trace lengths.) Ensure that signals with a dummy via are compensated correctly.
  - ALL RSL signals must have one via near the MCH BGA pad. Signals routed on the secondary side of the MB will have a “real via,” while signals routed on the primary side will have a “dummy via.” Additionally, all signals with a dummy via must have an additional trace length of 25 mils.
  - B-side RIMM connector signals are routed on the secondary side of the motherboard. A-side RIMM connector signals are routed on the primary side of the motherboard.
  - Signals must “alternate” layers, as shown in the following table:

If Signal Routed from MCH to 1st RIMM on:	Then Route Signal from 1st RIMM to Next RIMM on:
Primary side	Secondary side
Secondary side	Primary side

* Clock routing
  - Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation) when they are routed as a differential pair. For very short sections under the MCH and under the first RIMM, it will not be possible to route as a differential pair. In these sections, the clocks signals **must** neck up to 18 mils and be ground-isolated with at least 10 mils ground isolation.
  - Clock signals must be length-compensated (using the 1.021 length factor mentioned in *Section 2.8.3 2×/4× Timing Domain Routing Guidelines*, 2×/4× Timing Domain Routing Guidelines). Ensure that each clock pair is length-matched within ±2 mils.
  - When clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).
  - 22 mil ground isolation is required on each side of the differential pair.

2.8. AGP 2.0

For detailed AGP interface functionality (e.g., protocols, rules, signaling mechanisms), refer to Revision 2.0 of the latest *AGP Interface Specification* obtainable from http://www.agpforum.org. This document focuses only on specific Intel 820E chipset platform recommendations.

Revision 2.0 of the *AGP Interface Specification* enhances the functionality of the original *AGP Interface Specification* (Rev. 1.0) by allowing 4× data transfers (4 data samples per clock) and 1.5 V operation. In addition to these major enhancements, additional performance enhancement and clarifications (e.g., *fast-write* capability) are included in the *AGP Interface Specification* (Rev. 2.0). The Intel 820E chipset supports the enhanced features of AGP 2.0.

The 4× operation of the AGP interface provides for “quad-pumping” of the AGP AD (address/data) and SBA (side-band addressing) buses. That is, data is sampled four times during each 66 MHz AGP clock. This means that each data cycle is ¼ of a 15-ns (66 MHz) clock, or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2× operation, data is sampled twice during a 66 MHz clock cycle. Therefore, the data cycle time is 7.5 ns.

To allow for these high-speed data transfers, the 2× mode of AGP operation uses source-synchronous data strobing. (Refer to *Source-Synchronous Strobing* section.) During 4× operation, the AGP interface uses differential source-synchronous strobing.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, the propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines will cause the settling time to be long. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5 V) requires even more noise immunity. For example, during 1.5 V operation, V_{ILMAX} is 570 mV. Without proper isolation, crosstalk could create signal integrity issues.

2.8.1. AGP Interface Signal Groups

The signals on the AGP interface are broken into three groups: 1× timing domain signals, 2×/4× timing domain signals, and miscellaneous signals. Each group has different routing requirements. In addition, within the 2×/4× timing domain signals, there are three sets of signals. All signals in the 2×/4× timing domains must meet minimum and maximum trace length requirements as well as trace width and spacing requirements. However, trace length matching requirements only must be met within each set of 2×/4× timing domain signals.

Signal Groups

- 1× timing domain
  - CLK (3.3 V)
  - RBF#
  - WBF#
  - ST[2:0]
  - PIPE#
  - REQ#
  - GNT#
  - PAR
  - FRAME#
  - IRDY#
  - TRDY#
  - STOP#
  - DEVSEL#
- 2×/4× timing domains

  Set 1
  - AD[15:0]
  - C/BE[1:0]#
  - AD_STB0
  - AD_STB0# (used in 4× mode *only*)

  Set 2
  - AD[31:16]
  - C/BE[3:2]#
  - AD_STB1
  - AD_STB1# (used in 4× mode *only*)

  Set 3
  - SBA[7:0]
  - SB_STB
  - SB_STB# (used in 4× mode *only*)
- Miscellaneous, async
  - USB+
  - USB-
  - OVRCNT#
  - PME#
  - TYPDET#
  - PERR#
  - SERR#
  - INTA#
  - INTB#

Table 10. AGP 2.0 Data/Strobe Associations

Data	Associated Strobe in 1×	Associated Strobe in 2×	Associated Strobes in 4×
AD[15:0] and C/BE[1:0]#	Strobes are not used in 1× mode. All data is sampled on rising clock edges.	AD_STB0	AD_STB0, AD_STB0#
AD[31:16] and C/BE[3:2]#	Strobes are not used in 1× mode. All data is sampled on rising clock edges.	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	Strobes are not used in 1× mode. All data is sampled on rising clock edges.	SB_STB	SB_STB, SB_STB#

Throughout this chapter, the term "data" refers to AD[31:0], C/BE[3:0]#, and SBA[7:0]. The term "strobe" refers to AD_STB[1:0], AD_STB#[1:0], SB_STB, and SB_STB#. When the term data is used, it refers to one of the three sets of data signals. When the term strobe is used, it refers to one of the strobes as it relates to the data in its associated group.

The routing guidelines for each group of signals (1× timing domain signals, 2×/4× timing domain signals, and miscellaneous signals) will be discussed separately.

2.8.2. 1× Timing Domain Routing Guidelines

- The AGP 1× timing domain signals have a maximum trace length of 7.5 inches. (Refer to signal groups listed previously.) This maximum applies to **all** signals listed as 1× timing domain signals in the Signal Groups section.
- AGP 1× timing domain signals can be routed with 5 mil minimum trace separation.
- There are no trace length matching requirements for 1× timing domain signals.

2.8.3. 2×/4× Timing Domain Routing Guidelines

These trace length guidelines apply to **all** signals listed as 2×/4× timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

The maximum line length and length mismatch requirements depend on the routing rules used on the motherboard. These routing rules were created to allow design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 inches) and long AGP interfaces (e.g., > 6 inches and < 7.25 inches) are documented separately. The maximum allowable length of the AGP interface is 7.25 inches.

Interfaces < 6 Inches

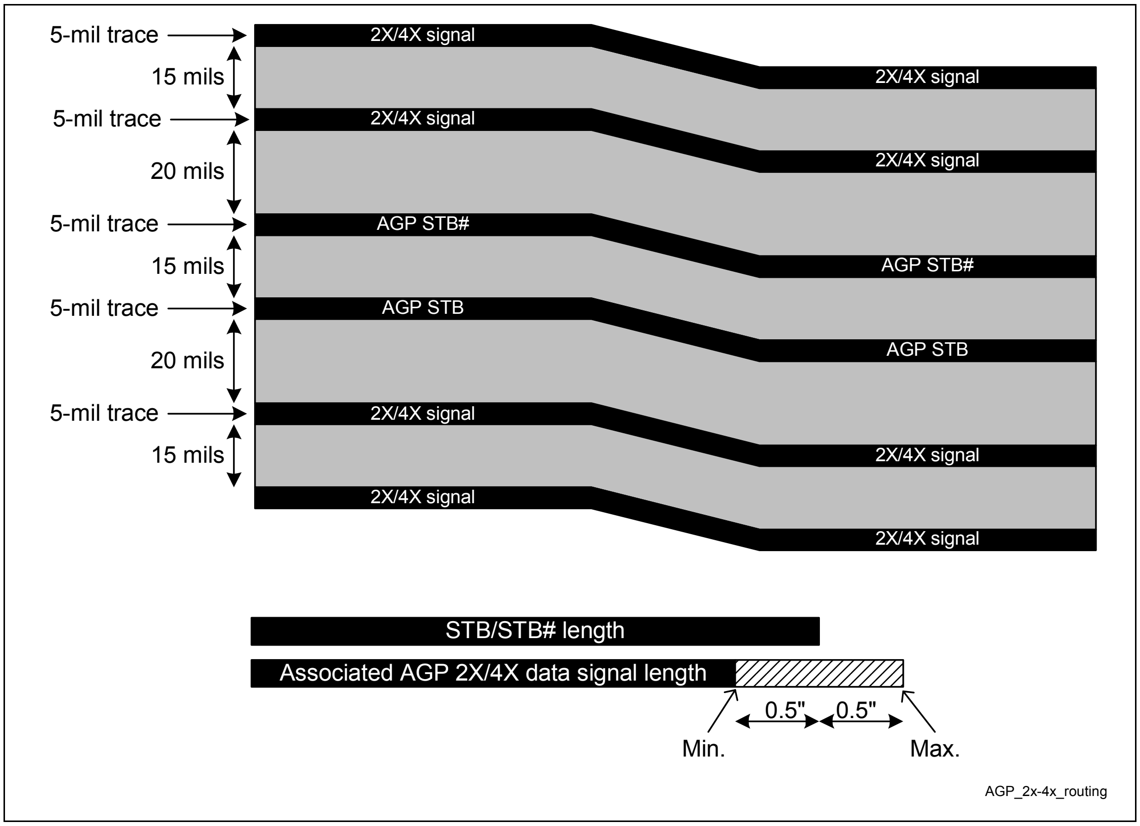
If the AGP interface is less than 6 inches, a minimum 1:3 trace spacing is required for 2×/4× lines (data and strobes). These 2×/4× signals must be matched to their associated strobe, within ±0.5 inch. These guidelines are for designs that require less than 6 inches between the AGP connector and the MCH.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 4.8 inches to

5.8 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) can be 3.7 inches to 4.7 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together. (For example, AD_STB0 and AD_STB0# should be routed next to each other.) The two strobes in a strobe pair should be routed on 5 mil traces, with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1 inch. (That is, a strobe and its complement must be the same length, within 0.1 inch.)

Figure 36. AGP 2×/4× Routing Example for Interfaces < 6 Inches



Interfaces > 6 Inches and < 7.25 Inches

Longer lines have more crosstalk. Therefore, to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.25 inches, 1:4 routing is required for all data lines and strobes. For these designs, the line length mismatch must be less than ±0.125 inch within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5 inches long, the data signals associated with those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2 inches long, and the data signals associated with those strobe signals (e.g., SBA[7:0]) can be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, and SB_STB#) act as clocks on the source-synchronous AGP interface. Therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together. (For example, AD_STB0 and AD_STB0# should be routed next to each other.) The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length-matched to less than ±0.1 inch. (i.e., a strobe and its complement must be the same length, within 0.1 inch.)

All AGP Interfaces

The 2×/4× timing domain signals can be routed with 5 mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3 inch of the MCH package.

When matching the trace length for the AGP 4× interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

Reduce line length mismatch to ensure added margin. To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements **must** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible, to provide timing margin.

2.8.4. AGP 2.0 Routing Summary

Table 11. AGP 2.0 Routing Summary[1,2]

Signal	Maximum Length (inches)	Trace Spacing (5 mil Traces)	Length Mismatch (inches)	Relative To	Notes
1× Timing Domain	7.5	5 mils	No requirement	N/A	None
2×/4× Timing Domain Set 1	7.25	20 mils	±0.125	AD_STB0 and AD_STB0#	AD_STB0 and AD_STB0# must be the same length.
2×/4× Timing Domain Set 2	7.25	20 mils	±0.125	AD_STB1 and AD_STB1#	AD_STB1 and AD_STB1# must be the same length.
2×/4× Timing Domain Set 3	7.25	20 mils	±0.125	SB_STB and SB_STB#	SB_STB and SB_STB# must be the same length.
2×/4× Timing Domain Set 1	6	15 mils[1]	±0.5	AD_STB0 and AD_STB0#	AD_STB0 and AD_STB0# must be the same length.
2×/4× Timing Domain Set 2	6	15 mils[1]	±0.5	AD_STB1 and AD_STB1#	AD_STB1 and AD_STB1# must be the same length.
2×/4× Timing Domain Set 3	6	15 mils[1]	±0.5	SB_STB and SB_STB#	SB_STB and SB_STB# must be the same length.

NOTES:

1. Each strobe pair must be separated from other signals by at least 20 mils.
2. These guidelines apply to board stack-ups with 10% impedance tolerance.

2.8.5. AGP Clock Routing

The maximum total AGP clock skew (between the MCH and the graphics component) is 1 ns for all data transfer modes. This 1 ns includes skew and jitter that originates on the motherboard, add-in card, and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage, but at all points on the clock edge that fall within the switching range. The 1-ns skew budget is divided such that the motherboard is allotted 0.9 ns of clock skew. (The motherboard designer determines how the 0.9 ns are allocated between the board and the synthesizer.) For the Intel 820E chipset platform's AGP clock routing guidelines, refer to *Chapter 4 Clocking*.

2.8.6. General AGP Routing Guidelines

The following routing guidelines are recommended for the optimal system design. The main focus of these guidelines is the minimization of signal integrity problems on the AGP interface of the Intel 820E chipset's MCH. The following guidelines are not intended to replace thorough system validation on Intel 820E chipset-based products.

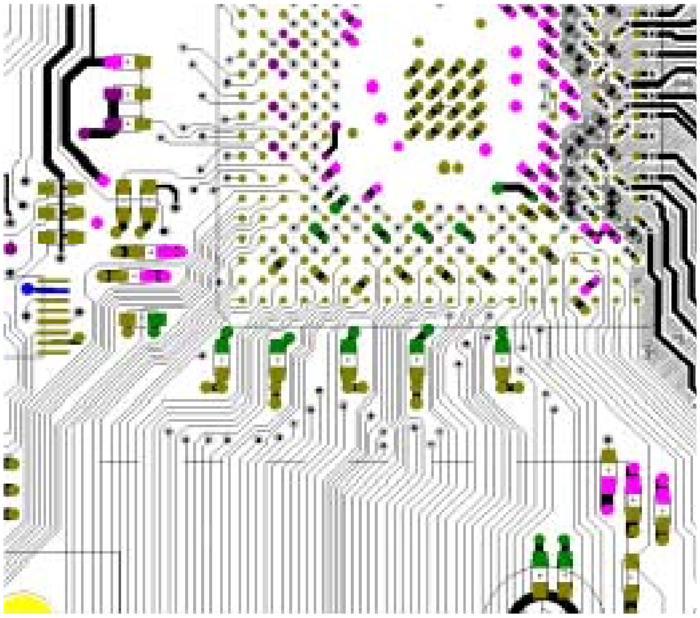
2.8.6.1. Recommendations

Decoupling

- For V_{DDQ} decoupling, at least six 0.01-µF capacitors are required, of which at least four must be within 70 mils of the outer row of balls on the MCH. (See Figure 37.)
- Evenly distribute the placement of decoupling capacitors in the AGP interface signal field.
- Use a low-ESL ceramic capacitor (e.g., 0603 body type, X7R dielectric).
- In addition to the minimum decoupling capacitors, bypass capacitors should be placed at vias that transition AGP signals from one reference signal plane to another. In a typical four-layer PCB design, the signals transition from one side of the board to the other.
- One extra 0.01-µF capacitor is required per 10 vias. The capacitor should be placed as close as possible to the center of the via field.
- Ensure that the AGP connector is well decoupled, as described in the *AGP Design Guide*, Revision 1.0 (Section 1.5.3.3).

Note: To add the decoupling capacitors as close as possible to the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of the space between traces should be minimal and for as short a distance as possible (1 inch max.).

Figure 37. Top Signal Layer



Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector (or to an AGP video controller, if implemented as a "down" solution), utilizing a minimum number of vias on each net: AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT#, and ST[2:0].

In addition to the minimum signal set listed previously, it is strongly recommended that half of all AGP signals be referenced to ground, depending on the board layout. In the ideal design, the entire AGP interface signal field would be referenced to ground.

These recommendations are not specific to any particular PCB stack-up, but are applicable to all Intel chipset designs.

2.8.7. V_{DDQ} Generation and TYPEDET#

AGP specifies two separate power planes (V_{CC} and V_{DDQ}). V_{CC} is the core power for the graphics controller. V_{CC} is **always** 3.3 V. V_{DDQ} is the interface voltage. In AGP 1.0 implementations, V_{DDQ} was also 3.3 V. For the designer developing an AGP 1.0 motherboard, there is no distinction between V_{CC} and V_{DDQ}, because both are tied to the 3.3 V power plane on the motherboard.

AGP 2.0 requires that these power planes be separate. In conjunction with the 4× data rate, the AGP 2.0 interface specification provides for low-voltage (1.5 V) operation. The AGP 2.0 specification implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (V_{DDQ}). The motherboard must provide either 1.5 V or 3.3 V to the add-in card, depending on the state of the TYPEDET# signal. (Refer to Table 12.) 1.5 V low-voltage operation applies **only** to the AGP interface (V_{DDQ}). V_{CC} is **always** 3.3 V.

Note: The motherboard provides 3.3 V to the V_{CC} pins of the AGP connector. If the graphics controller needs a lower voltage, then the add-in card must regulate the 3.3 V V_{CC} voltage to the controller's requirements. The graphics controller may *only* power AGP I/O buffers with the V_{DDQ} power pins.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates at 1.5 V or 3.3 V. If TYPEDET# is floating (i.e., no connect) on an AGP add-in card, the interface is 3.3 V. If TYPEDET# is shorted to ground, the interface is 1.5 V.

Table 12. TYPDET#/V_{DDQ} Relationship

TYPEDET# (on Add-in Card)	V_{DDQ} (Supplied by MB)
GND	1.5 V
N/C	3.3 V

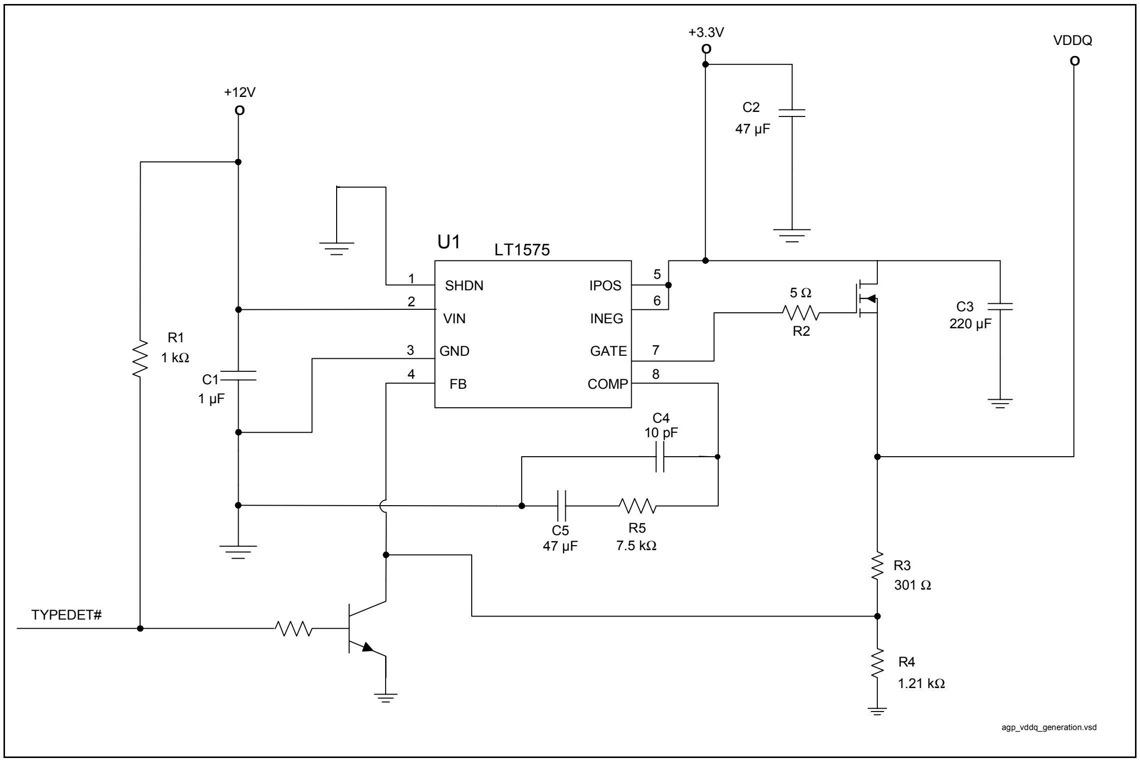
As a result of this requirement, the motherboard must provide a flexible voltage regulator. This regulator must supply the appropriate voltage to the V_{DDQ} pins on the AGP connector. For specific design recommendations, refer to the schematics in *Appendix A: Reference Design Schematics (Uniprocessor)*. V_{DDQ} generation and AGP V_{REF} generation must be considered together. Before developing V_{DDQ} generation circuitry, refer to *the AGP 2.0 Interface Specification*.

Figure 38 demonstrates one way to design the V_{DDQ} voltage regulator. This regulator is a linear regulator with an external, low-$R_{DS\text{-}ON}$ FET. The source of the FET is connected to 3.3 V. This regulator will convert 3.3 V to 1.5 V or pass 3.3 V, depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3 V (not 5 V) to control thermals. (i.e., 5 V regulated down to 1.5 V with a linear regulator will dissipate approximately 7 W at 2 A.) Because it must draw power from 3.3 V and, in some situations, must simply pass that 3.3 V to V_{DDQ} (when a 3.3 V add-in card is placed in the system), the regulator **must** use a low-$R_{DS\text{-}ON}$ FET.

AGP 1.0 modified V_{DDQ} 3.3_{MIN} to 3.1 V. When an ATX power supply is used, the 3.3 V_{MIN} is 3.168 V. Therefore, 68 mV of drop is allowed across the FET at 2 A. This corresponds to an FET with an $R_{DS\text{-}ON}$ of 34 mW.

How does the regulator switch? The feedback resistor divider is set to 1.5 V. When a 1.5 V card is placed in the system, the transistor is off and the regulator regulates to 1.5 V. When a 3.3 V card is placed in the system, the transistor is on and the feedback is pulled to ground. When this happens, the regulator drives the gate of the FET to nearly 12 V. This turns on the FET and passes 3.3 V – 2 A × $R_{DS\text{-}ON}$ to V_{DDQ}.

Figure 38. AGP V_{DDQ} Generation Example Circuit



2.8.8. V_{REF} Generation for AGP 2.0 (2× and 4×)

V_{REF} generation for AGP 2.0 will differ, depending on the AGP card type used. The 3.3 V AGP cards generate V_{REF} locally (i.e., they have a resistor divider on the card that divides V_{DDQ} down to V_{REF}), as shown in Figure 39. To account for potential differences between V_{DDQ} and GND at the MCH and graphics controller, 1.5 V cards use a source-generated V_{REF}. (i.e., the V_{REF} signal is generated at the graphics controller and sent to the MCH, and another V_{REF} is generated at the MCH and sent to the graphics controller.).

Both the graphics controller and the MCH are required to generate V_{REF} and distribute it through the connector (1.5 V add-in cards only). Two pins are defined on the AGP 2.0 universal connector to allow this V_{REF} passing, as follows:

- VREFGC: V_{REF} from the graphics controller to the chipset
- VREFCG: V_{REF} from the chipset to the graphics controller

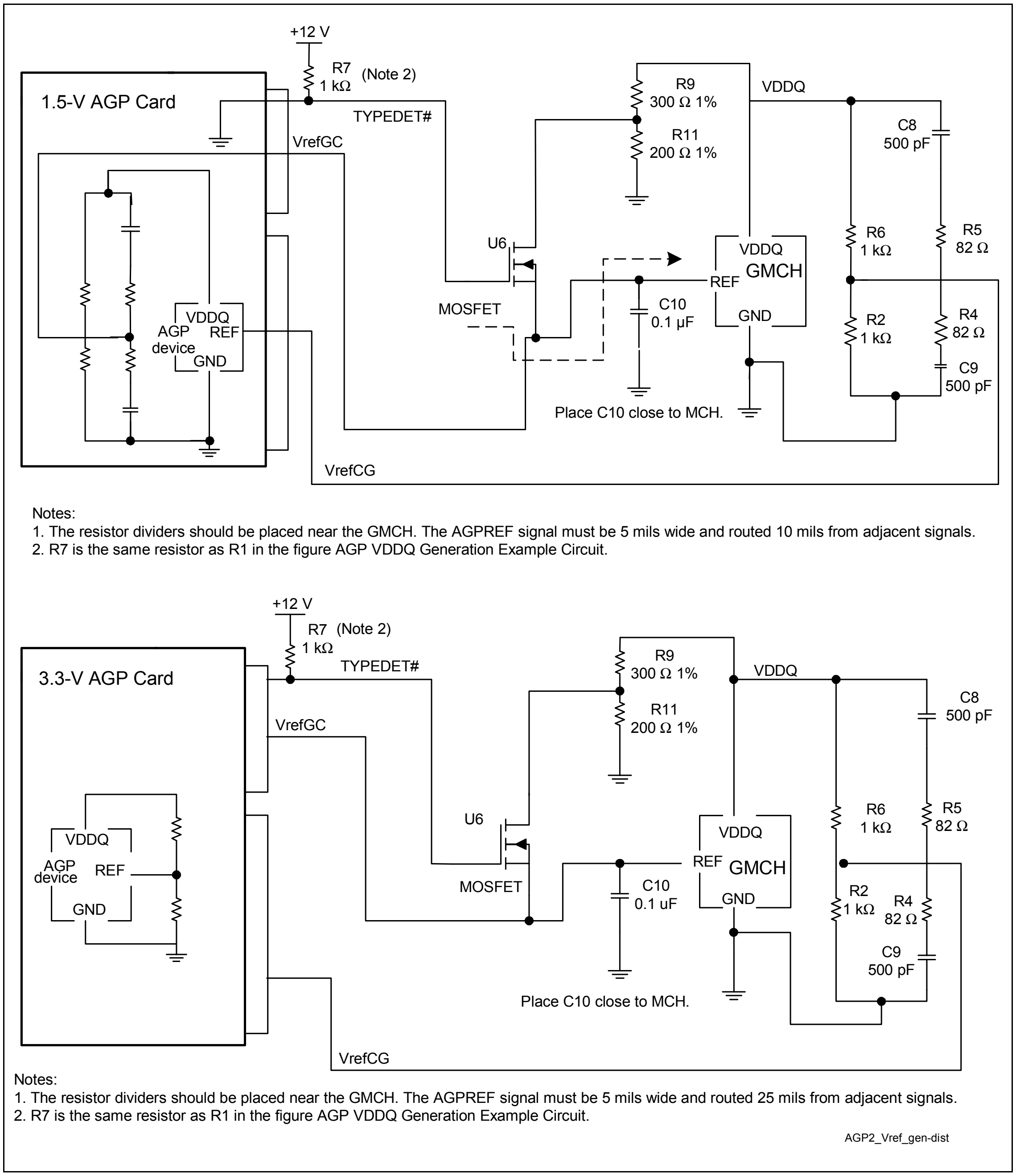
To preserve the common-mode relationship between the V_{REF} and data signals, the routing of the two V_{REF} signals must be matched in length to the strobe lines, within 0.5 inch on the motherboard and within 0.25 inch on the add-in card.

The voltage-divider networks consist of AC and DC elements, as shown in Figure 39.

The V_{REF} divider network should be placed as close as practical to the AGP interface, to obtain the benefit of the common-mode power supply. However, the trace spacing around the V_{REF} signals must be a minimum of 25 mils, to reduce crosstalk and maintain signal integrity.

During a 3.3 V AGP 2.0 operation, V_{REF} must be 0.4 V_{DDQ}. However, during a 1.5 V AGP 2.0 operation, V_{REF} must be 0.5 V_{DDQ}. This requires a flexible voltage divider for V_{REF}. Various methods of accomplishing this exist, such as the example in the following figure.

Figure 39. AGP 2.0 V_{REF} Generation and Distribution



The flexible V_{REF} divider shown in the preceding figure uses an FET switch to switch between the locally generated V_{REF} (for 3.3 V add-in cards) and the source-generated V_{REF} (for 1.5 V add-in cards).

Use of the source-generated V_{REF} at the receiver is optional and is a product implementation issue beyond the scope of this document.

2.8.9. Compensation

The MCH AGP interface supports resistive buffer compensation (RCOMP). Tie the GRCOMP pin to a 40 Ω, 2% (or 39-Ω, 1%) pull-down resistor (to ground), via a 10 mil-wide, very short (<0.5 inch) trace.

2.8.10. AGP Pull-Ups

AGP control signals require pull-up resistors to V_{DDQ} on the motherboard, to ensure that they maintain stable values when no agent is actively driving the bus. The signals requiring pull-up resistors are:

- 1× timing domain signals
  - FRAME#
  - TRDY#
  - IRDY#
  - DEVSEL#
  - STOP#
  - SERR#
  - PERR#
  - RBF#
  - PIPE#
  - REQ#
  - WBF#
  - GNT#
  - ST[2:0]

  It is critical that these signals be pulled up to V_{DDQ} (**not** 3.3 V).

  The trace stub to the pull-up resistor on 1× timing domain signals should be kept at less than 0.5 inch, to avoid signal reflections from the stub.

  The strobe signals require pull-up/pull-downs on the motherboard, to ensure that they maintain stable values when no agent is driving the bus.

Note: INTA# and INTB# should be pulled to 3.3 V, not V_{DDQ}.

- 2×/4× timing domain signals
  - AD_STB[1:0] (pull-up to V_{DDQ})
  - SB_STB (pull-up to V_{DDQ})
  - AD_STB[1:0]# (pull-down to ground)
  - SB_STB# (pull-down to ground)

  The trace stub to the pull-up/pull-down resistor on 2×/4× timing domain signals should be kept to less than 0.1 inch, to avoid signal reflections from the stub.

  The pull-up/pull-down resistor value requirements are shown in the following table.

R_{MIN}	R_{MAX}
4 kΩ	16 kΩ

The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ.

2.8.10.1. AGP Signal Voltage Tolerance List

The following signals on the AGP interface are 3.3 V tolerant during a 1.5 V operation:

- PME#
- INTA#
- INTB#
- GPERR#
- GSERR#
- CLK
- RST

The following signals on the AGP interface are 5 V tolerant (refer to the USB specification):

- USB+
- USB-
- OVRCNT#

The following signal is a special AGP signal, which is either grounded or not connected on an AGP card.

- TYPEDET#

Note: All other signals on the AGP interface are in the V_{DDQ} group. They are not 3.3 V tolerant during a 1.5 V AGP operation.

2.8.11. Motherboard / Add-in Card Interoperability

Currently, there are three AGP connectors:

- 3.3 V AGP connector
- 1.5 V AGP connector
- Universal AGP connector.

To maximize add-in flexibility, it is highly advisable to implement the universal connector in an Intel 820E chipset-based system. All add-in cards are either 3.3 V or 1.5 V cards. Due to timings, 4× transfers at 3.3 V are not allowed.

Table 13. Connector / Add-in Card Interoperability

	1.5 V Connector	3.3 V Connector	Universal Connector
1.5 V card	Yes	No	Yes
3.3 V card	No	Yes	Yes

Table 14. Voltage / Data Rate Interoperability

	1×	2×	4×
1.5 V V_{DDQ}	Yes	Yes	Yes
3.3 V V_{DDQ}	Yes	Yes	No

2.8.12. AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that, without proper retention, AGP cards and AGP In-Line Memory Module (AIMM) cards may come unseated during system shipping and handling. In order to prevent the disengagement of AGP cards and AIMM modules, Intel recommends that AGP-based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket used to properly locate the card with respect to the chassis and to assist with card retention. The AGP RM is available in two different handle orientations: left-handed (see Figure 40) and right-handed. Most system boards accommodate the left-handed AGP RM. Because the manufacturing capacity is greater for the left-handed RM, Intel recommends that customers design into their systems the left-handed AGP RM (Figure 41). The right-handed AGP RM is identical to the left-handed AGP RM, except for the position of the actuation handle, which is located on the same end as in the primary design, but extends from the opposite side, parallel to the longitudinal axis of the part. Figure 41 details the keep-out information for the left-handed AGP RM. Use this information to ensure that your motherboard design leaves adequate space for RM installation.

The AGP interconnect design requires that the AGP card be retained so as to limit card back-out within the AGP connector to 0.99 mm (0.039 in.) max. For this reason, new cards should have an additional mechanical keying tab notch, which provides an anchor point on the AGP card for interfacing with the AGP RM. The RM's round peg engages with the AGP or AIMM card's retention tab, thereby preventing the card from disengaging during dynamic loading. The additional notch in the mechanical keying tab is required for 1.5 V AGP cards and is recommended for the new 3.3 V AGP cards.

Figure 40. AGP Left-Handed Retention Mechanism

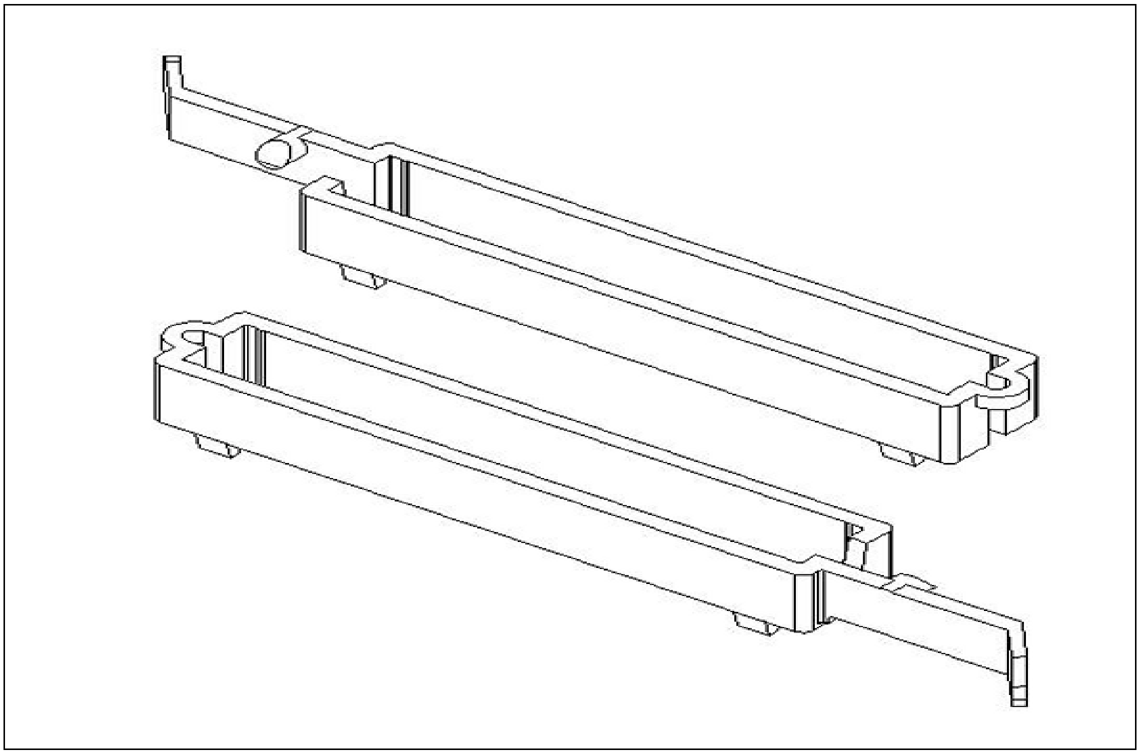
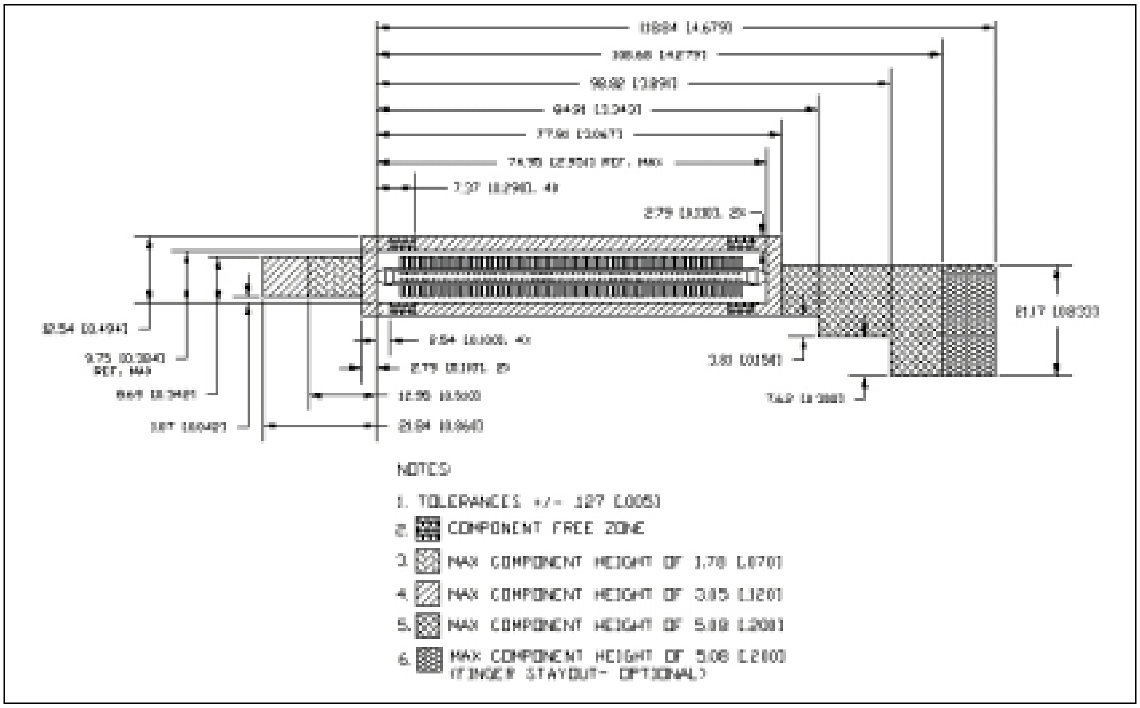


Figure 41. AGP Left-Handed RM Keep-Out Information



Recommended for all AGP cards, the AGP RM is detailed in Engineering Change Request No. 48 (ECR #48), which details approved changes to the *Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0*. Intel intends to incorporate the AGP RM changes into later revisions of the AGP interface specification. In addition, Intel has defined a reference design for a mechanical device utilizing the features defined in ECR #48.

ECR #48 can be viewed on the Intel Web site at: http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors:

Resin Color	Supplier Part No.	"Left-Handed" Orientation (Preferred)	"Right-Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

2.9. Hub Interface

The MCH and ICH2 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the MCH to ICH2, with all signals referenced to V_{SS}. Layer transition should be keep to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer. The hub interface is broken into two signal groups: data signals and strobe signals. These groups are:

- Data signal
  - HL[10:0]
- Strobe signals
  - HL_STB
  - HL_STB#

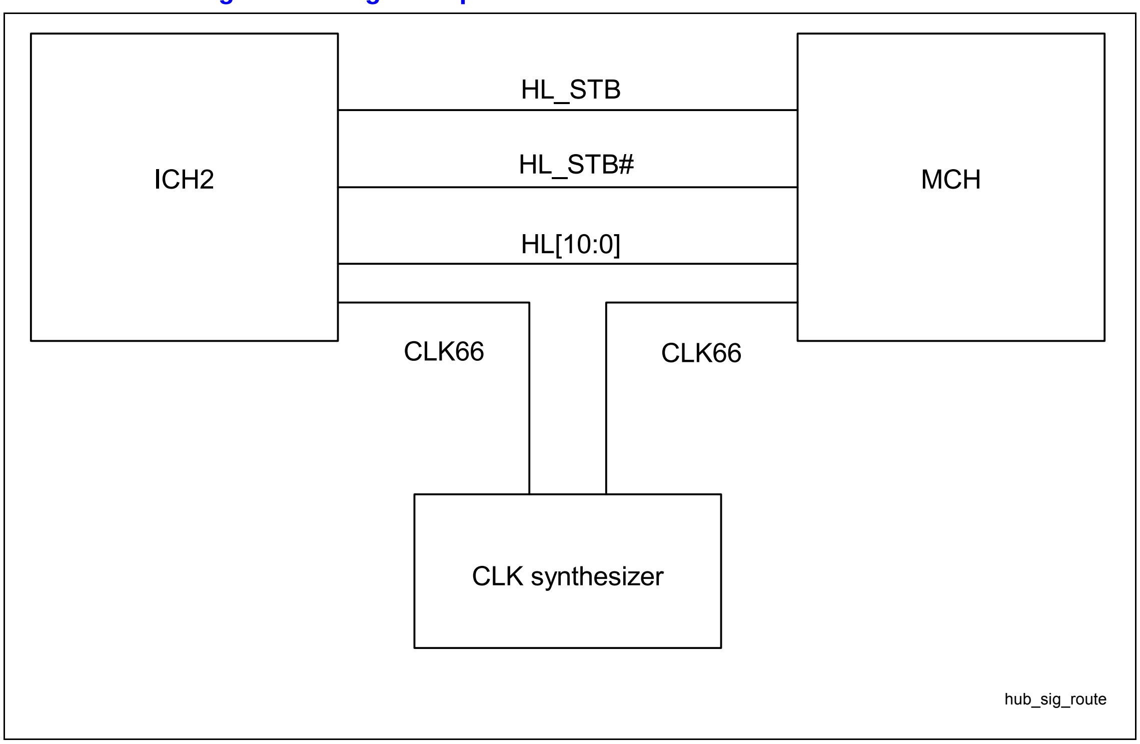
Note: HL_STB/HL_STB# is a differential strobe pair.

For the 8-bit hub interface, HL[7:0] are associated with HL_STB and HL_STB#.

No pull-ups or pull-downs are required on the hub interface.

Each signal must be routed so as to meet the guidelines documented for the signal group to which it belongs.

Figure 42. Hub Interface Signal Routing Example



2.9.1. 8-Bit Hub Interface Routing Guidelines

This section documents the routing guidelines for the 8-bit hub interface. This hub interface connects the ICH2 to the MCH. This interface supports two buffer modes: normal and enhanced. The ICH2 uses its HLCOMP pin to set the buffer mode, and the MCH uses its HLA_ENH# pin to configure its 8-bit hub interface buffers. Both devices must be configured for the same buffer mode.

When the buffers are configured for normal mode, the trace impedance must equal 60 Ω ± 10%. In the enhanced buffer mode, the trace impedance can be 50 Ω ± 10% or 60 Ω ± 15%.

Table 15. 8-Bit Hub Interface Buffer Configuration Setting

Component	Hub Interface Buffer Mode	Trace Impedance	Strap
ICH2	Normal/Single	60 Ω	HLCOMP pulled to V_{CC} 1_8 (see Note)
	Normal/Local	50 or 60 Ω	HLCOMP pulled to GND (see Note)
MCH	Normal/Single	60 Ω	Default
	Normal/Local	50 or 60 Ω	HLA_ENH# pulled to GND via a 100 Ω resistor

Note: Refer to Section 2.9.1.4 for the specific resistor value

2.9.1.1. 8-Bit Hub Interface Data Signals

The 8-bit hub interface data signal traces should be routed 5 mils wide with 20 mils trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. To break out of the MCH and ICH2 package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mils of the package.

The maximum hub interface data signal trace lengths in the normal and enhanced buffer modes are 8 inches and 14 inches, respectively. Each data signal must be matched within ±0.1 inch of the HL_STB differential pair. There is no explicit matching requirement between the individual data signals.

2.9.1.2. 8-Bit Hub Interface Strobe Signals

The hub interface strobe signals should be routed 5 mils wide with 20 mils trace spacing (5 on 20). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signals in normal mode is 8 inches and in enhanced mode is 14 inches. Each strobe signal must be the same length, and each data signal must be matched within ±0.1 inch of the strobe signals.

2.9.1.3. 8-Bit Hub Interface HUBREF Generation/Distribution

HUBREF is the hub interface reference voltage. Depending on the buffer mode (i.e., normal or enhanced buffer mode), the HUBREF voltage requirement must be set appropriately for proper operation. See Table 16 for the HUBREF voltage specifications for normal and enhanced buffer modes and the associated resistor recommendations for the voltage divider circuit.

Table 16. 8-Bit Hub Interface HUBREF Generation Circuit Specifications

Buffer Mode	HUBREF Voltage Specification (V)	Recommended Resistor Values for the HUBREF Divider Circuit (Ω)
Normal/Single	1/2 V_{CC} 1_8 ± 2%	R1 = R2 = 150 ± 1%
Normal/Local	2/3 V_{CC} 1_8 ± 2%	R1 = 150 ± 1%, R2 = 301 ± 1%

The single HUBREF divider should not be located more than 4 inches away from either MCH or ICH2. If the single HUBREF divider is located more than 4 inches away, then the locally generated hub interface reference dividers should be used instead. The reference voltage generated by a single HUBREF divider should be bypassed to ground at each component with a 0.0 µF capacitor located close to the component HUBREF pin. If the reference voltage is generated locally, the bypass capacitor must be close to the component HUBREF pin. Example HUBREF divider circuits are shown in the following figures.

Figure 43. 8-Bit Hub Interface with a Shared Reference Divider Circuit (Normal/Single Mode)

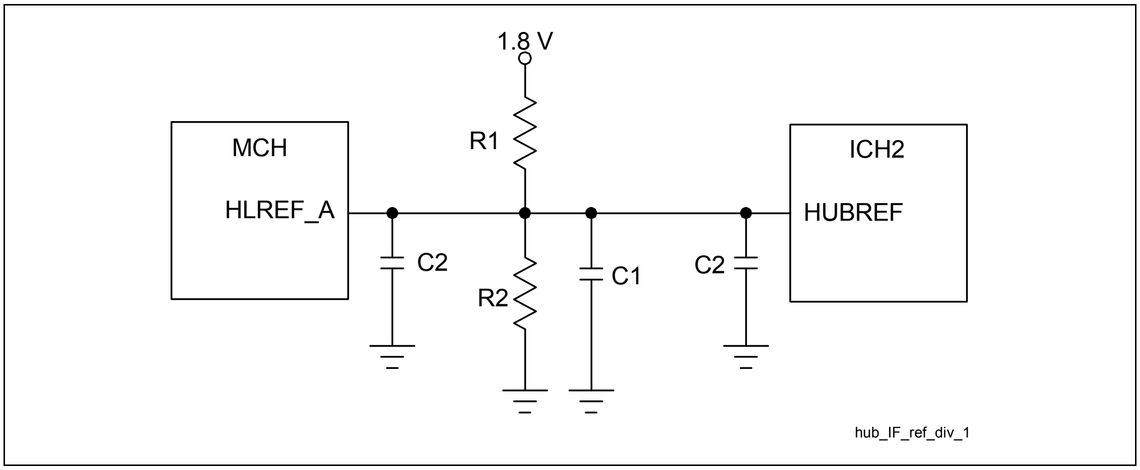
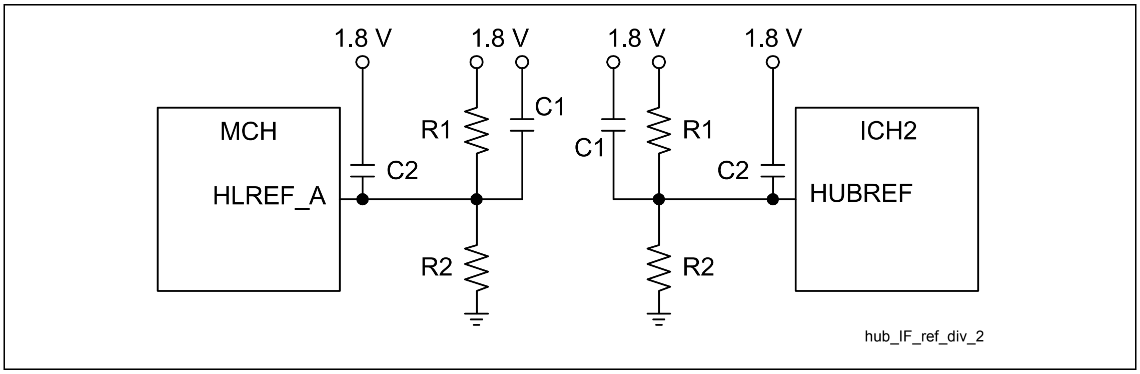


Figure 44. 8-Bit Hub Interface with Locally Generated Reference Divider Circuits (Normal/Local Mode)



The resistor values, R1 and R2, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the previous circuits) should be placed close to R1 and R2. Also, a 0.01 µF bypass capacitor (C2 in the previous circuits) should be placed within 0.25 inch of each HUBREF pin. The trace length from the divider circuit to the HLREF pin must be no longer than 3.5 inches.

2.9.1.4. 8-Bit Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires resistive compensation (RCOMP). The guidelines are as follows shown in the following table.

Table 17. 8-Bit Hub Interface RCOMP Resistor Values

Component	Hub Interface Buffer Mode	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied to
ICH2	Normal/Single	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	VCC1_8
	Normal/Local	60 Ω ± 15%	30 Ω ± 1%	V_{SS}
		50 Ω ± 10%	25 Ω ± 1%	V_{SS}
MCH	NormalSingle	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	VCC1_8
	Normal/Local	60 Ω ± 15%	30 Ω ± 1%	V_{SS}
		50 Ω ± 10%	25 Ω ± 1%	V_{SS}

The MCH also has a hub interface compensation pin. This signal (HLCOMP) also requires the RCOMP method described for the ICH2.

2.9.1.5. 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per component (i.e., the ICH2 and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the VCC1_8 side of the capacitors to the VCC1_8 power pins. Similarly, if the layout allows, metal fingers running on the VCC1_8 side of the board should connect the ground side of the capacitors to the V_{SS} power pins.

2.10. System Bus Design – Pentium® III Processor for the Intel® PGA370 Socket Layout Guidelines

The Pentium III processor in the FC-PGA package is the next member of the P6 family in the Intel® IA-32 processor line. The processor uses the same core and offers the same performance as the Pentium III processor in the S.E.C.C. 2 package, but utilizes a new package technology called “Flip-Chip Pin Grid Array,” or FC-PGA. This package utilizes the same 370-pin, zero-insertion-force socket (Intel PGA370) used by the Intel® Celeron™ processor. Thermal solutions are attached directly to the back of the processor core package, without the use of a thermal plate or heat spreader.

The Intel PGA370 design requires additional termination at the chipset for the AGTL+ signals. In addition, the platform power delivery requirements are different for the Intel PGA370 design, compared with the SECC2 design. The AGTL+ layout considerations detailed in *Chapter 3 Advanced System Bus Design* still apply to FC-PGA designs (including ground-referencing the AGTL+ signals).

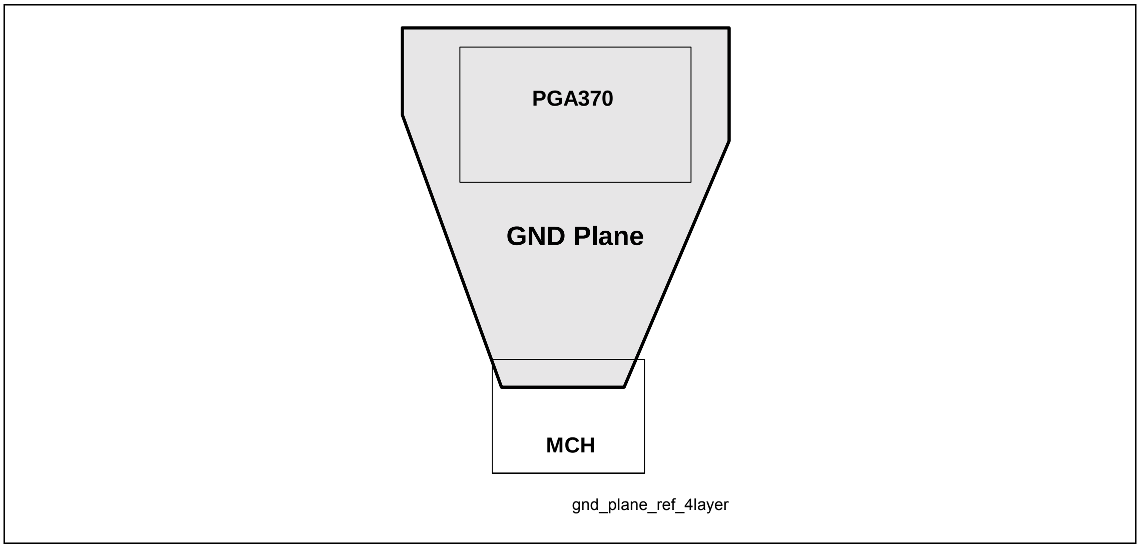
The design guidelines are found in the *Intel® 820 Chipset Design Guide Addendum for the Pentium® III Processor for the PGA370 socket*. These guidelines can be downloaded from the Intel website at:

http://developer.intel.com/design/chipsets/designex/298178.htm

2.10.1. System Bus Ground Plane Reference

All system bus signals must be referenced to GND to provide the optimal current return path. The ground reference must be continuous from the MCH to the Intel PGA370 socket. This may require a GND reference island on the plane layers closest to the signals. Any split in the ground island will provide a suboptimal return path. In a 4-layer board, this will require that the VCCID island be on an outer signal layer. The following figure shows a 4-layer motherboard power plane with ground reference for system bus signals.

Figure 45. Ground Plane Reference (4-Layer Motherboard)



2.11. Additional Host Bus Guidelines

Minimizing Crosstalk on the AGTL+ Interface

The following general rules will minimize the effect of crosstalk in a high-speed AGTL+ bus design:

- Maximize the space between traces. Maintain a minimum of 0.010 inch between traces, wherever possible. It may be necessary to use tighter spacings when routing between component pins.
- Avoid parallelism between signals on adjacent layers.
- Since AGTL+ is a low-signal-swing technology, it is important to isolate AGTL+ signals from other signals by at least 0.025 inch. This will avoid coupling from signals with larger voltage swings, such as 5 V PCI.
- Select a board stack-up that minimizes the coupling between adjacent signals.
- Route AGTL+ address, data, and control signals in separate groups, to minimize crosstalk between groups. The Pentium III processor in the FC-PGA package uses a split-transaction bus. In a given clock cycle, the address lines and corresponding control lines could be driven by a different agent than the data lines and their corresponding control lines.

Additional Considerations

- Distribute V_{TT} with a wide trace. A 0.050 inch minimum trace is recommended to minimize DC losses. Route the V_{TT} trace to all components on the host bus. Be sure to include decoupling capacitors. Guidelines for V_{TT} distribution and decoupling are contained in the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*.
- PV_{REF} should be generated with one voltage divider between the MCH and the processor for all V_{REF} pins. Be sure to include decoupling capacitors. Guidelines for V_{REF} distribution and decoupling are contained in the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. Regarding special-case AGTL+ signals for simulation, there are six AGTL+ signals that can be driven simultaneously by more than one agent. These signals may require extra attention during the layout and validation portions of the design. When a signal is asserted (driven low) by two agents on the same clock edge, the two falling wavefronts will meet at some point on the bus. This can create a large undershoot, followed by ringback, which may violate the ringback specifications. This "wired-OR" situation should be simulated for the following signals: AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

2.12. IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH2 has integrated the series resistors typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. Intel does not anticipate requiring additional series termination, but OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5 mil traces on 7 mil spaces, and must be less than 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inch shorter than the longest IDE signal (on that channel).

Cable

- **Length of cable:** Each IDE cable must be ≤18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the connector next closest to the end of the cable (6 inches away from the end of the cable).
- **Grounding:** Provide a direct low-impedance chassis path between the motherboard ground and the hard disk drives.
- **ICH2 placement:** The ICH2 must be placed ≤8 inches from the ATA connector(s).

2.12.1. Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE controller supports PIO, multiword (8237-style) DMA, and Ultra DMA modes 0 through 5. The ICH2 must determine the type of cable present, to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate as follows: ground, signal, ground, signal, ground, signal, ground…. All ground wires are tied together on the cable (and they are tied to ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049, which is obtainable from the Small Form Factor Committee.

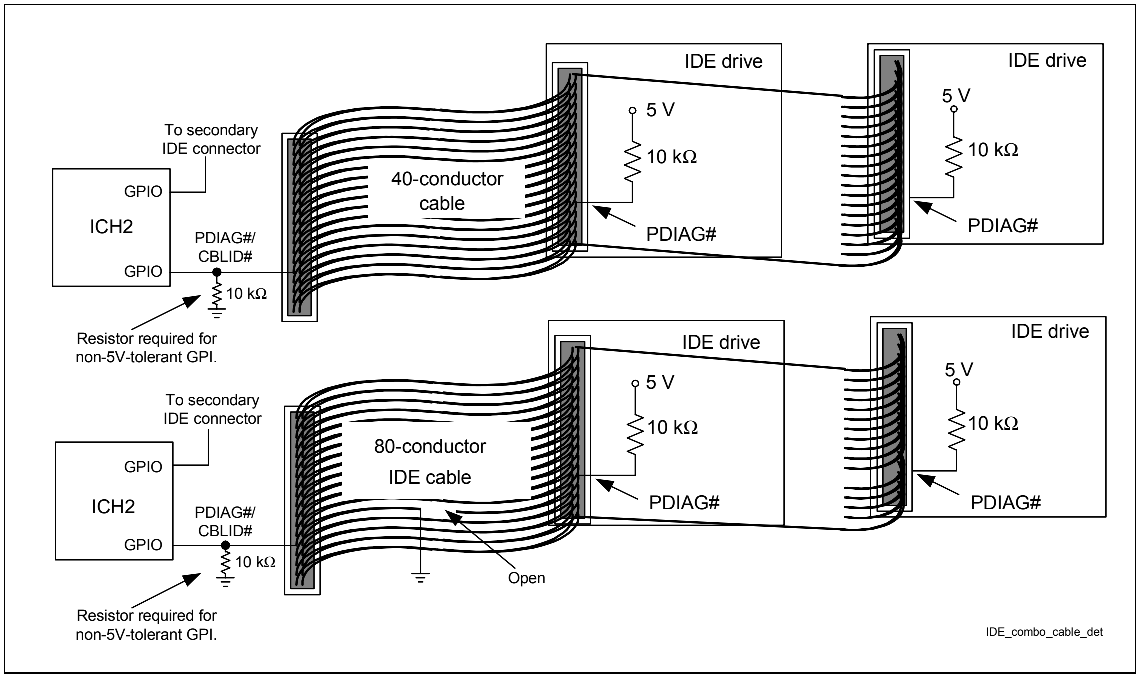
To determine if the ATA/66 or ATA/100 mode can be enabled, the Intel 820E chipset requires that the system software attempt to determine the type of cable used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination host-side/device-side detection mechanism. Note that host-side detection cannot be implemented on an NLX form factor system, since this configuration does not define the interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely only on the device-side detection mechanism.

2.12.2. Combination Host-Side/Device-Side Cable Detection

Host-side detection (described in the ATA/ATAPI-4 Standard, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in the following figure. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. Not all GPI and GPIO pins on the ICH2 are 5 V tolerant. If non-5 V tolerant inputs are used, a resistor divider is required to prevent 5 V on the ICH2 or FWH Flash BIOS pins. The proper value of the divider resistor is 10 kΩ, as shown in Figure 46.

Figure 46. Combination Host-Side/Device-Side IDE Cable Detection



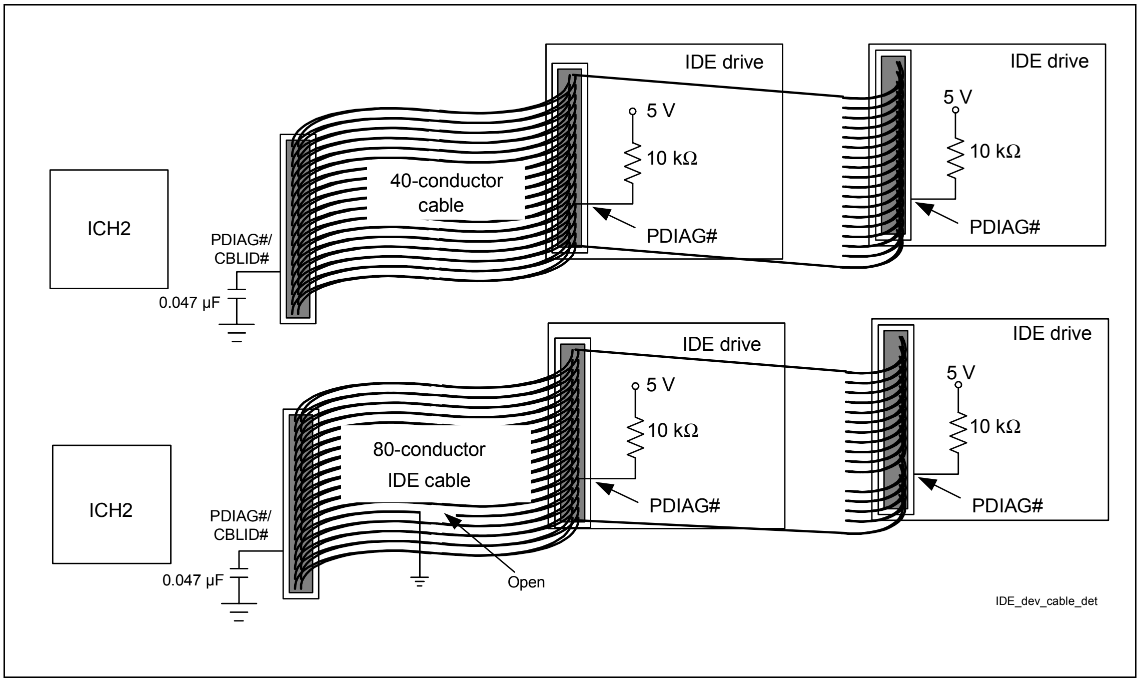
After diagnostics, this mechanism allows the BIOS to sample PDIAG#/CBLID#. If the signal is high, there is a 40-conductor cable in the system and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected low, then there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93 bit 13 is 1, then an 80-conductor cable is present. If this bit is 0, then a legacy slave (Device 1) is preventing proper cable detection, and the BIOS should configure the system as though a 40-conductor cable were present and notify the user of the problem.

2.12.3. Device-Side Cable Detection

For platforms that must implement device-side detection **only** (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard, as shown in the following figure. This capacitor **should not** be populated when implementing the recommended combination host-side/device-side cable detection mechanism described previously.

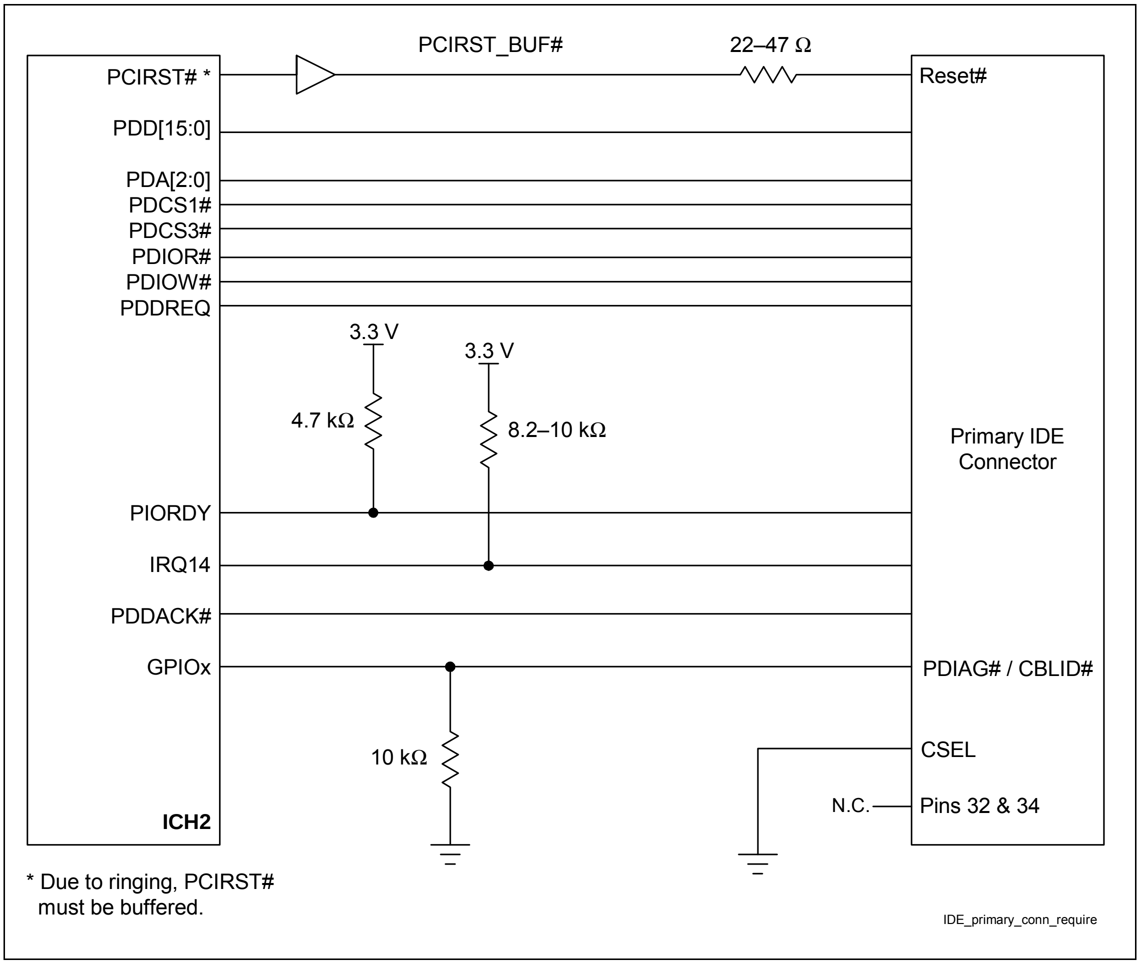
Figure 47. Device-Side IDE Cable Detection



This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4, or 5 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host, so the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host, so the signal will rise more slowly as the capacitor charges. The drive can detect the difference in rise times and will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during the system boot, as described in the ATA/66 specification.

2.12.4. Primary IDE Connector Requirements

Figure 48. Connection Requirements for Primary IDE Connector

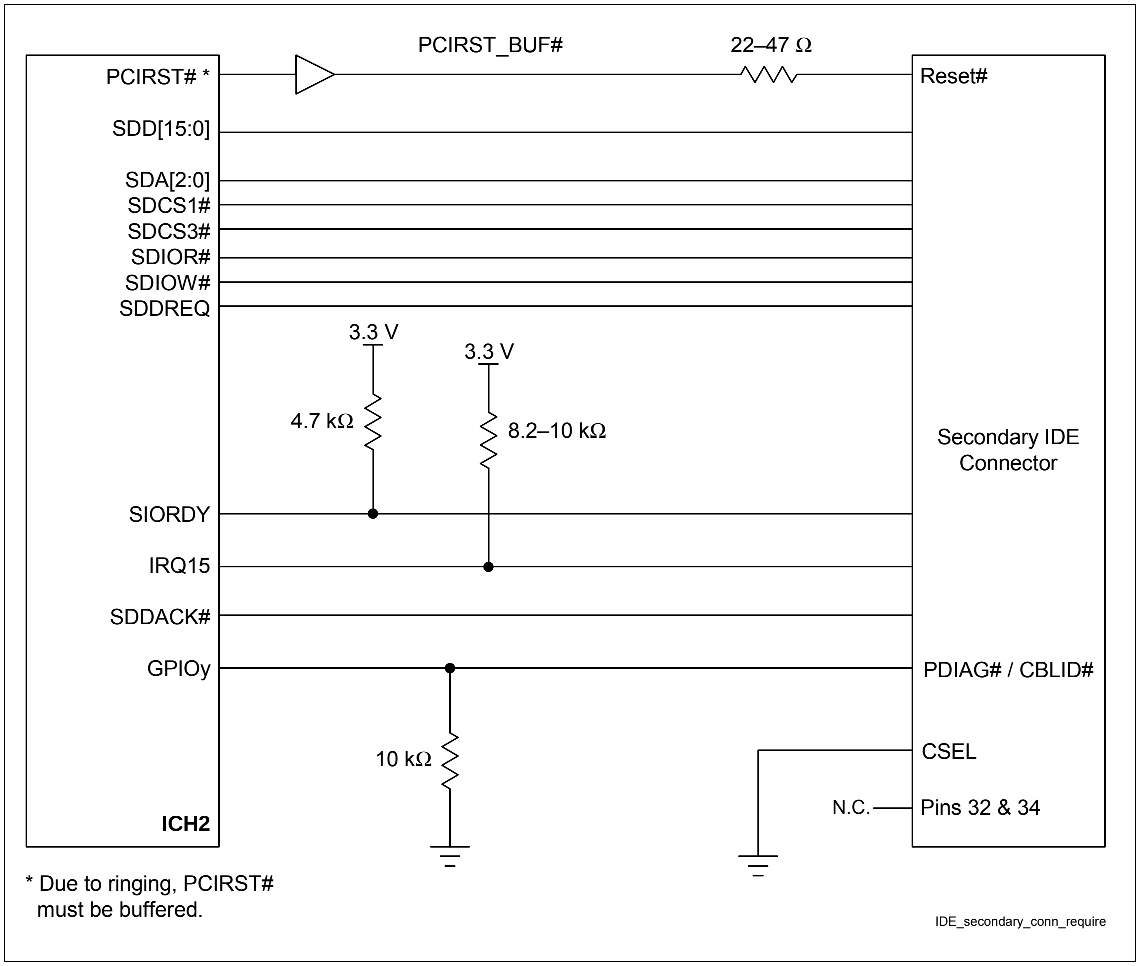


NOTES:

1. 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on the signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7 kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY.
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are place as close as possible to the connector. Values are determined for each unique motherboard design.
5. A 10 kΩ pull-down resistor to ground is required on the PDIAG/CBLID signal. This prevents the GPI pin from floating if a device is not present on the primary IDE interface.

2.12.5. Secondary IDE Connector Requirements

Figure 49. Connection Requirements for Secondary IDE Connector



NOTES:

1. 22 Ω to 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on the signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC3.
3. A 4.7 kΩ pull-up resistor to VCC3 is required on PIORDY and SIORDY
4. Series resistors can be placed on the control and data lines to improve signal quality. The resistors are place as close as possible to the connector. Values are determined for each unique motherboard design.
5. A 10 kΩ pull-down resistor to ground is required on the PDIAG/CBLID signal. This prevents the GPI pin from floating if a device is not present on the secondary IDE interface.

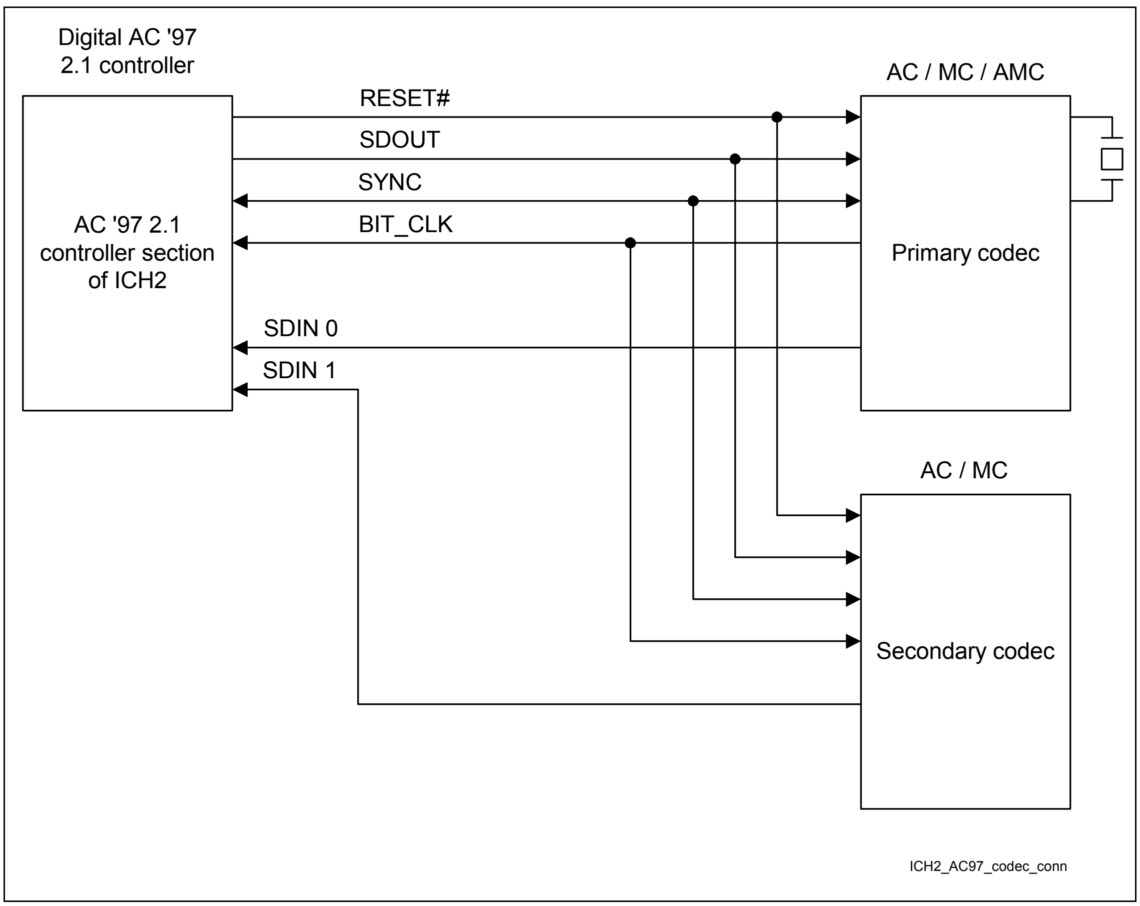
2.13. AC’97

The ICH2 implements an AC’97 2.1-compliant digital controller. Any codec attached to the ICH2 AC-link also must be AC’97 2.1 compliant. Please contact your codec IHV for information on 2.1-compliant products. The AC’97 2.1 specification is on the following Intel web page:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted serially. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. The following figure shows a two-codec topology of the AC-link for the ICH2.

Figure 50. ICH2 AC’97– Codec Connection



The AC’97 interface can be routed using 5 mil traces, with 5 mil space between traces. The maximum length from ICH2 to CODEC/CNR is 14 inches, in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC-link. The trace impedance should be as follows: $Z_0 = 60\ \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2) and any other codec present. This clock is used as the time base for latching and driving data.

The ICH2 supports Wake on Ring from S1-S5 via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are enabled only when the AC-Link Shut Off bit in the ICH2 is set. This keeps the link from floating when the AC-link is off or when no codec is present.

If the shut-off bit is not set, it implies that there is a codec on the link. Therefore, BITCLK and AC_SDOUT will be driven by the codec and ICH2, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, it can be assumed that there is at least one codec. If there is one or no codec on board, then the unused AC_SDINx pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

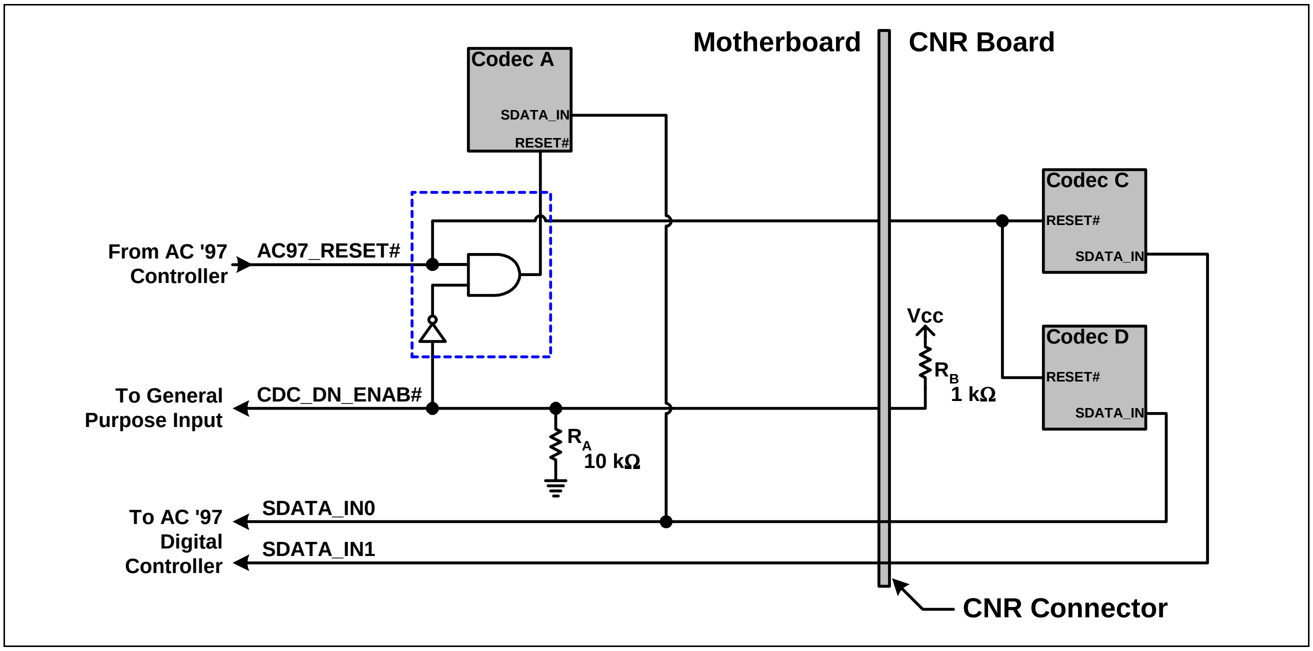
2.13.1. AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Please refer to Intel's White Paper Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser) for Intel's recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (shown in Figure 51 through Figure 54) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 51. CDC_DN_ENAB# Support Circuitry for a Single Codec on Motherboard



As shown in Figure 51, when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required in order to disable the motherboard codec when a CNR is installed which contains two AC '97 codecs (or a single AC '97 codec which must be the primary codec on the AC-Link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-Link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 52 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 52 and Figure 53 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line as to not conflict with the motherboard codec(s).

Figure 52. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

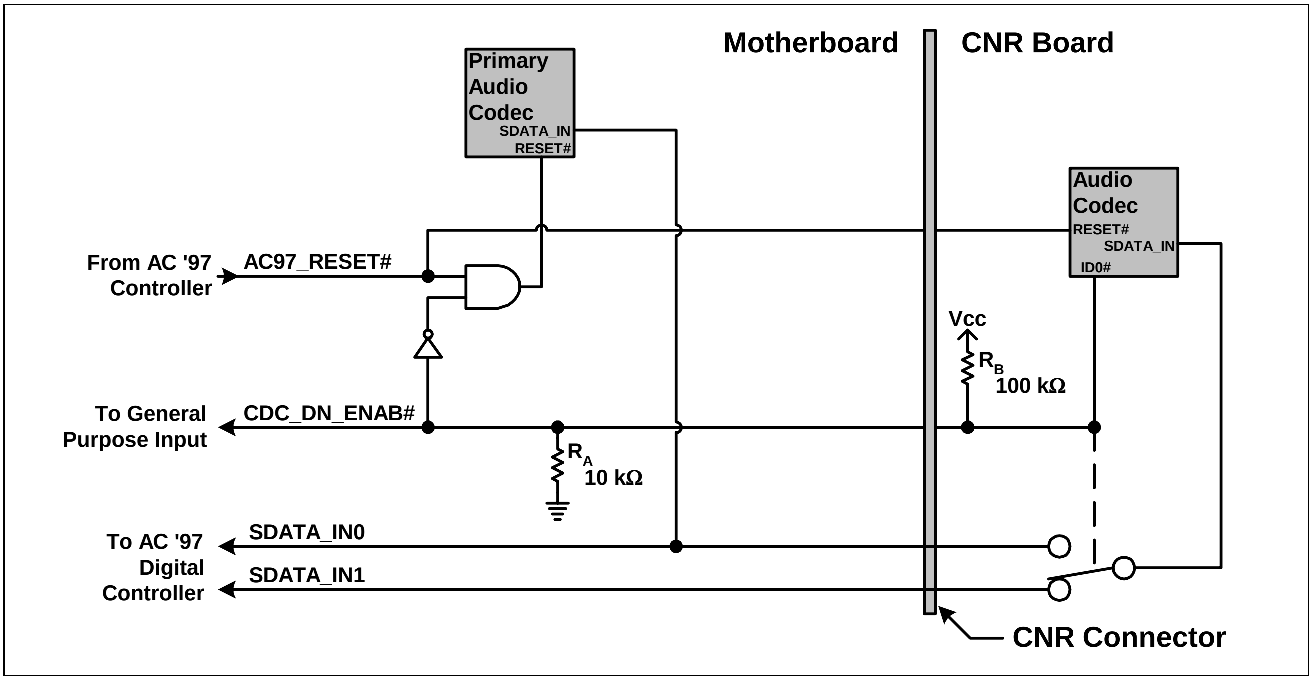


Figure 52 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 53. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR

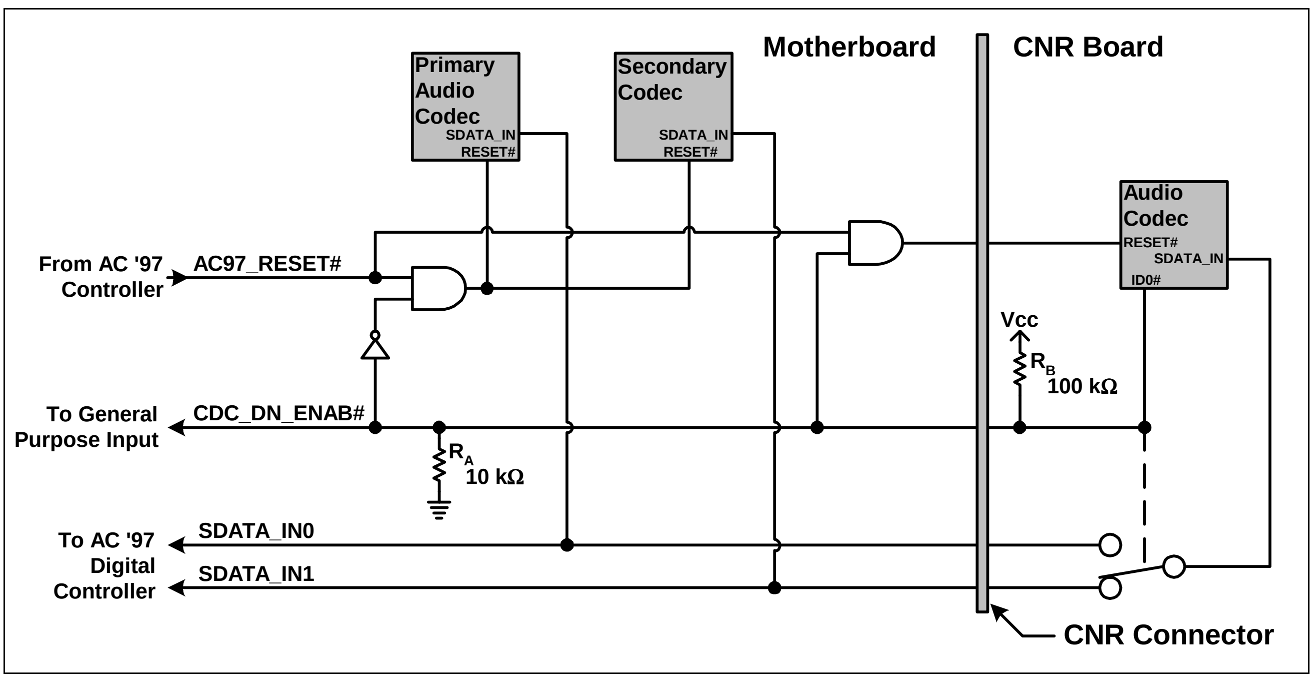
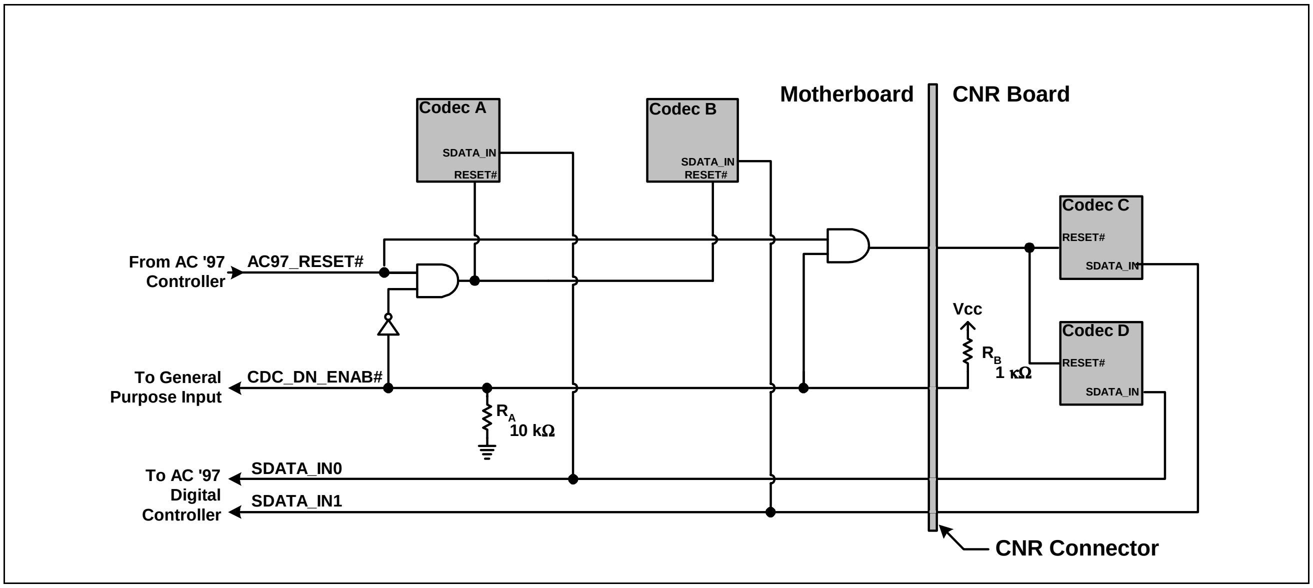


Figure 53 shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 54. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / Two-Codecs on CNR



Circuit Notes

1. While it is possible to disable down codecs, as shown above in Figure 53 and Figure 54, it is recommended against for reasons cited in the ICHx/AC'97 White Paper, including avoidance of shipping redundant and/or non-functional audio jacks.
2. All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
4. A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is **strongly recommended** for testing purposes.

Table 18. Signal Descriptions

CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC’97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC’97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC’97 Interface.
AC97_RESET#	Reset signal from the AC’97 Digital Controller (ICH2).
SDATA_IN*n*	AC’97 serial data from an AC’97-compliant codec to an AC’97-compliant controller (i.e., the ICH2).

Valid Codec Configurations

Table 19. Codec Configurations

Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

2.13.2. Communication and Networking Riser (CNR)

Related Documents:

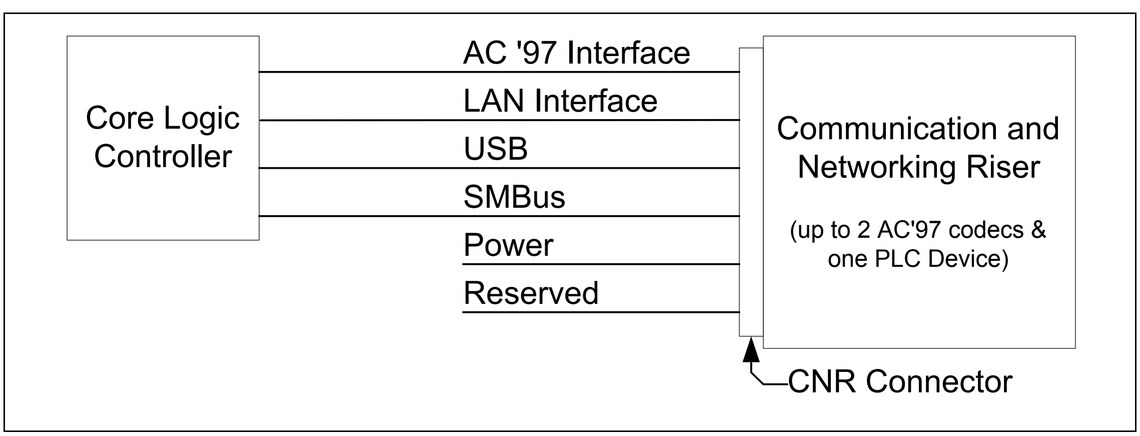
Communication Network Riser Specification, Revision 1.1, available at:

http://developer.intel.com/technology/cnr

The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Unlike the AMR, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build. It is required that the CNR A0-A2 pins be set to a unique address, so that the CNR EEPROM can be accessed. See CNR specification.

Figure 55 indicates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) can either be an Intel 82562EH or Intel 82562EM component. Refer to the CNR specification for additional information.

Figure 55. CNR Interface



2.13.3. AC'97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

Clocking is provided from the primary codec on the link via BITCLK, and it is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for the crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2) and by any other codec present. The clock is used as the time base for latching and driving data.

2.13.4. Motherboard Implementation

The following design considerations are provided for the implementation of an ICH2 platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH2 platform.

- Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH2 supports wake-on-ring from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required. The ICH2 does not wake from the S5 state via the AC'97 link.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

2.14. USB

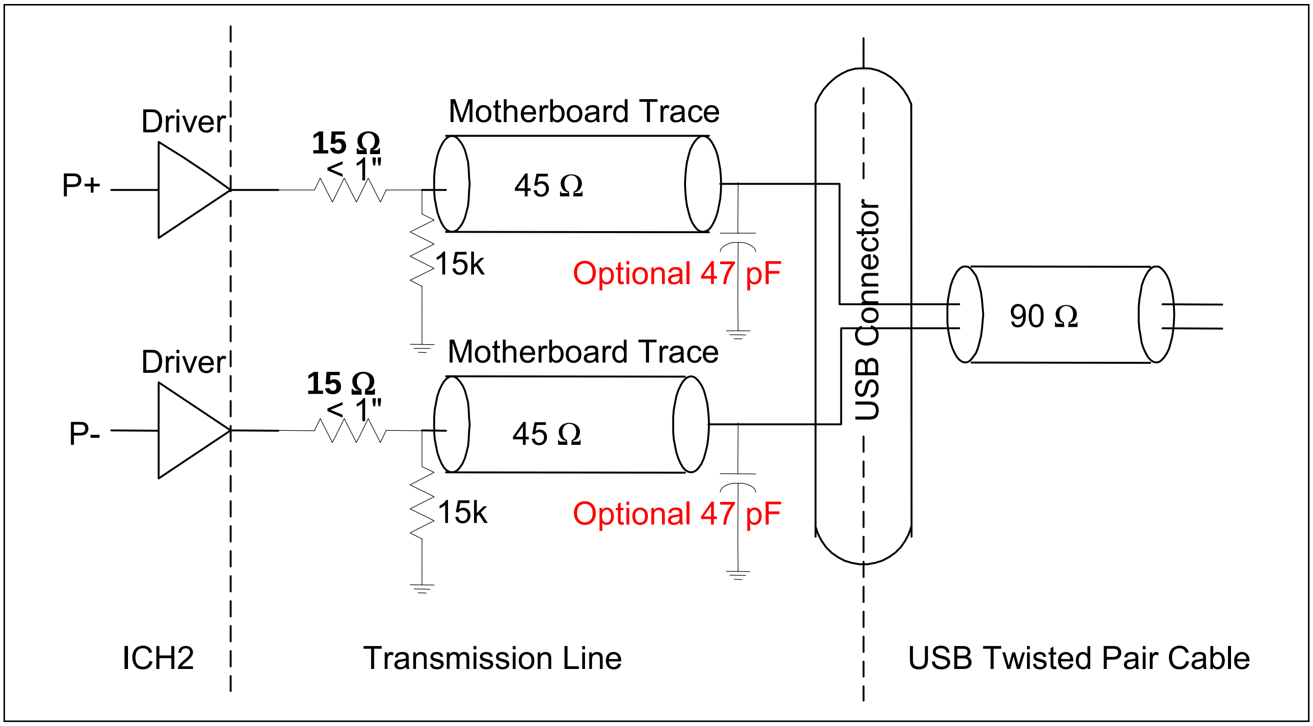
2.14.1. Using Native USB Interface

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15K pull-down resistors on both P+/P- data lines.
- 15 ohm series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.
- An optional 47 pF cap may be placed as close to the USB connector as possible on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap can be used for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15K +/-5% pull-down resistors should be placed on the USB Connector side of the series resistors on the USB data lines (P0+/- … P3+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-… P3+/- signals should be 45 ohms (to ground) for each USB signal P+ or P-. Using the stackup recommended in section 6.1, USB requires 9 mils traces. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 o Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
  USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 56 is the recommended USB schematic:

Figure 56. USB Data Signals



Recommended USB trace characteristics

• Impedance Z_0	=	45.4 Ω
• Line delay	=	160.2 ps
• Capacitance	=	3.5 pF
• Inductance	=	7.3 nH
• Resistance at 20 °C	=	53.9 mΩ

2.14.3. Disabling the Native USB Interface of ICH2

The ICH2 native USB interface can be disabled. This can be done when an external PCI based USB controller is being implemented in the platform. To disable the native USB Interface, ensure the differential pairs are pulled down thru 15 kΩ resistors, ensure the OC[3:0]# signals are de-asserted by pulling them up weakly to VCC3SBY, and that both function 2 and 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48 MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.

2.15. ISA Support

Implementations that require ISA support can benefit from the enhancements of the ICH2, while “ISA-less” designs are not burdened with the complexity and cost of the ISA subsystem. For an implementation of an ISA design, contact external suppliers.

2.16. I/O APIC Design Recommendation

UP systems not using the integrated I/O APIC should comply with the following recommendations:

- On the ICH2
  - Connect PICCLK directly to ground.
  - Connect PICD0 and PICD1 to ground through a 10 kΩ resistor.
- On the processor
  - PICCLK must be connected from the clock generator to the PICCLK pin on the processor.
  - Connect PICD0 to 2.5 V through 10 kΩ resistors.
  - Connect PICD1 to 2.5 V through 10 kΩ resistors.

2.17. SMBus/SMLink Interface

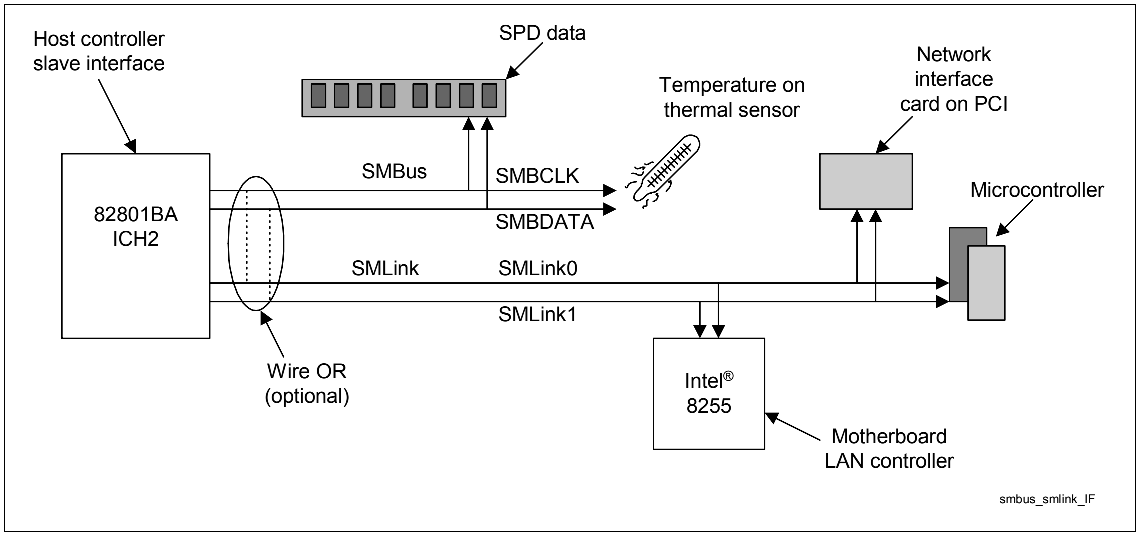
The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals (SMBCLK, SMBDATA) to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus host controller, which resides inside the ICH2. If the SMBus is used only for the Rambus SPD EEPROMs (one on each RIMM), both signals should be pulled up to 3.3. V with a 4.7 kΩ resistor.

The ICH2 incorporates a new SMLink interface supporting Alert on LAN (AOL), AOL2*, and slave functionality. It uses two signals (SMLINK[1:0]). SMLINK[0] corresponds to an SMBus clock signal, and SMLINK[1] corresponds to an SMBus data signal. These signals are part of the SMB slave interface.

For AOL functionality, the ICH2 transmits heartbeat and event messages over the interface. When the Intel 82562EM LAN connect component is used, the ICH2's integrated LAN controller will claim the SMLink heartbeat and event messages and will send them out over the network. An external, AOL2-enabled LAN controller (i.e., Intel 82550) connects to the SMLink signals, to receive heartbeat and event messages as well as to access the ICH2 SMBus slave interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus host controller and the SMBus slave interface obey the SMBus protocol, so the two interfaces can be externally wire-OR'd together, to allow an external management ASIC (e.g., Intel 82550) to access targets on the SMBus as well as the ICH2 slave interface. This is done by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA. See Figure 57. Since SMBus and SMLINK are pulled up to VCCSUS3_3, system designers must be sure to properly isolate any device that may be powered down while VCCSUS3_3 is still active (e.g., thermal sensors).

Figure 57. SMBUS/SMLink Interface



Note: Intel does not support external access to the ICH2's integrated LAN controller via the SMLink interface. Also, Intel does not support access to the ICH2's SMBus slave interface by the ICH2's SMBUS host controller.

The following table describes the pull-up requirements for different implementations of the SMBus and SMLink signals.

Table 20. Pull-Up Requirements for SMBus and SMLink Signals

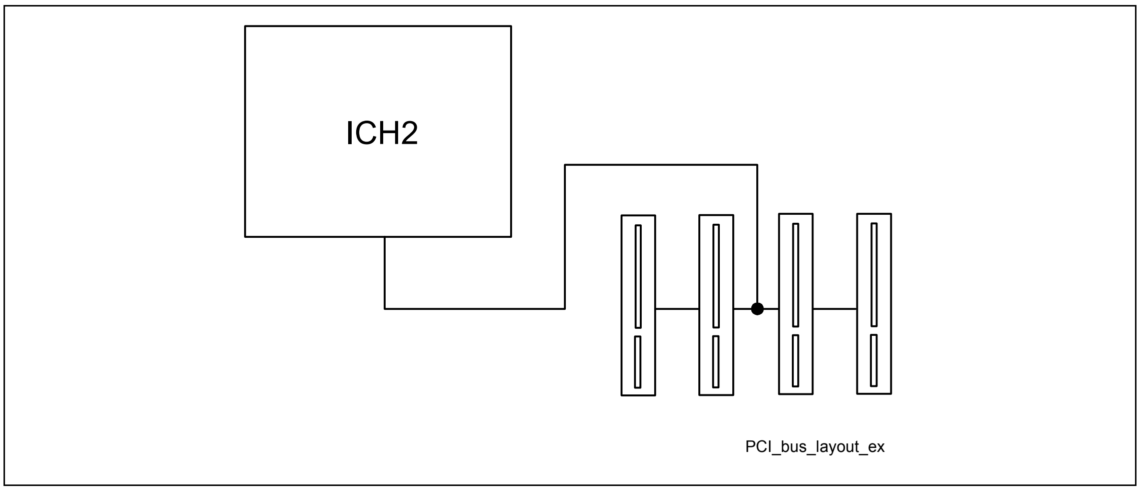
SMBus / SMLink Use	Implementation
Alert-on-LAN* signals	4.7 kΩ pull-up resistors to 3.3 V_{SB} are required.
GPIOs	Pull-up resistors to 3.3 V_{SB} and the signals must be allowed. To change states on power-up. (For example, during power-up the ICH2 will drive *heartbeat* messages until the BIOS programs these signals as GPIOs.) The values of the pull-up resistors depend on the loading on the GPIO signal.
Unused	4.7 kΩ pull-up resistors to 3.3 V_{SB} are required.

2.18. PCI

The ICH2 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification*, Revision 2.2. The implementation is optimized for high-performance data streaming when the ICH2 acts as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification*, Revision 2.2.

The ICH2 supports six PCI Bus masters, excluding the ICH2, by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 58. PCI Bus Layout Example



2.19. RTC

The ICH2 contains a real-time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping the date and time and storing system data in its RAM when the system is powered down.

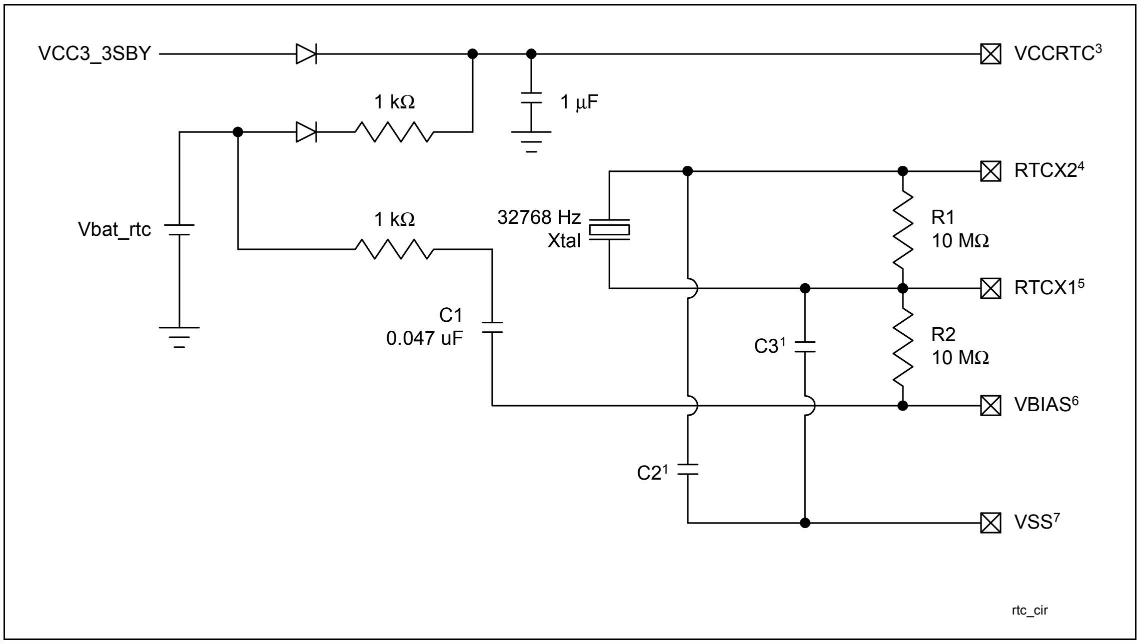
This section will discuss the recommended hookup for the RTC circuit for the ICH2.

Note: This circuit is not the same as the circuit used for the PIIX4.

2.19.1. RTC Crystal

The ICH2 RTC module requires an external 32.768 kHz oscillating source connected on the RTCX1 and RTCX2 pins. The following figure shows the external circuitry that comprises the oscillator of the ICH2 RTC.

Figure 59. External Circuitry for the ICH RTC[2]



NOTES:
1. The exact capacitor value must be based on the crystal maker's recommendation.
2. This circuit is not the same as the one used for PIIX4.
3. VCC_{RTC}: Power for RTC well
4. RTCX2: Crystal input 2 – Connected to the 32.768 kHz crystal
5. RTCX1: Crystal input 1 – Connected to the 32.768 kHz crystal
6. VBIAS: RTC bias voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
7. V_{SS}: Ground

2.19.2. External Capacitors

To maintain RTC accuracy, the external capacitor C1 must have a capacitance of 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (C_{LOAD}) for the crystal, when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

The following equation can be used to choose the external capacitance values (C2 and C3):

$$C_{LOAD} = (C2 \times C3) / (C2 + C3) + C_{PARASITIC}.$$

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

2.19.3. RTC Layout Considerations

- Minimize the RTC lead lengths. Approximately 0.25 inch is sufficient.
- Minimize the capacitance between Xin and Xout in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator V_{CC} should be clean. Use a filter (e.g., an RC low-pass) or a ferrite inductor.

2.19.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

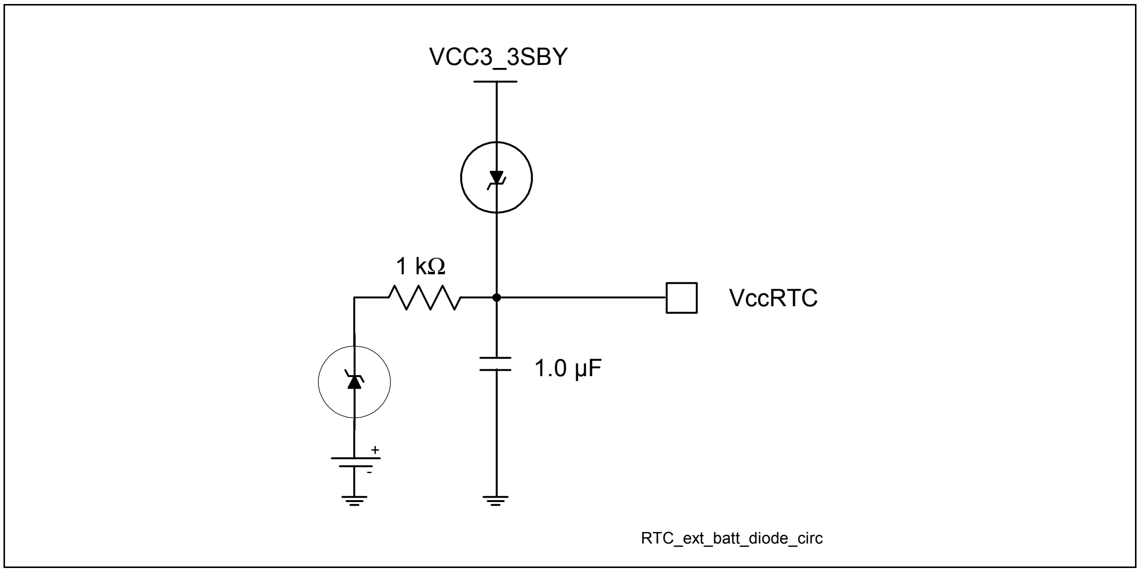
Example batteries are the Duracell* 2032, 2025 or 2016 (or equivalent), which provide many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

170,000 µAh / 3 µA = 56,666 h = 6.4 years

The battery voltage can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is within the range 3.0 V to 3.3 V.

The battery must be connected to the ICH2 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC well to be powered by the battery when system power is unavailable, but by system power when it is available. For this purpose, the diodes are set to be reverse-biased when system power is unavailable. The following figure is an example diode circuit.

Figure 60. Diode Circuit Connecting RTC External Battery

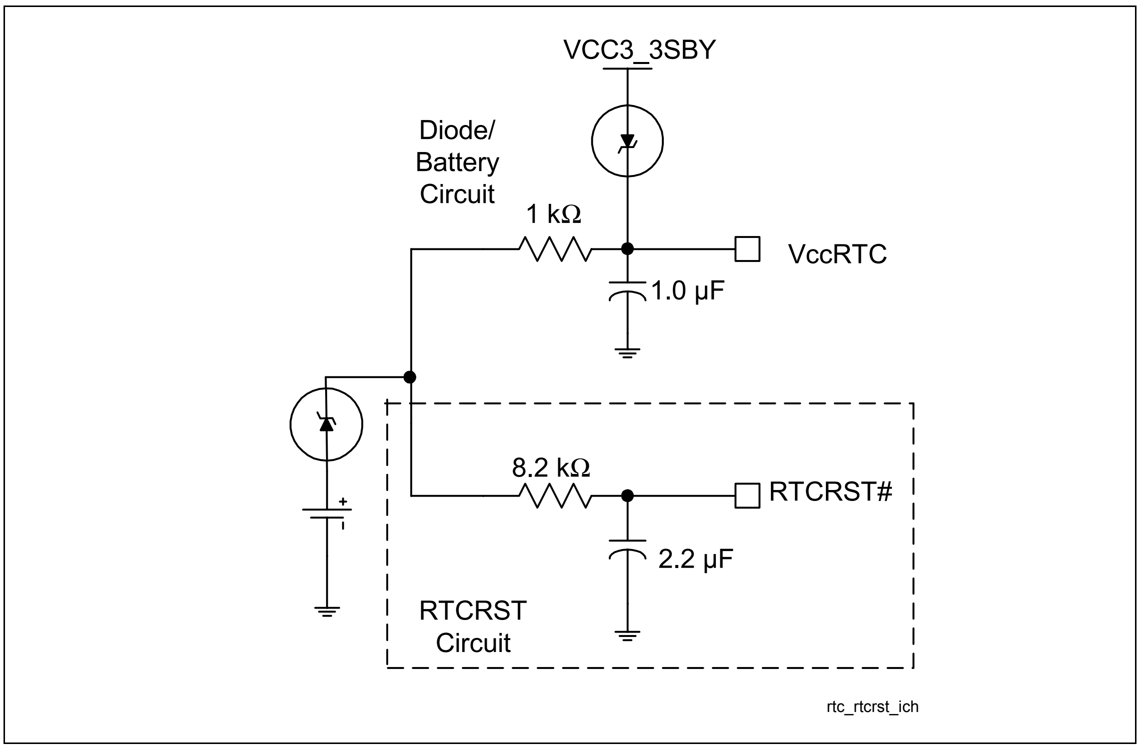


A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby increase the RTC accuracy.

2.19.5. RTC External RTCRST Circuit

The ICH2 RTC requires additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (V_{BAT}) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage becomes valid. The RC time delay should be within the range 10 ms–20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until cleared by software. As a result, when the system boots, the BIOS knows that the RTC battery has been removed.

Figure 61. RTCRST External Circuit for ICH2 RTC



This RTCRST# circuit is combined with the diode circuit (Figure 60. Diode Circuit Connecting RTC External Battery), which allows the RTC well to be powered by the battery when system power is unavailable. Figure 59 is an example of the circuit used in conjunction with the external diode circuit.

2.19.6. RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should be routed with trace lengths of less than 1 inch. The shorter, the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing. (Optimally, there would be a ground line between them.)
- Put a ground plane under all external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

2.19.7. VBIAS DC Voltage and Noise Measurements

- The steady-state VBIAS is a DC voltage of approximately 0.38 V ± 0.06 V.
- When the battery is inserted, the VBIAS is “kicked” to approximately 0.7 V–1.0 V, but it will return to its DC value within a few ms.
- Noise on VBIAS must be minimized at ≤200 mV.
- VBIAS is very sensitive and cannot be probed directly. It can be probed through a 0.01 µF capacitor.
- Excess noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize VBIAS noise, it is necessary to implement the routing guidelines described previously and the required external RTC circuitry.

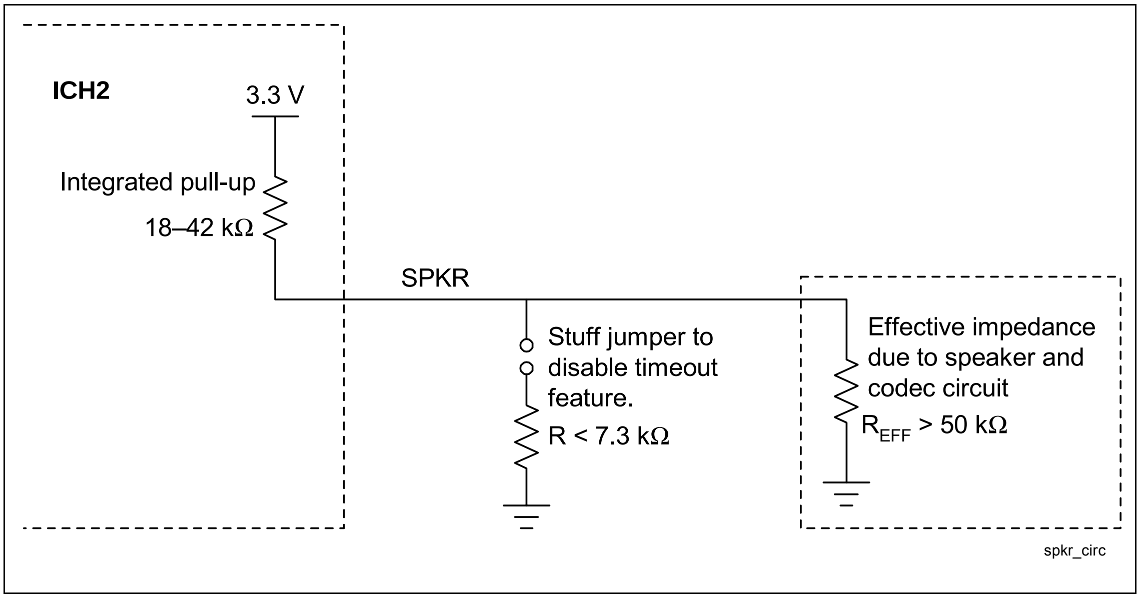
2.19.8. RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 61 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

2.20. SPKR Pin Consideration

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Otherwise, the TCO Timer Reboot function will be disabled erroneously. SPKR is used both as the output signal to the system speaker and as a functional strap. The strap function enables or disables the “TCO Timer Reboot function,” depending on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor when a TCO timer timeout occurs. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, offset D4h). The SPKR signal has a weak integrated pull-up resistor, which is enabled only during boot/reset. Therefore, its default state when the pin is a “no connect” is a logical one or enabled. To disable this feature, a jumper can be populated to pull the signal line low (see Figure 62). The value of the pull-down must be such that the voltage divider caused by the pull-down and integrated pull-up resistors will be read as a logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or less than that of the integrated pull-up resistor. Therefore, it is strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

Figure 62. SPKR Circuit



It should be noted that this is not the only solution to this problem. Board designers can also isolate the load from the SPKR pin until POWEROK is in a stable high state. This would allow a weak effective load to be implemented.

2.21. ICH2 PIRQ Routing

This section deals with the routing of the four added PCI IRQ signals implemented with the ICH2.

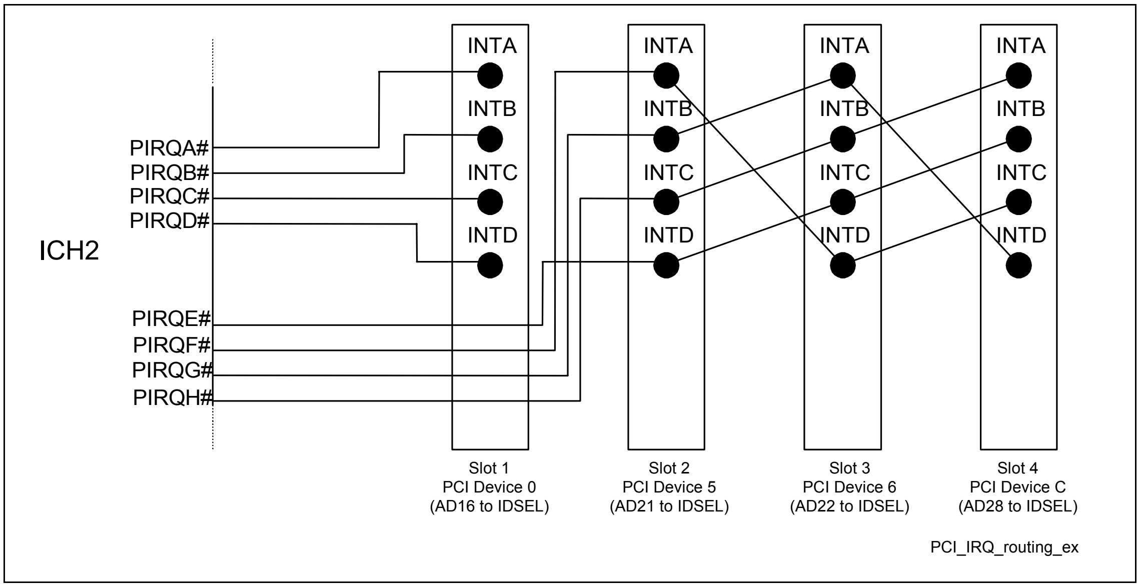
The PCI interrupt request signals E-H are new to the ICH2. These signals have been added to lower the latency caused by the presence of multiple devices on one interrupt line. These new signals allow each PCI slot to have an individual PCI interrupt request line, assuming that the system has four PCI slots. The following table shows how the ICH2 uses the PCI IRQ when the I/O APIC is active.

Table 21. Usage of I/O APIC Interrupt Inputs 16 through 23

No.	IOAPIC INTIN PIN	Function in ICH2 using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	
2	IOAPIC INTIN PIN 17 (PIRQB)	AC'97, modem and SMBUS
3	IOAPIC INTIN PIN 18 (PIRQC)	
4	IOAPIC INTIN PIN 19 (PIRQD)	USB controller 1
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN device
6	IOAPIC INTIN PIN 21 (PIRQF)	
7	IOAPIC INTIN PIN 22 (PIRQG)	
8	IOAPIC INTIN PIN 23 (PIRQH)	USB controller 2

Interrupts B, D, E, and H service devices internal to the ICH2. Interrupts A, C, F, and G are unused and can be used by PCI slots. The following figure shows an example of IRQ line routing to the PCI slots.

Figure 63. Example PCI IRQ Routing



The PCI IRQ routing in the previous figure allows the ICH2's internal functions to have a dedicated IRQ, assuming add-in cards are single-function devices and use INTA. If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI bus, the ICH2's internal functions will start sharing IRQs.

Figure 63 is one example. It is up to board designers to route these signals most efficiently for their particular systems. A PCI slot can be routed to share interrupts with any of the ICH2's internal device/functions.

2.22. LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components, depending on the target market. These guidelines use the Intel 82562ET to refer to both the Intel 82562ET and the Intel 82562EM. The Intel 82562EM is specified in those cases where there is a difference.

LAN Connect Component	Connection	Features
Intel 82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 connection
Intel 82562ET	10/100 Ethernet	Ethernet 10/100 connection
Intel 82562EH	1-Mbit HomePNA* LAN	1-Mbit HomePNA connection

Intel developed a dual footprint for the Intel 82562ET and Intel 82562EH components, to minimize the required number of board builds. A single layout with the specified dual footprint allows the OEM to install the LAN connect component appropriate for the market need. Design guidelines are provided for each required interface and connection. Refer to Figure 64 and Table 22 for the corresponding section of the design guide.

Figure 64. ICH2 / LAN Connect Section

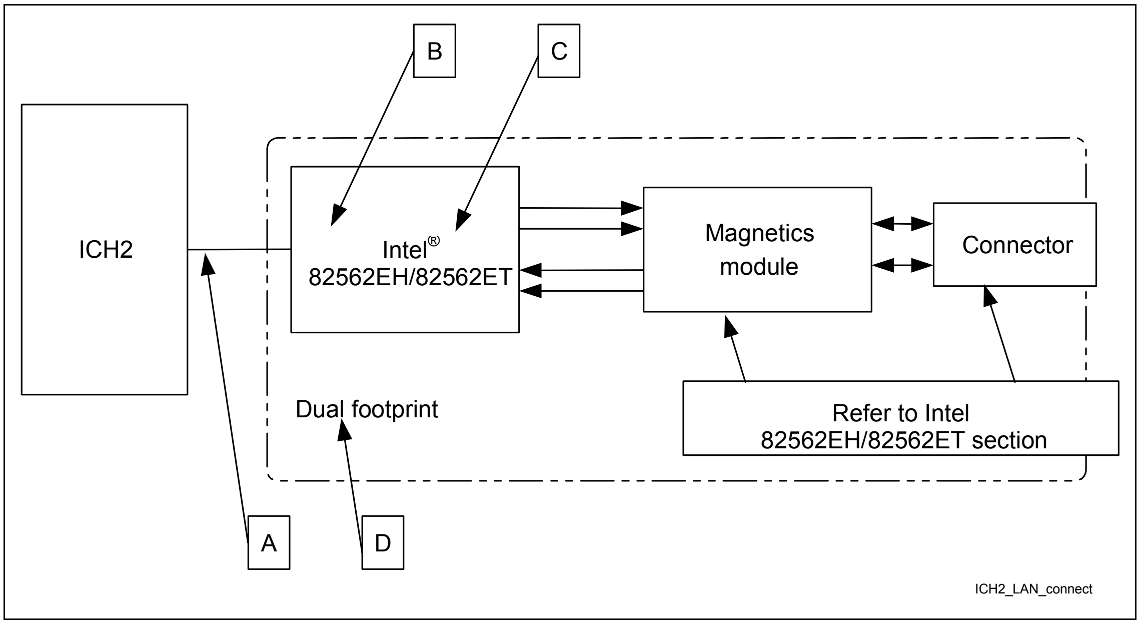


Table 22. LAN Design Guide Section Reference

Layout Section	Previous Figure Reference	Design Guide Section
ICH2 – LAN interconnect	A	2.22.1 ICH2 – LAN Interconnect Guidelines
General routing guidelines	B,C,D	2.22.2 General LAN Routing Guidelines and Considerations
Intel® 82562EH	B	Intel® 82562EH Home/PNA* Guidelines
Intel® 82562ET/82562EM	C	2.22.4 Intel® 82562ET / Intel® 82562EM Component Guidelines
Dual-footprint layout	D	Intel® 82562ET and Intel® 82562EH Components' Dual-Footprint Guidelines

2.22.1. ICH2 – LAN Interconnect Guidelines

This section contains guidelines for the design of motherboards and riser cards that comply with LAN connect. The guidelines should not be treated as a specification, and the system designer must ensure, via simulations or other techniques, that the system meets the specified timings. Special care must be taken when matching the *LAN_CLK* traces to those of the other signals, as discussed next. The following are guidelines for the ICH2-to-LAN component interface. The following signal lines are used on this interface: LAN_CLK, LAN_RSTSYNC, LAN_RXD[2:0], and LAN_TXD[2:0].

This interface supports both Intel 82562EH and Intel 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when the Intel 82562EH component is installed. The AC characteristics of this interface are discussed in the *Intel® 82801BA I/O Controller (ICH2) Datasheet*. Dual footprint guidelines are found in Section 2.22.6.

2.22.1.1. Bus Topologies

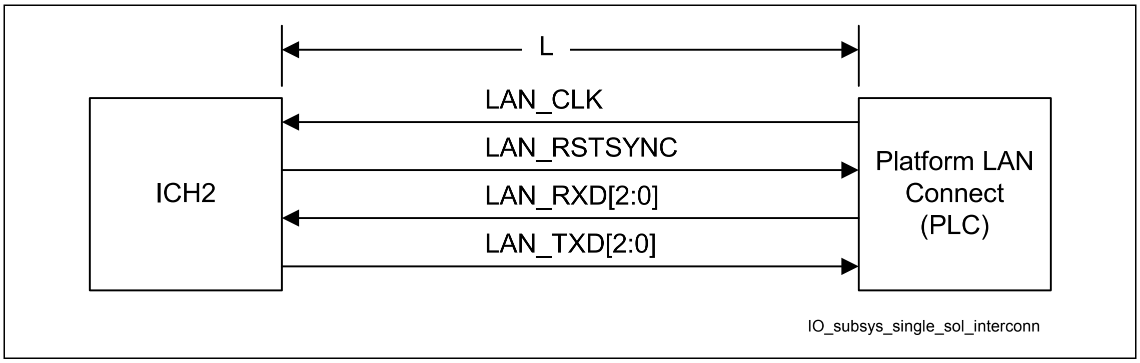
The LAN Connect Interface can be configured in several topologies, as follows:

- Direct point-to-point connection between the ICH2 and the LAN component
- Dual footprint (see Section 2.22.6.)
- LOM/CNR implementation

2.22.1.2. Point-to-Point Interconnect

The following are guidelines for a single-solution motherboard. Either the Intel 82562EH component, Intel 82562ET component or CNR is installed.

Figure 65. Single-Solution Interconnect



Length requirements for Figure 65:

Intel 82562EH: L = 4.5 inches to 10.0 inches (Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.)

Intel 82562ET: L = 3.5 inches to 10.0 inches

CNR*: L = 3.0 inches to 9.0 inches (0.5 inch to 3.0 inches on card)

2.22.1.3. LOM/CNR Interconnect

The following guidelines enable an all-inclusive motherboard solution. This layout combines the LOM, dual footprint, and CNR solutions. The resistor pack ensures that either a CNR option or a LAN-on-motherboard option can be implemented at one time. The following figures show a model of this. The recommended trace routing lengths are shown in Table 23.

Figure 66. LOM/CNR Interconnect

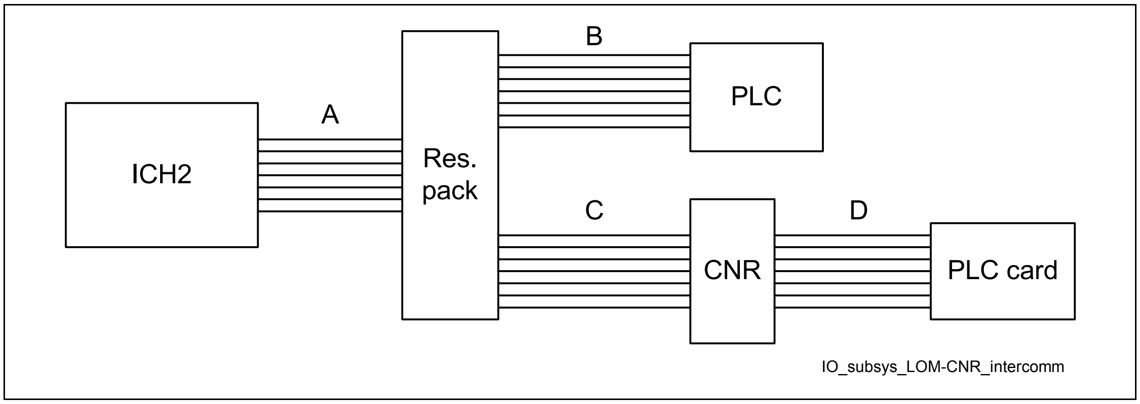


Table 23. Length Requirements for Figure 66

Configuration	A	B	C	D
Intel® 82562EH	0.5” to 6”	4” to (10” – A)		
Intel® 82562ET	0.5” to 7”	3” to (10” – A)		
Dual footprint	0.5” to 6.5”	3.5” to (10” – A)		
Intel® 82562ET/EH card (see Note)	0.5” to 6.5”		2.5” to (9” – A)	0.5” to 3”

Note: The total trace length should not exceed 13 inches.

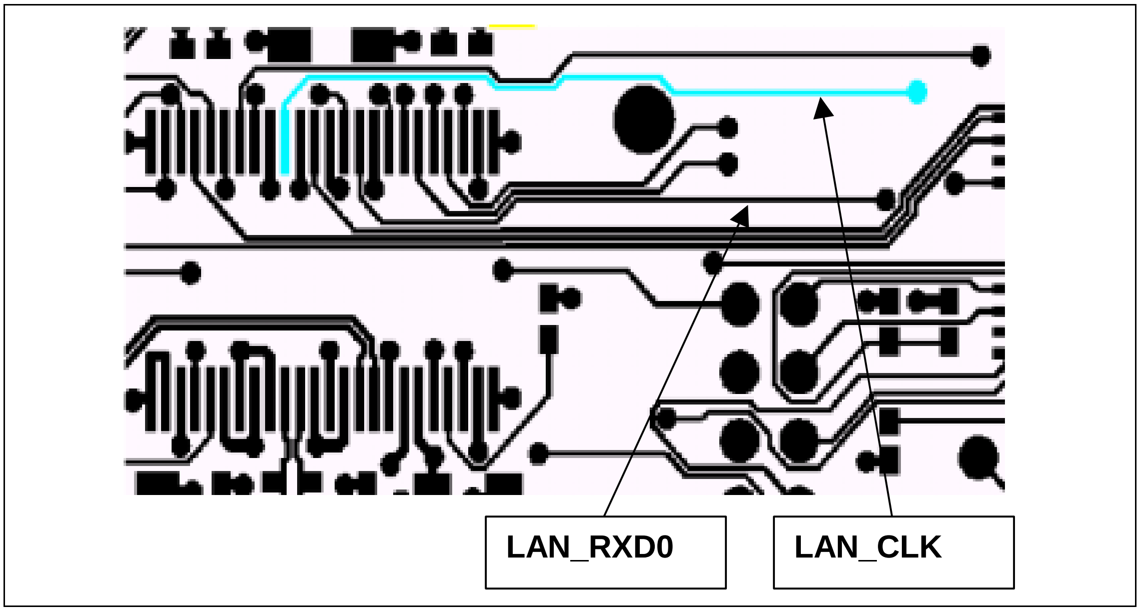
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω or 22 Ω.
- LAN-on-motherboard PLC can have a dual-footprint configuration.

2.22.1.4. Signal Routing and Layout

LAN connect signals must be carefully routed on the motherboard, to meet the timing and signal quality requirements of this interface specification. The following are general guidelines that should be followed. It is recommended that the board designer simulate the board routing, to verify that the specifications are met for flight times and skews resulting from trace mismatch and crosstalk. On the motherboard, the length of each data trace is either equal to or up to 0.5 inch shorter than the *LAN_CLK* trace. (*LAN_CLK* should always be the longest motherboard trace in each group.) See Figure 67.

Figure 67. LAN_CLK Routing Example



2.22.1.5. Crosstalk Consideration

Crosstalk-induced noise must be carefully minimized. Crosstalk is the principal cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

2.22.1.6. Impedances

Motherboard impedances should be controlled to minimize the effect of any mismatch between the motherboard and an add-in card. An impedance of 60 Ω ± 15% is strongly recommended. Otherwise, the signal integrity requirements may be violated.

2.22.1.7. Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew rate-controlled output buffers provide acceptable signal integrity by controlling signal reflection, overshoot/undershoot, and ringback. A 33-Ω series resistor can be installed at the driver side of the interface, if the developer has concerns about overshoot/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

2.22.2. General LAN Routing Guidelines and Considerations

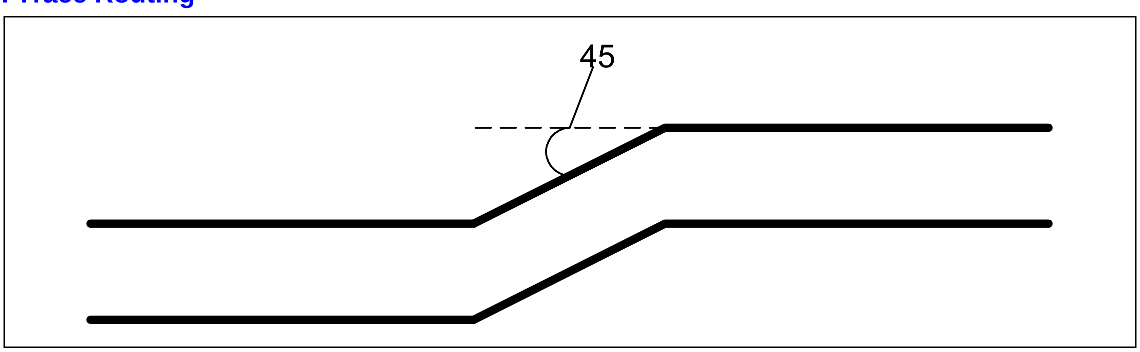
2.22.2.1. General Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on board sections where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through the power and ground planes.

Comply with the following suggestions, to help optimize board performance:

- The maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inch.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. (Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.)
- Do not route the transmit differential traces closer than 100 mils from the receive differential traces.
- Do not route any other signal trace both parallel to the differential traces and closer than 100 mils from the differential traces (300 mils recommended).
- Keep the maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be minimized. If a 90° bend is required, two 45° bends should be used instead. Refer to Figure 68.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane, rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures, at a distance greater than the largest aperture dimension.

Figure 68. Trace Routing



2.22.2.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, high-speed signals and signal layers close to a ground or power plane should be as short and wide as practical. Ideally, this ratio of trace width to height above ground plane should be between 1:1 and 3:1. To maintain trace impedance, the trace width should be modified when changing from one board layer to another, if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled at approximately 100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 0.030 inch (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long-and-thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

2.22.2.1.2. Signal Isolation

Signal isolation rules include the following:

- If possible, separate and group signals by function on separate layers. Maintain a gap of 100 mils between all differential pairs (phone line and Ethernet) and other nets, but group associated differential pairs. Note: Over the length of a trace run, each differential pair should be at least 0.3 inch from any parallel signal trace.
- Physically group all components associated with one clock trace, to reduce the trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN or phone line traces near other high-frequency signals associated with a video controller, cache controller, processor or similar device.

2.22.2.2. Power and Ground Connections

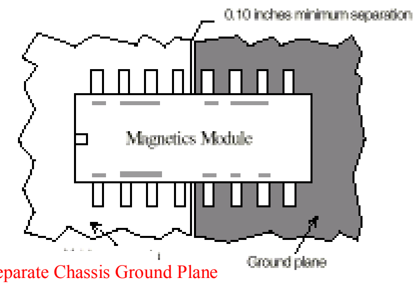
Rules and guidelines for power and ground connections include the following:

- All V_{CC} pins should be connected to the same power supply.
- All V_{SS} pins should be connected to the same ground plane.
- Four to six decoupling capacitors, including two 4.7 µF capacitors are recommended.
- Place decoupling as close as possible to power pins.

2.22.2.2.1. General Power and Ground Plane Considerations

To properly implement the common-mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be physically separated from the digital or input ground (primary side) by at least 100 mils.

Figure 69. Ground Plane Separation



Good grounding requires the minimization of inductance levels in the interconnections. EMI radiation can be reduced significantly by keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return.

Rules that help reduce backplane and motherboard circuit inductance include the following:

- Route traces over a continuous plane with no interruptions (i.e., don't route over a split plane). If there is a vacant area on a ground or power plane, avoid routing signals over it. This would increase inductance and EMI radiation levels.
- To reduce coupling, separate noisy digital grounds from analog grounds. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times whenever possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have a chassis ground beneath it. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer. There should not be a power plane under the magnetics module.
- Create a spark gap between pins 2 through 5 of the phone line connector(s) and a shield ground of 1.6 mm (59.0 mil). This requirement is critical to passing the FCC Part 68 test for a phone line connection. Note: For world-wide certification, a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6 mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

2.22.2.3. 4-Layer Board Design

Top-Layer Routing

Sensitive analog signals are routed completely on the top layer without the use of vias. This allows tight control of signal integrity and removes any impedance inconsistencies due to layer changes.

Ground Plane

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended.

Power Plane

Physically separate digital and analog power planes must be provided to prevent digital switching noise from being coupled into the analog power supply plane's VDD_A. Analog power may be a metal fill "island," separated from digital power, and better filtered than digital power.

Bottom Layer Routing

The digital high-speed signals, which include all LAN interconnect interface signals, are routed on the bottom layer.

Common Physical Layout Issues

The most common physical layer design and layout mistakes in LAN-on-motherboard designs are as follows:

1. **Unequal length of the two traces within a differential pair**. Inequalities create common-mode noise which will distort the transmit or receive waveforms.
2. **Lack of symmetry between the two traces within a differential pair**. (For each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. **Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector**. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. If they are long, traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, longer traces will increase the impedance mismatch (see mistake 9). The magnetics should be as close to the connector as possible (<= 1 inch).
4. **Routing any other trace parallel to and close to one of the differential traces**. Crosstalk on the receive channel will degrade the long-cable BER. Crosstalk on the transmit channel can cause excessive emissions—resulting in FCC test failure—and can result in a low transmission BER on long cables. Other signals should be kept at least 0.3 inch from the differential traces.
5. **Routing the transmit differential traces next to the receive differential traces**. The transmit trace closest to a receive trace will induce more crosstalk on the closest receive trace, and it can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces

should be kept at least 0.3 inch from the nearest receive trace. Possible exceptions are only where the traces enter or exit the magnetics, the RJ-45/11, and the PLC.

6. **Use of an inferior magnetics module**. The magnetics modules used by Intel have been fully tested for IEEE PLC conformance, for long-cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no autotransformer in the transmit channel.)

7. **Using an Intel® 82555 or Intel® 82558 component's physical layer schematic in a PLC design**. The transmit terminations and decoupling are different and there also are differences in the receive circuit. Please use the appropriate reference schematic or Application Notes.

8. **Failure to use (or incorrect use of) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules**. Unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper-value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (i.e., FCC) problems, IEEE conformance issues, and long-cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for unused RJ pins and the magnetics center-taps.

9. **Incorrect differential trace impedances**. It is important to have an approximately 100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs with differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close to each other (see Note), the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. A 10 Ω to 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. **Use of an excessively large capacitor between the transmit traces and/or excessive capacitance from the magnetics' transmit center-tap (on the Intel 82562ET component's side of the magnetics) to ground**. The use of capacitors with capacitances of more than a few pF in either of these locations can slow the 100 Mbps rise and fall time to such a degree that they fail the IEEE rise time and fall time specs, will cause the return loss to fail at higher frequencies, and will degrade the transmit BER performance. Caution is required if a cap is put in either of these locations. If a cap is used, it almost certainly should have a capacitance below 22 pF. (6 pF to 12 pF values have been used in past designs with reasonably good success.) Unless there is some overshoot in the 100 Mbps mode, these caps are unnecessary.

Note: It is important to keep the two traces within a differential pair close to each other, which increases their immunity to crosstalk and other sources of common-mode noise. Keeping them close means lower emissions (i.e., FCC compliance) from the transmit traces as well as an improved receive BER for the receive traces. Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inches trace-to-trace spacing is recommended.

2.22.3. Intel® 82562EH Home/PNA* Guidelines

Table 24. Related Documents

Title	Doc #
Intel® 82562EH HomePNA 1-Mbit/s Physical Layer Interface Product Preview Datasheet	OR-2183
RS-82562EH 1-Mbit/s Home PNA LAN Connect Option Application Note	OR-2182

For correct LAN performance, designers must follow the general guidelines outlined in Section 2.22.2. Additional guidelines for implementing an Intel 82562EH Home/PNA* LAN connect component are provided in the following sections.

2.22.3.1. Power and Ground Connections

Power and ground connection rules include the following:

- For optimal performance, place decoupling capacitors on the backside of the PCB, directly under the Intel 82562EH component, with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for the Intel 82562EH (V_{CCA}, V_{SSA}) should be isolated from the digital V_{CC} and V_{SS} through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between V_{CC} and V_{SS} as well as V_{CCA} and V_{SSA} power supplies.

2.22.3.2. Guidelines for Intel® 82562EH Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section discusses guidelines for component placement.

Careful component placement provides the following benefits:

- Decreases potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC specifications
- Simplifies the task of routing traces. To some extent, component orientation affects the trace routing complexity. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the HomePNA LAN interface because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA LAN circuits must be as close as possible to the connector. Thus, all designs must be optimized to fit in a very small space.

2.22.3.3. Crystals and Oscillators

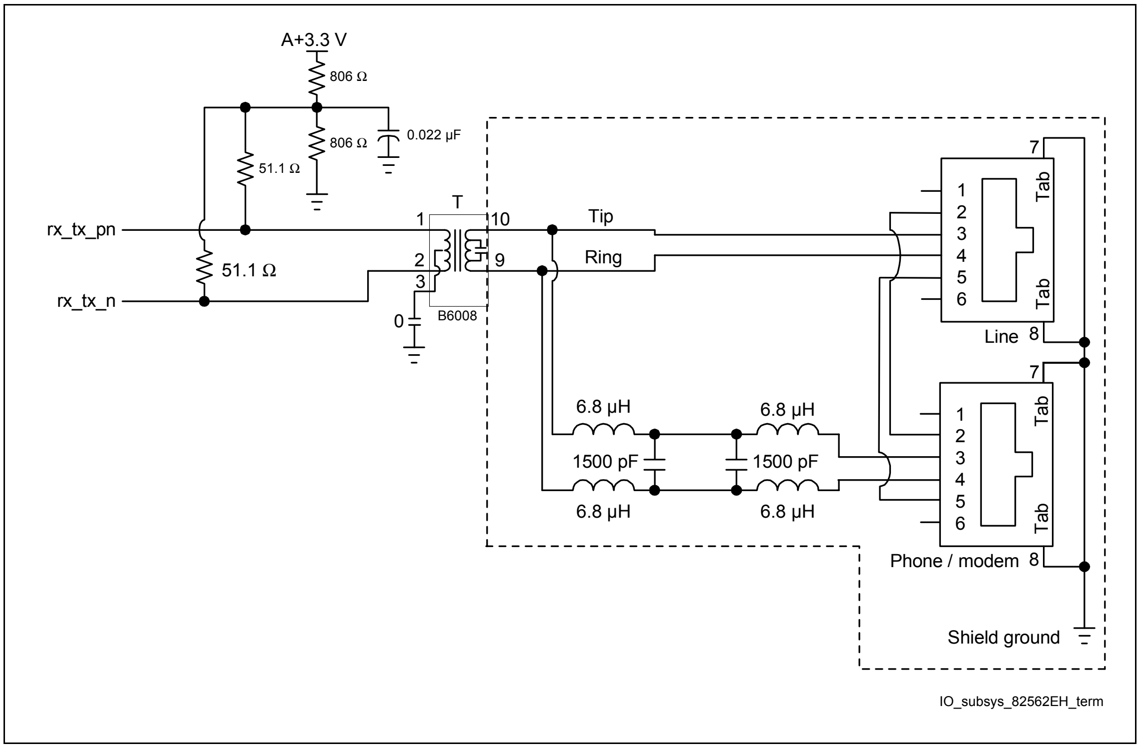
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the HomePNA magnetics module, to prevent communication interference. The crystal's retaining straps (if they exist) should be grounded to prevent possible radiation from the crystal case, and the crystal should lie flat against the PC board, to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discretes as close as possible to the Intel 82562EH component, keeping the length as short as possible. Do not route any noisy signals in this area.

2.22.3.4. Phoneline HPNA Termination

The transmit/receive differential-signal pair is terminated with a pair of 51.1 Ω (1%) resistors. This parallel termination should be placed close to the Intel 82562EH component. The center, common point between the 51.1 Ω resistors is connected to a voltage divider network. The opposite end of one, 806 Ω resistor is tied to VCCA (3.3V), and the opposite end of the other 806 Ω resistor and the cap are connected to ground. The termination is shown in the following figure.

Figure 70. Intel® 82562EH Component Termination



The filter and magnetics component T integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA LAN interface.

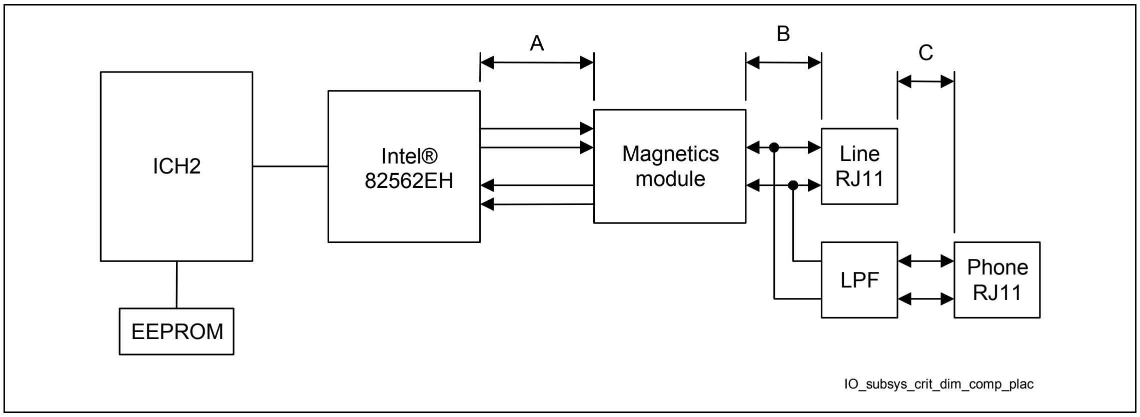
One RJ-11 jack (labeled LINE in the previous figure) allows the node to be connected to the phone line, and the second jack (labeled PHONE in the previous figure) allows other down-line devices to be connected at the same time. This second connector is not required by the HomePNA. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter set up in line with the second RJ-11 jack also is recommended by the HomePNA, to minimize interference between the HomeRun connection and a POTS voice or modem connection on the second jack. This restricts the type of devices connected to the second jack, because the pass-band of this filter is set at approximately 1.1 MHz. Please refer to the HomePNA website (www.homepna.org) for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA certifications.

2.22.3.5. Critical Dimensions

As shown in the following figure, there are three dimensions to consider during layout: Distance B, from the line RJ11 connector to the magnetics module; distance C, from the phone RJ11 to the LPF (if implemented); and distance A, from the Intel 82562EH component to the magnetics module.

Figure 71. Critical Dimensions for Component Placement



Distance	Priority	Guideline
B	1	<1 inch
A	2	<1 inch
C	3	<1 inch

2.22.3.5.1. Distance from Magnetics Module to Line RJ11

Distance B should be given highest priority and should be less then 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetry and unequal length in differential pairs contribute to common-mode noise. This can degrade the receive-circuit performance and contribute to radiated emissions from the transmit side.

2.22.3.5.2. Distance from Intel® 82562EH Component to Magnetics Module

Due to the high speed of signals present, distance 'A' between the Intel 82562EH component and the magnetics also should be less than 1 inch, but it should be second priority relative to the distance from the connects to the magnetics module.

In general, any trace section intended for use with high-speed signals should comply with the proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between devices and trace routes. A signal's reflection may contain a high-frequency component that may contribute more EMI than the original signal itself.

2.22.3.5.3. Distance from LPF to Phone RJ11

Distance 'C' should be less than 1 inch. Regarding trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetry and unequal length in the differential pairs contribute to common-mode noise. This can degrade the receive-circuit performance and contribute to radiated emissions from the transmit side.

2.22.4. Intel® 82562ET / Intel® 82562EM Component Guidelines

Related document are as follows:

- Intel® 82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Preview Datasheet (Order# OR-2106).
- Intel® 82562ET Platform LAN Connect (PLC) Networking Silicon Advance Information Datasheet (released).
- Intel® 82562EM Platform LAN Connect (PLC) Networking Silicon Advance Information Datasheet (released).
- Intel® 82562ET LAN on Motherboard Design Guide (AP-414): OR-2336
- Intel® 82562ET/EM PCB Design Platform LAN Connect (AP-412): OR-2059.
- CNR Reference Design Application Note (AP-418): OR-2281.

For correct LAN performance, designers must comply with the general guidelines outlined in Section 2.22.2. Additional guidelines for implementing an Intel 82562ET or Intel 82562EM LAN connect component are as follows:

2.22.4.1. Guidelines for Intel® 82562ET / Intel® 82562EM Component Placement

Component placement can affect the signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement has the following benefits:

- Decreases potential problems directly related to electromagnetic interference (EMI), which could result in failure to meet FCC and IEEE test specifications.
- Simplifies the task of routing traces. To some extent, component orientation affects the trace routing complexity. The overall objective is to minimize turns and crossovers between traces.

It is important to minimize the space needed for the Ethernet LAN interface, because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, all designs must be optimized to fit in a very small space.

2.22.4.2. Crystals and Oscillators

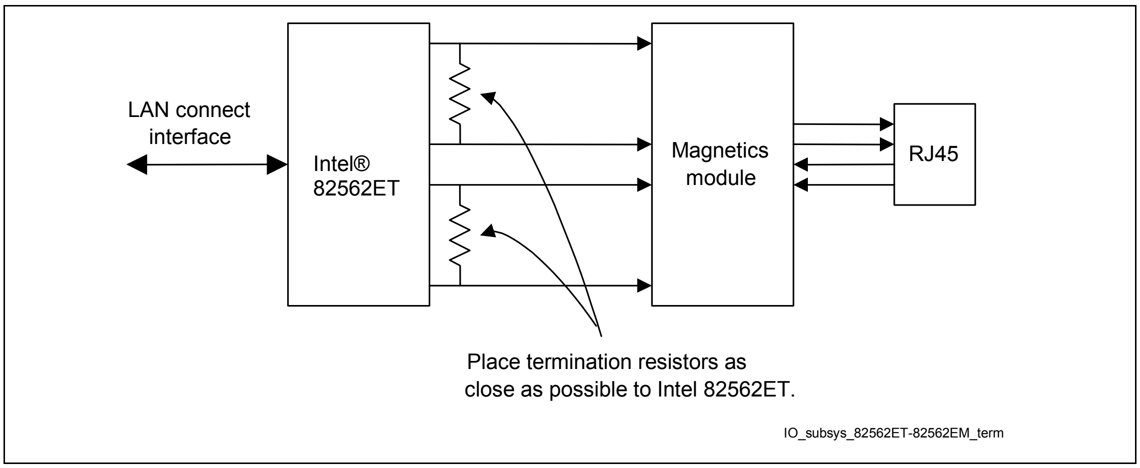
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals also should be kept away from the Ethernet magnetics module, to prevent communication interference. The crystal's retaining straps (if they exist) should be grounded to prevent possible radiation from the crystal case, and the crystal should lie flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For noise-free and stable operation, place the crystal and associated discretes as close as possible to the Intel 82562ET or Intel 82562EM component, keeping the trace length as short as possible. Do not route any noisy signals in this area.

2.22.4.3. Intel® 82562ET / Intel® 82562EM Component Termination Resistors

The 120 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 100 Ω (1%) receive differential pairs (RDP/RDN) should be placed as close as possible to the LAN connect component (Intel 82562ET or Intel 82562EM component). The reason is that these resistors terminate the entire impedance seen at the termination source (i.e., Intel 82562ET component), including the wire impedance reflected through the transformer.

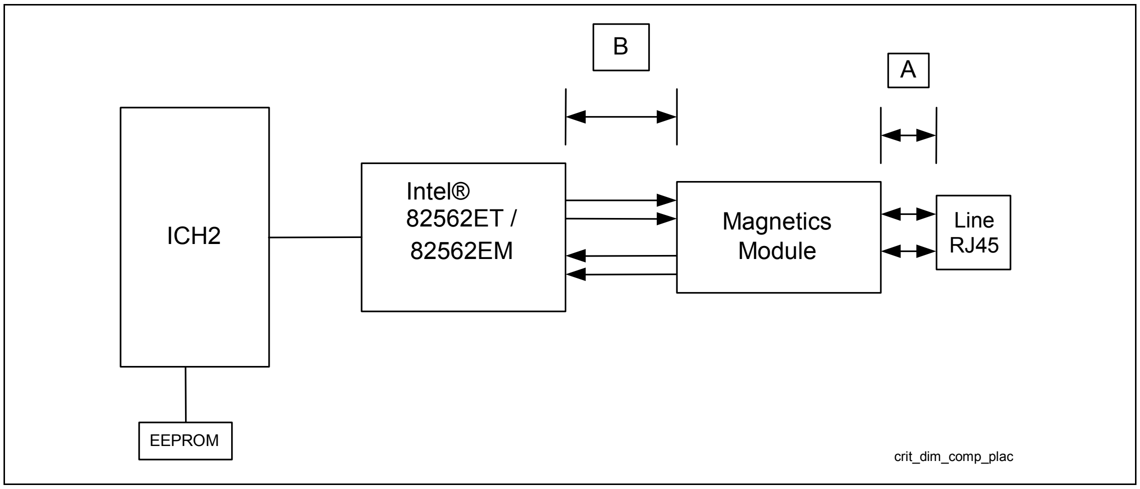
Figure 72. Intel® 82562ET/82562EM Component Termination



2.22.4.4. Critical Dimensions

As shown in Figure 73, two dimensions must be considered during layout: distance 'B' from the line RJ45 connector to the magnetics module, and distance 'A' from the Intel 82562ET or Intel 82562EM component to the magnetics module.

Figure 73. Critical Dimensions for Component Placement



Distance	Priority	Guideline
A	1	<1 inch
B	2	<1 inch

2.22.4.4.1. Distance from Magnetics Module to RJ45

Distance 'A,' in the previous figure, should be given the highest priority during board layout. The separation between the magnetics module and the RJ45 connector should be kept to less than 1 inch. The following trace characteristics are important and should be observed:

- Differential impedance: The differential impedance should be 100 Ω. The single-ended trace impedance is approximately 50 Ω. However, the differential impedance also can be affected by the spacing between traces.
- Trace symmetry: Differential pairs (e.g., TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (e.g., width).

Caution: Asymmetric and unequal-length traces in the differential pairs contribute to common-mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the Intel 82562ET component must be placed farther than a couple of inches from the RJ45 connector, distance B can be sacrificed. It should be a priority to minimize the total distance between the Intel 82562ET component and RJ-45.

Note: The measured trace impedance for layout designs targeting 100 Ω often yields a lower actual impedance. OEMs should verify the actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω–110 Ω should compensate for second-order effects.

2.22.4.4.2. Distance from the Intel® 82562ET Component to the Magnetics Module

Distance ‘B’ in Figure 73 also should be designed to be less than 1 inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be observed closely. Generally speaking, any trace section intended for use with high-speed signals should comply with proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between a device and the traces. Reflected signals may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed with a 100 Ω differential value. These traces also should be symmetric and of equal length within each differential pair.

2.22.4.5. Reducing Circuit Inductance

The following guidelines explain how to reduce circuit inductance in both backplanes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross them. This increases inductance and associated radiated-noise levels. To reduce coupling, noisy logic grounds should be separated from analog signal grounds. Noisy logic grounds sometimes can affect sensitive DC subsystems, such as analog-to-digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane. Similarly, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. It also is recommended to physically locate grounds so as to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high-frequency harmonics, significant radiation can result. The most-sensitive signal returns closest to the chassis ground should be connected. This results in a smaller loop area and reduces the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

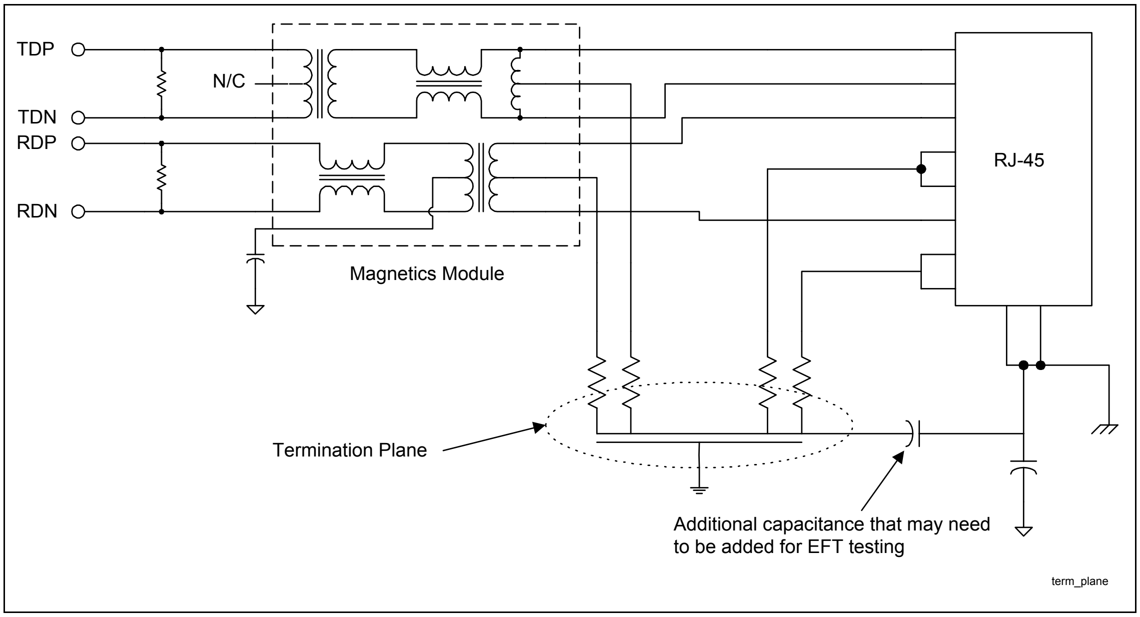
2.22.4.6. Terminating Unused Connections

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, grounding may be to the chassis ground, signal ground or a termination plane. Care must be taken when using various grounding methods, to insure that emission requirements are met. The method most often implemented is use of a floating termination plane, which is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. The stray energy on unused pins is then carried to the plane.

2.22.4.6.1. Termination Plane Capacitance

The recommended minimum termination plane capacitance is 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN), from the unused pairs of the RJ45. Pads may be placed for additional capacitance to chassis ground, which may be required if the termplane capacitance is not high enough to pass EFT (Electrical Fast Transient) testing. To meet EFT requirements, used discrete capacitors should be rated at 1000 V_{AC} minimum.

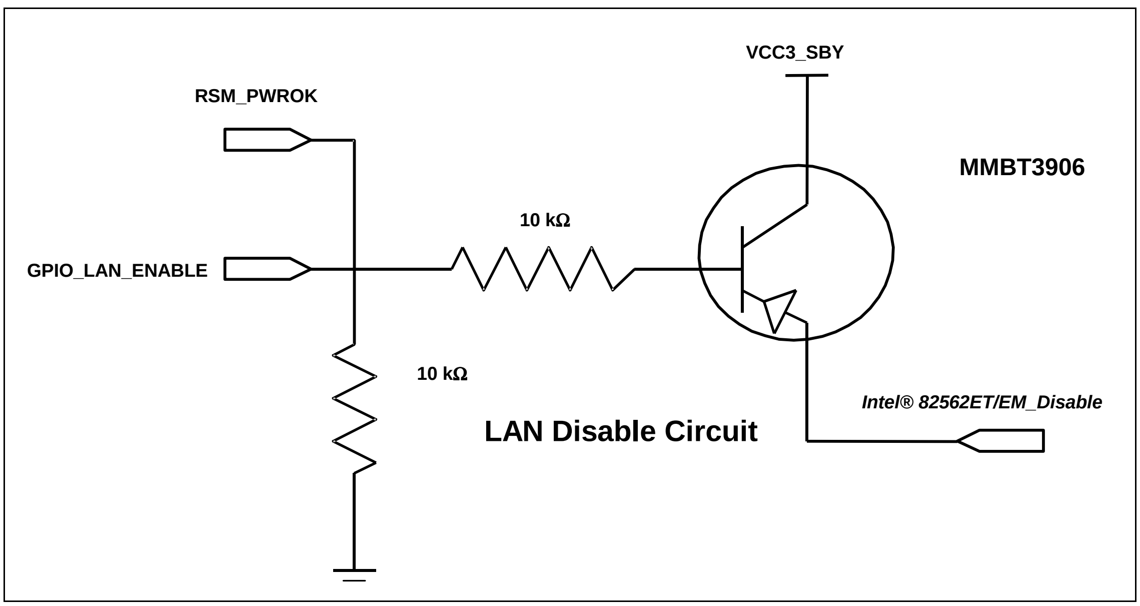
Figure 74. Termination Plane



2.22.5. Intel® 82562ET/EM Disable Guidelines

To disable the Intel 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. BIOS by controlling the GPIO can disable the LAN microcontroller.

Figure 75. Intel® 82562ET/EM Disable Circuit



There are four pins which are used to put the Intel 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node "82652ET/EH_Disable" of the disable circuit.

2.22.6. Intel® 82562ET and Intel® 82562EH Components' Dual-Footprint Guidelines

These guidelines explain the proper layout for a dual-footprint solution. This configuration allows the developer to install either the Intel 82562EH or Intel 82562ET/82562EM component, with only one motherboard design. The following guidelines are for the Intel 82562ET/82562EH components' dual-footprint option. The guidelines called out in Sections 2.22.1 and 2.22.4 apply to this configuration. The dual footprint for this particular solution uses a SSOP footprint for the Intel 82562ET component and a TQFP footprint for the Intel 82562EH component. The combined footprint for this configuration is shown in Figure 76 and Figure 77.

Figure 76. Dual-Footprint LAN Connect Interface

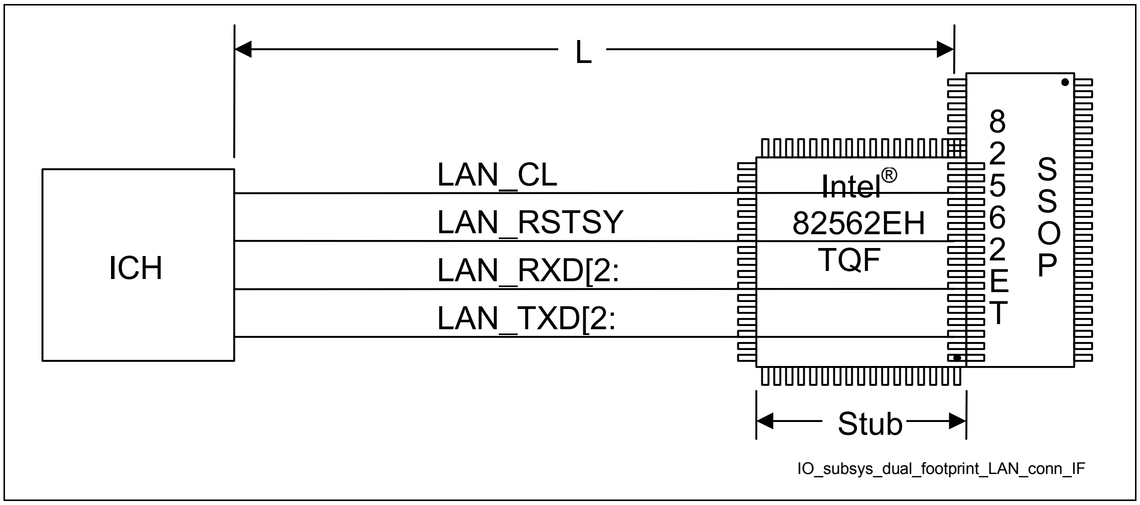
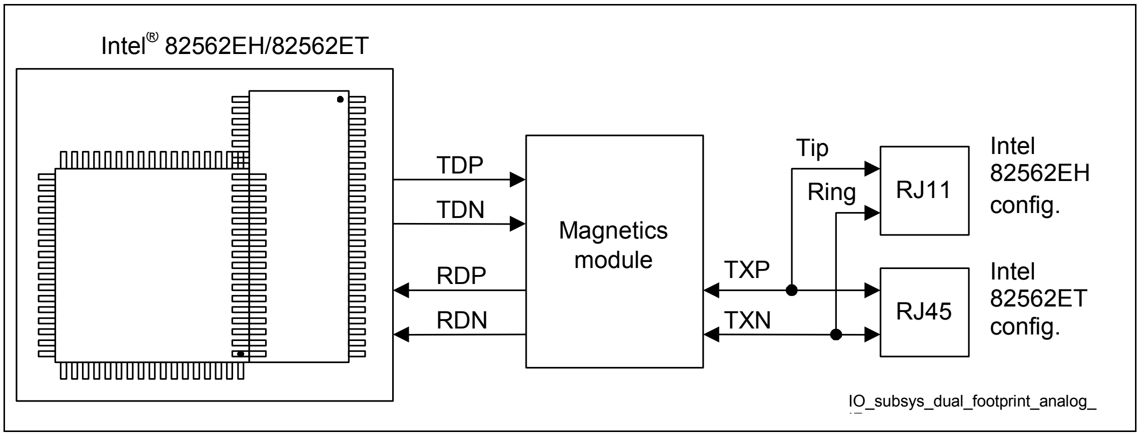


Figure 77. Dual-Footprint Analog Interface



Additional guidelines for this configuration are as follows:

- L = 0.5 inch to 6.5 inches
- Stub = <0.5 inch
- Either the Intel 82562EH or Intel 82562ET/82562EM component can be installed. Not both.
- Pins 28, 29, and 30 of the Intel 82562ET component overlap pins 17, 18, and 19 of the Intel 82562EH component.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip are shared by the Intel 82562EH and Intel 82562ET component configurations.
- No stubs should be present when the Intel 82562ET component is installed.
- The packages used for the dual footprint are the TQFP for the Intel 82562EH component and the SSOP for the Intel 82562ET component.
- A 22 Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistors should be placed as close as possible to components.
- Use components that can satisfy both the Intel 82562ET and Intel 82562EH component configurations (i.e., a magnetics module).
- Install components for either the Intel 82562ET or Intel 82562EH component configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are minimized.
- Stubs may occur on shared signal lines (i.e., RDP and RDN). These stubs result from traces routed to an uninstalled component.
- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Refer to the Intel 820E CRB layout for routing examples.

- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

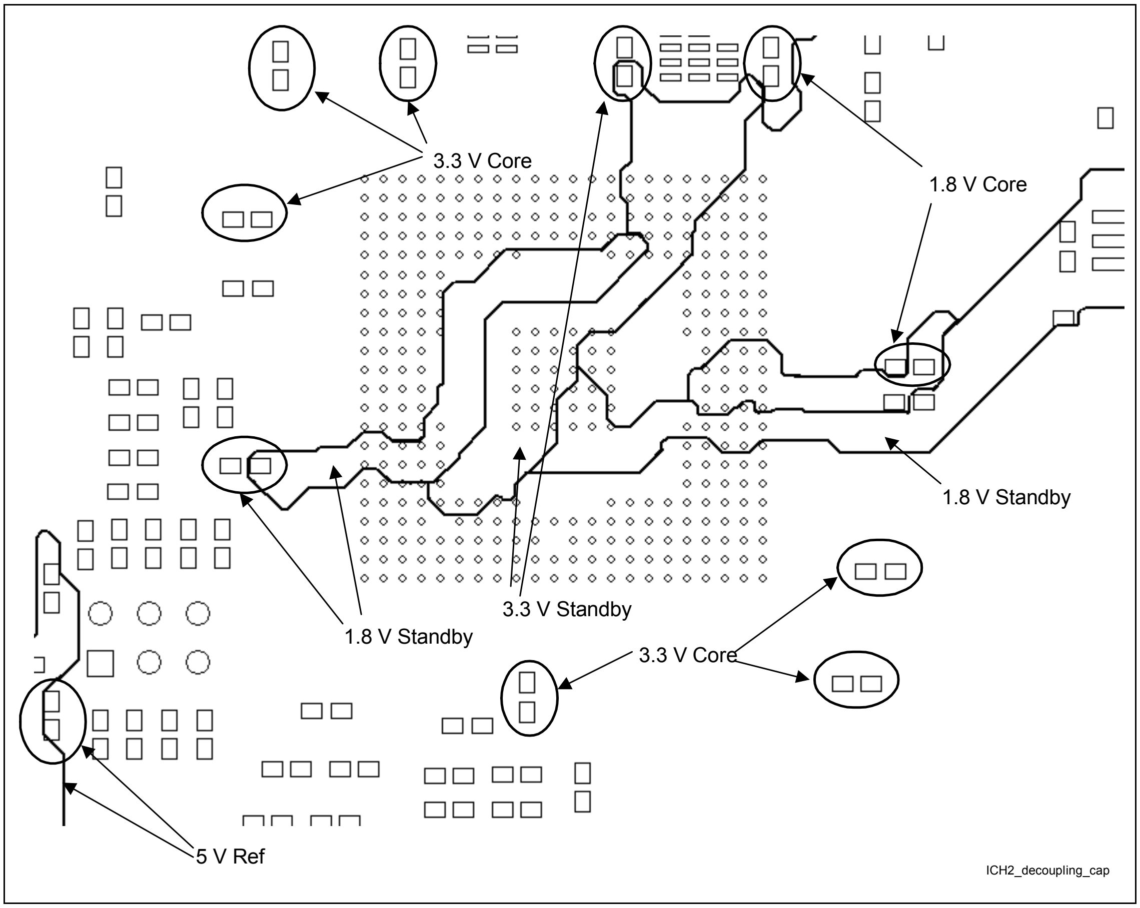
2.22.7. ICH2 Decoupling Recommendations

The ICH2 can generate large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below the specified limits. To avoid such a situation, ensure that the appropriate amount of bulk capacitance is added in parallel with the voltage input pins. It is recommended that the developer use the number of decoupling capacitors specified in the following table, to ensure that the component maintains stable supply voltages. The capacitors should be placed as close as possible to the package. Refer to Figure 78 for a layout example. For prototype board designs, it is recommended that the designer include pads for extra power plane decoupling caps.

Table 25. Decoupling Capacitor Recommendation

Power Plane/Pins	# Decoupling Capacitors	Capacitor Value (µF)
3.3 V core	6	0.1
3.3 V standby	1	0.1
processor I/F (1.3 – 2.5 V)	1	0.1
1.8 V core	2	0.1
1.8 V standby	1	0.1
5 V reference	1	0.1
5 V reference standby	1	0.1

Figure 78. Decoupling Capacitor Layout



The previous figure shows the layout of the ICH2 decoupling capacitors for various power planes around the ICH2. The decoupling caps are circled, with an arrow pointing to the power plane/trace to which they are connected.

2.23. FWH Flash BIOS Guidelines

The general compatibility guidelines and the design recommendations for supporting the FWH Flash BIOS device are discussed next. Most changes will be incorporated into the BIOS. Refer to the FWH Flash BIOS specification or equivalent.

2.23.1. In-Circuit FWH Flash BIOS Programming

All cycles destined for the FWH Flash BIOS appear on PCI. The ICH2 hub interface-to-PCI bridge puts all processor boot cycles out on the PCI (before sending them out on the FWH Flash BIOS interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive-decode agent out on the PCI. This enables booting from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH2 in the subtractive-decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, two devices will positively decode the same cycle. In systems with a PCI-to-ISA bridge, it also is necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot from a ROM behind a PCI-to-ISA bridge. After booting from the PCI card, it is possible to program the FWH Flash BIOS in circuit and program the ICH2 CMOS.

2.23.2. FWH Flash BIOS VPP Design Guidelines

The VPP pin on the FWH Flash BIOS is used for programming the flash cells. The FWH Flash BIOS supports a VPP of 3.3 V or 12 V. If VPP is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH Flash BIOS only supports 12 V VPP for 80 hours. The 12 V VPP is useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin **must** be tied to 3.3 V on the motherboard.

2.24. ICH2 Design Checklist

This checklist highlights design considerations that should be reviewed before manufacturing an Intel 820E chipset-based motherboard that implements an ICH2. The entries in this checklist should provide the important connections to these devices and any critical supporting circuitry. This is not a complete list and it doesn't guarantee that a design will function properly.

This list is only a reference. For correct operation, all design guidelines within this document must be followed.

Table 26. PCI Interface

Checklist Items	Recommendations	Reason/Effect
FYI	Inputs to the ICH2 must not be left floating.	Many GPIO signals are fixed inputs that must be pulled up to different sources. See the GPIO section for recommendations
PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ#[4:0], GPIO[1:0], THRM#	These signals require a pull-up resistor. An 8.2 kΩ pull-up resistor to V_{CC} 3.3 V or a 2.7 kΩ pull-up resistor to V_{CC} 5 V is recommended.	See the *PCI 2.2 Component Specification*. Pull-up recommendations for V_{CC} 3.3 V and V_{CC} 5 V
PCIRST#	The PCIRST#signal should be buffered to for the IDERST# signal. 33 Ω series resistor to IDE connectors	Improves signal integrity
PCIGNT#	No external pull-ups are required on PCI GNT signals. However, if external pull-ups are implemented, they must be pulled up to V_{CC} 3.3 V.	These signals are actively driven by the ICH2.
PME#	No extra pull-up resistors	This signal has an integrated pull-up of 9 kΩ ± 3 kΩ.
SERIRQ	External weak (8.2 kΩ) pull-up resistor to V_{CC} 3.3 V is recommended.	Open-drain signal
GNT[A]# / GPIO[16], GNT[B] / GNT[5]# / GPIO[17]	No extra pull-up is needed.	These signals have integrated pull-ups of 24 kΩ. GNT[A] has an added strap function of "top block swap." The signal is sampled on the rising edge of PWROK. The default value is high or disabled due to the pull-up. A jumper to a pull-down resistor can be added to manually enable the function.

Table 27. Hub Interface

Checklist Items	Recommendations	Reason/Effect
HL[11]	No pull-up resistor is required.	Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing.
HL_COMP	Tie the COMP pin to a 40 Ω, 1% or 2% (or 39 Ω, 1%) pull-up resistor (to 1.8 V), via a 10 mil wide, very short (~0.5 inch) trace.	ZCOMP no longer supported.

Table 28. LAN Interface

Checklist Items	Recommendations	Reason/Effect
LAN_CLK	Connect to platform LAN connect device.	
LAN_RXD[2:0]	Connect to LAN_RXD on platform LAN connect device.	ICH2 contains integrated 9K pull-up resistors on interface
LAN_TXD[2:0] LAN_RSTSYNC	Connect to LAX_TXD on platform LAN connect device.	
	LAN connect interface can be left NC if not used.	Input buffers are terminated internally.

Table 29. EEPROM Interface

Checklist Items	Recommendations	Reason/Effect
EE_DOUT	Prototype boards should include a placeholder for a pull-down resistor on this signal line, but should not populate the resistor. Connect to EE_DIN of EEPROM or CNR connector.	Connected to EEPROM data input signal. (Input from EEPROM perspective and output from ICH2 perspective.)
EE_DIN	No extra circuitry is required. Connect to EE_DOUT of EEPROM or CNR connector.	ICH2 contains integrated pull-up resistor for this signal. Connected to EEPROM data output signal. (Output from EEPROM perspective and input from ICH2 perspective.)

Table 30. FWH Flash BIOS Interface

Checklist Items	Recommendations	Reason/Effect
FWH[3:0] LAD[3:0] LDRQ[1:0]	No extra pull-ups required. Connect straight to FWH Flash BIOS.	ICH2 Integrates 24 kΩ resistors on these signal lines.

Table 31. Interrupt Interface

Checklist Items	Recommendations	Reason/Effect
PIRQ#[D:A]	These signals require a pull-up resistor. A 2.7 kΩ pull-up resistor to V_{CC} 5 V or an 8.2 kΩ pull-up resistor to V_{CC} 3.3 V is recommended.	In a non-APIC mode, the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx# line has a separate Route Control Register. In the APIC mode, these signals are connected to the internal I/O APIC, as follows: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the ISA interrupts.
PIRQ#[G:F] / GPIO[4:3]	These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to V_{CC} 5 or an 8.2 kΩ pull-up resistor to V_{CC} 3.3.	In non-APIC mode, the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC, as follows: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the ISA interrupts.
PIRQ#[H] PIRQ#[E]	These signals require a pull-up resistor. A 2.7 kΩ pull-up resistor to V_{CC} 5 or an 8.2 kΩ pull-up resistor to V_{CC} 3.3 is recommended.	In a non-APIC mode, the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx# line has a separate Route Control Register. In the APIC mode, these signals are connected to the internal I/O APIC, as follows: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the ISA interrupts. If not needed for interrupts, these signals can be used as GPIO.
APIC	• If the APIC is used — 150 Ω pull-up resistors on APICD[0:1] → Same as SC242 checklist: PICD[0:1] — Connect APICCLK to CK133, with a 20 Ω to 33 Ω series termination resistor. • If the APIC is not used on UP systems — APICCLK can either be tied to GND or connected to CK133, but cannot be left floating. — Pull APICD[0:1] to GND through 10 kΩ pull-down resistors.	**If the APIC is not used on UP systems:** Use pull-downs for each APIC signal. Do not share a resistor to pull-up signals.

Table 32. GPIO

Checklist Items	Recommendations	Reason/Effect
GPIO pins	**GPIO[0:7]:** • These pins are in the main power well. Pull-ups must use the 3.3 V plane. • Unused *core* well inputs must either be pulled up to VCC3.3 or be pulled down. These inputs must not be allowed to float. • GPIO[1:0] can be used as REQ[A:B]#. • GPIO[1] also can be used as PCI REQ[5]#. • These signals are 5 V tolerant.	Ensure that *all* unconnected signals are *outputs only*!
	GPIO[8] & [11:13]: • These pins are in the resume power well. Pull-ups must use the VCCSUS3.3 plane. • Unused *resume* well inputs must be pulled up to VCCSUS3.3. • These are the only GPIs that can be used as ACPI-compliant wake events. • These signals are not 5 V tolerant. **GPIO[16:23]:** • Fixed as output only. Can be left NC. • In the main power well • GPIO22 is open-drain. **GPIO[24, 25, 27, 28]:** • I/O pins. Can be left NC. • From resume power well	These are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.

Table 33. USB Interface

Checklist Items	Recommendations	Reason/Effect
USBP[3:0]P USBP[3:0]N	See Figure 56 for the circuitry needed on each differential pair.	

Table 34. Power Management

Checklist Items	Recommendations	Reason/Effect
THRM#	Connect to temperature sensor. Pull-up if not used.	Input to ICH2 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up.
SLP_S3# SLP_S5#	No pull-up/pull-down resistors needed. Signals driven by ICH2.	Signal driven by ICH2.
PWROK	This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both Vcc 3_3 and Vcc 1_8 have reached their nominal voltages	Timing requirement
PWRBTN#	No extra pull-up resistors	This signal has an integrated pull-up of 9 kΩ ± 3 kΩ.
RI#	RI# does not have an internal pull-up. An 8.2 kΩ pull-up resistor to the resume well is recommended.	If this signal is enabled as a wake event, it is important to keep it powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	This signal should be connected to power monitoring logic, and it should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_8 have reached their nominal voltages. It can be tied to RESUMEPWROK on desktop platforms.	Timing requirement

Table 35. Processor Signals

Checklist Items	Recommendations	Reason/Effect
A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#	Internal circuitry has been added to the ICH2. External pull-up resistors are not needed.	Push/pull buffers now drive the output signals.
FERR#	Requires a weak external pull-up resistor to VCC_{CORE}.	For specific values, refer to the processor documentation for the processor that the platform utilizes.
RCIN# A20GATE	Pull-up signals to V_{CC} 3.3 through a 10 kΩ resistor	Typically driven by an open-drain external microcontroller.
CPUPWRGD	Connect to the processor PWRGOOD input. Requires a weak external pull-up resistor to VCC_{CORE}.	For specific values, refer to the processor documentation for the processor that the platform utilizes.

Table 36. System Management

Checklist Items	Recommendations	Reason/Effect
SMBDATA SMBCLK	Requires external pull-up resistors to 3.3 V or 3.3 V standby.	Value of pull-up resistors is determined by the line load. Open-drain signal in resume well
SMBALERT#/ GPIO[11]	See GPIO section if SMBALERT# not implemented.	
SMLINK[1:0]	Requires external pull-up resistors to 3.3 V.	Open-drain signal in resume well
INTRUDER#	Pull signal to V_{BAT} if not needed.	Signal in VCCRTC (V_{BAT}) well.

Table 37. RTC

Checklist Items	Recommendations	Reason/Effect
VBIAS	The VBIAS pin of the ICH2 is connected to a 0.047 µF cap**.** *See Figure 59*	For noise immunity on VBIAS signal
RTCX1 RTCX2	Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor, and use 12 pF decoupling caps at each signal. RTCX1 may optionally be driven by an external oscillator instead of a crystal. These signals are 1.8 V only and must not be driven by a 3.3 V source.	The ICH2 implements new internal oscillator circuit as compared with the PIIX4, to reduce the power consumption. The external circuitry shown in Figure 59 is required to maintain RTC accuracy. The circuitry is required because the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step voltage change of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.

Table 38. AC'97

Checklist Items	Recommendations	Reason/Effect
AC_SDOUT	Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation.	This pin has a weak internal pull-down. To properly detect a safe_mode condition, a strong pull-up is required to override this internal pull-down.
AC_SDIN[1], AC_SDIN[0]	Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector. If there is no codec on the system board, then both AC_SDIN[1:0] should be pulled down externally with resistors to ground.	AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous.
AC_BITCLK	No extra pull-down resistors are required.	When nothing is connected to the link, the BIOS must set a shut-off bit for the internal keeper resistors to be enabled. At that point, pull-ups/pull-downs are not required on any of the link signals.
AC_SYNC	No extra pull-down resistors are required.	Some implementations add termination for signal integrity. Platform specific.

Table 39. Miscellaneous Signals

Checklist Items	Recommendations	Reason/Effect
SPKR	No extra pull-up resistors Effective impedance due to speaker and codec circuitry must be greater than 50 kΩ, or a means to isolate the resistive load from the signal while PWROK is low must be found.	Has integrated pull-up with a resistance between 18 kΩ and 42 kΩ. The integrated pull-up is enabled only during boot/reset for strapping functions. At all other times, the pull-up is disabled. A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled.
TP[0]	Requires external pull-up resistor to VCCSUS3.3.	This signal is used for BATLOW in mobile, but it is not required for desktop.
FS[0]	Route to a test point.	ICH2 contains an integrated pull-up for this signal. Test point used for manufacturing appears in XOR tree.

Table 40. Power

Checklist Items	Recommendations	Reason/Effect
V_CPU_IO[1:0]	The power pins should be connected to the proper power plane for the processor's CMOS compatibility signals. Use one 0.1 µF decoupling cap.	Used to pull-up all processor I/F signals
Vcc RTC	No clear CMOS jumper on Vcc RTC. Use a jumper on RTCRST# or a GPI, or use safe-mode strapping for clear CMOS	
Vcc 3.3 V	Requires six 0.1 µF decoupling caps	
Vcc Sus 3.3 V	Requires one 0.1 µF decoupling cap.	
Vcc 1.8 V	Requires two 0.1 µF decoupling caps.	
Vcc Sus 1.8 V	Requires one 0.1 µF decoupling cap.	
5V_REF SUS	Requires one 0.1 µF decoupling cap. V5REF_SUS affects only the 5 V tolerance for USB OC[3:0] ins, and it can be connected to VccSUS3_3 if 5 V tolerance is not required for these signals.	
5V_REF	5 V_{REF} is the reference voltage for 5 V-tolerant inputs in the ICH2. The VREF[2:1] pins must be tied together. 5 V_{REF} must power up before or simultaneously with Vcc 3_3. It must power down after or simultaneously with Vcc 3_3.	Refer to Figure 73, which shows an example circuit schematic that may be used to ensure the proper 5 VREF sequencing.

Figure 73. $5V_{REF}$ Circuitry

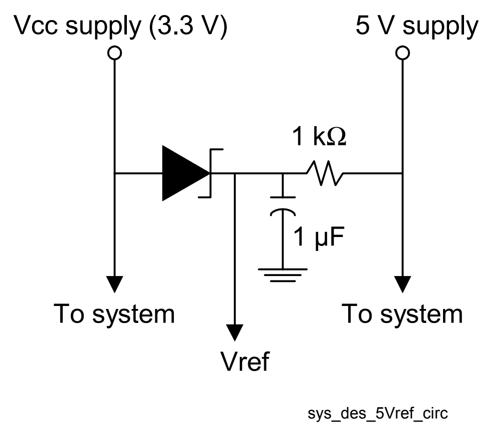


Table 41. IDE Checklist

Checklist Items	Recommendations	Reason/Effect
PDD[15:0], SDD[15:0]	No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 doesn't require a 10 kΩ pull-down resistor. Refer to the ATA TAPI-4 specification.	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but can range from 31 Ω to 43 Ω.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	No extra series termination resistors. Pads for series resistors can be implemented if the system designer has signal integrity concerns.	These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω, but can range from 31 Ω to 43 Ω.
PDREQ SDREQ	No extra series termination resistors No pull-down resistors are needed.	These signals have integrated series resistors in the ICH2. These signals have integrated pull-down resistors in the ICH2.
PIORDY SIORDY	No extra series termination resistors. Pull-up to 3.3 V via a 4.7 kΩ resistor.	These signals have integrated series resistors in the ICH2.
IRQ14, IRQ15	Recommend 8.2 kΩ to 10 kΩ pull-up resistor to 3.3 V. No extra series termination resistors	Open-drain outputs from drive
IDERST#	The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	

Checklist Items	Recommendations	Reason/Effect
Cable Detect*	• Host Side/Device Side Detection: — Connect the IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. • Device-side detection: — Connect a 0.04 µF capacitor from the IDE pin PDIAG/CBLID to GND. No ICH2 connection	The 10 kΩ resistor to GND prevents GPI from floating, if no devices are present on either IDE interface. Allows the use of 3.3 V GPIOs that are not 5 V tolerant. **Note:** All ATA66/100 drives can detect cables. See Figure 46. See Figure 47.

Note: *The maximum trace length from the ICH2 to the ATA connector is 8 inches.*

Table 42. ISA Bridge Checklist

Checklist Items	Recommendations	Reason/Effect
ICH2 GPO[21] / ISA NOGO input	Connect ICH2 GPO[21] to ISA NOGO input. If GPO[21] is not available on the ICH2, any other GPO that defaults high in the system can be used. GPO[21] is the only ICH2 GPO that defaults high.	
ICH2 AD22 / ISA IDSEL input	Connect ICH2 AD22 to the ISA IDSEL input.	

2.25. ICH2 Layout Checklist

Table 43. 8-Bit Hub Interface

#	Layout Recommendations	Yes	No	Comments
1	Board impedance must be 60 Ω ± 10%.			
2	Traces must be routed 5 mils wide with 20 mils spacing.			
3	In order to break out of the MCH and ICH2 package, the hub interface signals can be routed 5 on 5. Signals must be separated to 5 on 20 within 300 mils of the package.			
4	Max. trace length is 8 inches.			
5	Data signals must be matched within ±0.1 inch of the HL_STB diff pair.			
6	Each strobe signal must be the same length.			
7	HUBREF divider should be placed no more than 4 inches away from MCH or ICH2. If so, then separate resistor divider must be placed locally.			

Table 44. IDE Interface

#	Layout Recommendations	Yes	No	Comments
1	5 mils wide and 7 mil spaces			
2	Max. trace length is 8 inches.			
3	Shortest trace length must be 0.5 inch shorter than longest trace length.			

Table 45. USB

#	Layout Recommendations	Yes	No	Comments
1	Characteristic impedance of individual signal lines P+, P- : Z_0 = 45 Ω (90 Ω differential)			
2	Stack-up: 9 mils wide, 25 mil spacing between differential pairs			
3	Trace characteristics • Line delay = 160.2 ps • Capacitance = 3.5 pF • Inductance = 7.3 nH • Res at 20^{o} C = 53.9 mΩ			
4	15 Ω series resistor placed < 1 inch from ICH2.			
5	47 pF parallel caps should be placed as close as possible to the ICH2.			
6	15 kΩ ± 5% pull-down resistors must be present on the connector side of the series resistor.			
7	Stub length due to 15 kΩ pull-downs should be as short as possible.			

Table 46. LAN Connect I/F

#	Layout Recommendations	Yes	No	Comments
1	Stack-up: 5 mils wide, 10 mil spacing			
2	Z_0 = 60 Ω ± 15%			Signal integrity requirement
3	LAN max. trace length, ICH2 to CNR : L = 3 inches to 9 inches (0.5 inch to 3 inches on card)			To meet timing requirements
4	Stubs due to R-pak CNR/LOM stuffing option should not be present.			To minimize inductance
5	Max. trace lengths, ICH2 to 82562EH/ET/EM : L = 4.5 inches to 8.5 inches			To meet timing requirements
6	Max. mismatch between length of a clock trace and length of any data trace is 0.5 inch.			To meet timing and signal quality requirements
7	Maintain constant symmetry and spacing between the traces within a differential pair.			To meet timing and signal quality requirements
8	Keep the total length of each differential pair less than 4 inches.			Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and/or degraded receive BER
9	Do not route the transmit differential traces within 70 mils of the receive differential traces.			To minimize crosstalk
10	Distance between differential traces and any other signal line is 70 mils.			To minimize crosstalk
11	Keep max. separation between differential pairs at 7 mils.			To meet timing and signal quality requirements
12	Differential trace impedance should be controlled to ~100 Ω.			To meet timing and signal quality requirements
13	For high speed signals, the number of corners and vias should be minimized. If a 90º bend is required, it is advisable to use two 45º bends.			To meet timing and signal quality requirements
14	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.			This allows the field around the trace to couple more easily to the ground plane, rather than to adjacent wires or boards.
15	Do not route traces and vias under crystals or oscillators.			This will prevent coupling to or from the clock.
16	Ration of trace width to height above the ground plane should be between 1:1 and 3:1.			To control trace EMI radiation
17	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.			Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
18	Vias to decoupling capacitors should have sufficient diameter.			To decrease series inductance
19	Avoid routing high-speed LAN or phone line traces near other high-frequency signals associated with a video controller, cache controller, CPU or similar devices.			To minimize crosstalk

#	Layout Recommendations	Yes	No	Comments
20	Isolate I/O signals from high-speed signals.			To minimize crosstalk
21	Place the 82562ET/EM part more than 1.5 inches from any board edge.			This minimizes the potential of EMI radiation problems.
22	Verify the EEPROM size. 82562ET : 64 word 82562EM : 256 word			TheIntel® 82562EM requires a larger EEPROM to store the alert envelope and other configuration information.
23	Place at least one bulk capacitor (≥ 4.7 µF is OK) on each side of the 82562ET/EM.			Research and development has shown that this is a robust design.
24	Place decoupling caps (0.1 µF) as close as possible to the 82562ET/EM.			
25	RBIAS10 and RBIAS100 resistors should have 1% values.			These biasing resistors require 1% accuracy. Note that the values shown on the reference schematic are the recommended starting values. Fine tuning (via IEEE conformance testing) is required for each new design.

Table 47. AC’97

#	Layout Recommendations	Yes	No	Comments
1	Z_0 AC’97 = 60 Ω ± 15%			
2	5 mil trace width, 5 mil spacing between traces			
3	Max. trace length ICH2/codec/CNR = **14 inches**			

Table 48. ICH2 Decoupling

#	Layout Recommendations	Yes	No	Comments
1	3.3Vcore : Six 0.1 µF caps			
2	3.3VSBY : One 0.1 µF cap			
3	CPUI/F(VCCcore) : One 0.1 µF cap			
4	1.8Vcore : Two 0.1 µF caps			
5	1.8VSBY : One 0.1 µF cap			
6	5VREF : One 0.1 µF cap			
7	5VREFSBY : One 0.1 µF cap			
8	Place decoupling caps as close as possible to the ICH2 (~200 mils).			

Table 49. CK-SKS Clocking

#	Layout Recommendations	Yes	No	Comments
1	CLK_33 goes to ICH2, FWH FLASH BIOS, and SIO. Clock chip to series resistor = 0.5 inch, and from series resistor to receiver = 15 inches max. Routed on one layer.			
2	PCI_33 goes to PCI device or PCI slot. There are 5 clocks. Clock chip to series resistor = 0.5 inch, and from series resistor to receiver = 13 inches max. Routed on one layer.			
3	CLK_66 goes to ICH2 and MCH. Clock chip to series resistor = 0.5 inch, and from series resistor to receiver = 14 inches max. Routed on one layer.			
4	AGP_66 goes to AGP connector. Clock chip to series resistor = 0.5 inch, and from series resistor to receiver = 11 inches max. Routed on one layer.			

Table 50. RTC

#	Layout Recommendations	Yes	No	Comments
1	RTC lead length ≤ 0.25 inch max.			
2	Minimize capacitance between Xin and Xout.			
3	Put GND plane underneath crystal components.			
4	Don’t route switching signals under external components (unless on other side of board).			

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3. Advanced System Bus Design

Section 2.10 describes the recommendations for designing Intel 820E chipset-based platforms. This section discusses in more detail the methodology used to develop the advanced system bus guidelines. These layout considerations apply to Intel 820E chipset/FC-PGA designs. The design guidelines for the Pentium® III processor for the Intel PGA370 socket are found in the *Intel® 820 Platform Design Guide Addendum*, Revision 0.95.

Section 3.2 discusses specific system guidelines. This is a step-by-step methodology that Intel has successfully used to design high-performance desktop systems. Section 3.3 introduces the theories applicable to this layout guideline. Section 3.4 contains more details and insights. Section 3.4 expands on part of the rationale for the recommendations in the step-by-step methodology. This section also includes equations that may be used for reference.

3.1. Terminology and Definitions

Term	Definition
Aggressor	The network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+ (Assisted Gunning Transceiver Logic). AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor's AGTL+ output buffers differ from the GTL+ buffers, with the addition of an active pMOS pull-up transistor to "assist" the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus agent	Component or group of components that, when combined, represent a single load on the AGTL+ bus
Corner	Describes how a component performs when all parameters that could affect performance are adjusted to have the same effect on performance. Examples of these parameters include variations in the manufacturing process, the operating temperature, and the operating voltage. The resulting performance of an electronic component that may change as a result of corners includes, but is not limited to, the following: clock-to-output time, output driver edge rate, output drive current, and input drive current. A "slow" corner means a component operating at its slowest, weakest drive strength performance. Conversely, a "fast" corner means a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow and fast corners should bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by an aggressor network(s), through inductive and capacitive coupling between the networks Backward crosstalk: Coupling that creates a signal in a victim network, that travels in the direction opposite to the aggressor's signal Forward crosstalk: Coupling that creates a signal in a victim network, that travels in the same direction as the aggressor's signal Even-mode crosstalk: Coupling from multiple aggressors when all aggressors switch in the direction in which the victim is switching Odd-mode crosstalk: Coupling from multiple aggressors when all aggressors switch in the direction opposite to that in which the victim is switching

Term	Definition
Flight time	Flight time is a timing equation term that includes the signal propagation delay, any effects of the system on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as the time difference between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing V_{REF}, if the driver was driving the test load used to specify the driver's AC timings. The V_{REF} guard band takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition of the V_{REF} guard band. **Maximum and Minimum Flight Time.** Flight time variations can be caused by many different parameters. Obvious causes include variation of the board dielectric constant, changes in the load condition, crosstalk, V_{TT} noise, V_{REF} noise, variation of the termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and the manufacturing process. Less obvious causes include the effects of Simultaneous Switching Output (SSO) and packaging effects. **Maximum Flight Time** is the largest flight time a network will experience under all variations of conditions. Maximum flight time is measured at the appropriate V_{REF} guard-band boundary. **Minimum Flight Time** is the smallest flight time a network will experience under all variations of conditions. Minimum flight time is measured at the appropriate V_{REF} guard-band boundary.
GTL+	GTL+, the bus technology used by the Pentium® Pro processor, is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement of GTL (Gunning Transceiver Logic) technology.
Network	Trace of a printed circuit board (PCB) that completes an electrical connection between two or more components
Network length	Distance between extreme bus agents on the network. It does not include the distance of the connection between the end bus agents and the termination resistors.
Overdrive region	Voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis.
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for the overshoot specification.
Pad	A feature of a semiconductor die contained within an internal logic package used to connect the die to the package bond wires. A pad is only observable in simulation.
Pin	A feature of a logic package used to connect the package to an internal substrate trace
Ringback	Voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See the respective processor's datasheet for the ringback specification.
Settling limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for the settling limit specification.
Setup window	Time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may differ for each type of bus agent in the system.

Term	Definition
Simultaneous switching output (SSO) effects	Difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high to low), in the direction opposite to a single signal (e.g., low to high) or in the same direction (e.g., high to low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out") or a decrease in propagation delay (or "pull-in"). These SSO effects may affect the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	Branch from the trunk terminating at the pad of an agent
Test load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads
Undershoot	Maximum voltage a signal may extend below V_{SS} at the processor core pad. See the respective processor's datasheet for the undershoot specifications.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
V_{REF} guard band	A guard band (ΔV_{REF}) defined above and below V_{REF}, to provide a more realistic model accounting for noise, such as crosstalk, V_{TT} noise, and V_{REF} noise

3.2. AGTL+ Design Guidelines

The following step-by-step guideline was developed for systems based on two processor loads and one Intel 82820 MCH load. Systems using custom chipsets will require timing analysis and analog simulations specific to those components.

The guideline recommended in this section is based on experience accumulated at Intel while developing many different systems based on the Intel® Pentium® Pro processor family and the Pentium III processor. First, perform an initial timing analysis and topology definition. Then perform pre-layout analog simulations, for a detailed picture of a working "solution space" for the design. These pre-layout simulations help define the routing rules prior to placement and routing. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology

- Initial timing analysis
- Determine general topology, layout, and routing.
- Pre-layout simulation
  - Sensitivity sweep
  - Monte Carlo Analysis
- Place and route board
  - Estimate component-to-component spacing for AGTL+ signals.
  - Lay out and route board.
- Post-layout simulation
  - Interconnect extraction
  - Intersymbol interference (ISI), crosstalk, and Monte Carlo Analysis
- Validation
  - Measurements
  - Determining flight time

3.2.1. Initial Timing Analysis

Perform an initial timing analysis of the system using the following two equations, which are the basis for timing analysis. To complete the initial timing analysis, values for clock skew and clock jitter are needed, along with the component specifications. These equations contain a multi-bit adjustment factor, M_{ADJ}, to account for multi-bit switching effects (e.g., SSO push-out or pull-in) that often are hard to simulate. These equations **do not** take into consideration all signal integrity factors that affect timing. Additional timing margin should be budgeted to allow for these sources of noise.

Equation 4. Setup Time

$$T_{CO\_MAX} + T_{SU\_MIN} + CLK_{SKEW} + CLK_{JITTER} + T_{FLT\_MAX} + M_{ADJ} \leq \text{Clock period}$$

Equation 5. Hold Time

$$T_{CO\_MIN} + T_{FLT\_MIN} - M_{ADJ} \geq T_{HOLD} + CLK_{SKEW}$$

Symbols used in these two equations:

T_{CO_MAX}	Max. clock-to-output specification (see Note)
T_{SU_MIN}	Min. required time specified to setup before the clock (see Note)
CLK_{JITTER}	Max. clock edge-to-edge variation.
CLK_{SKEW}	Max. variation between components receiving the same clock edge
T_{FLT_MAX}	Max. flight time, as defined in Section 3.1
T_{FLT_MIN}	Min. flight time, as defined in Section 3.1
M_{ADJ}	Multi-bit adjustment factor to account for SSO push-out or pull-in
T_{CO_MIN}	Min. clock-to-output specification (see Note)
T_{HOLD}	Min. specified input hold time

Note: The clock-to-output (T_{CO}) and setup-to-clock (T_{SU}) timings are both measured from the signal's last crossing of V_{REF}, with the requirement that the signal does not violate the ringback or edge rate limits. See the respective processor's datasheet and the *Pentium® III Processor Developer's Manual* for more details.

Solving these equations for T_{FLT} yields the following equations:

Equation 6. Maximum Flight Time

$$T_{FLT\_MAX} \leq \text{Clock period} - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ}$$

Equation 7. Minimum Flight Time

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ}$$

Multiple cases must be considered. Note that while the same trace connects two components, component A and component B, the minimum and maximum flight time requirements for component A driving component B as well as component B driving component A must be met. The cases to be considered are:

- Processor driving processor
- Processor driving chipset
- Chipset driving processor

A designer using components other than those listed previously must evaluate additional combinations of driver and receiver.

Table 51. AGTL+ Parameters for Example Calculations[1,2]

IC Parameters	Pentium® III Processor Core at 133 MHz Bus	Intel® 82820 MCH	Notes
Clock-to-output maximum (T_{CO_MAX})	2.7	3.6	4
Clock-to-output minimum (T_{CO_MIN})	-0.1	0.5	4
Setup time (T_{SU_MIN})	1.2	2.27	3,4
Hold time (T_{HOLD})	0.8	0.28	4

NOTES:

1. All times in nanoseconds.
2. **Numbers in table are for reference only.** These timing parameters are subject to change. Please check the appropriate component documentation for the valid timing parameter values.
3. T_{SU_MIN} = 1.9 ns assumes the Intel 82820 MCH sees a minimum edge rate equal to 0.3 V/ns.
4. The Pentium III processor substrate's nominal impedance is set to 65 Ω ± 15%. Future Pentium III processor substrates may be set at 60 Ω ± 15%.

Table 51 lists the AGTL+ component timings of the processors and Intel 82820 MCH defined at the pins. These timings are for reference only.

Table 52 gives an example AGTL+ initial maximum flight time and Table 53 contains an example minimum flight time calculation for a 133 MHz, 2-way Pentium III processor/Intel 820E chipset system bus. Note that assumed values for clock skew and clock jitter were used. Clock skew and clock jitter values depend on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.

Intel highly recommends adding margin, as shown in the M_{ADJ} column, to offset the degradation caused by SSO push-out and other multi-bit switching effects. The Recommended T_{FLT_MAX} column contains the recommended maximum flight time after incorporating the M_{ADJ} value. If the edge rate, ringback, and monotonicity requirements are not met, flight time correction must first be performed as documented in the *Intel® Pentium® II Processor Developer's Manual*, with the additional requirements noted in Section 3.5. The commonly used "textbook" equations used to calculate the expected signal propagation rate of a board are included in Section 3.2.

Simulation and control of baseboard design parameters can ensure that the signal quality and maximum and minimum flight times are met. Baseboard propagation speed is highly dependent on the transmission line geometry configuration (stripline vs. microstrip), dielectric constant, and loading. This layout guideline includes high-speed baseboard design practices that may improve the amount of timing and signal quality margin. The magnitude of M_{ADJ} is highly dependent on the baseboard design implementation (stack-up, decoupling, layout, routing, reference planes, etc.) and must be characterized and budgeted appropriately for each design.

The following two tables were derived assuming the following:

- CLK_{SKEW} = 0.2 ns
  Note: This assumes that clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together ("ganging") at the clock driver output pins, and the PCB clock routing skew is 150 ps. The system timing budget must assume 0.175 ns of clock driver skew if outputs are not tied together and a clock driver that meets the CK98 clock driver specification is being used.
- CLK_{JITTER} = 0.250 ns

Some clock driver components may not support ganging the outputs. Be sure to verify with your clock component vendor before ganging the outputs. See the appropriate Intel 820E chipset documentation for details regarding the clock skew and jitter specifications. Refer to Section 2.7.2 and Chapter 4 for host clock routing details.

Table 52. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor[4]	Processor[4]	7.50	2.7	1.20	0.20	0.250	0.40	2.75
Processor[4]	Intel® 82820 MCH	7.50	2.7	2.27	0.20	0.250	0.40	1.68
82820 MCH	Processor[4]	7.50	3.63	1.20	0.20	0.25	0.40	1.82

NOTES:

1. All times in nanoseconds.
2. BCLK period = 7.50 ns @ 133.33 MHz
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   a. SSO push-out or pull-in.
   b. Rising-edge or falling-edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   c. Crosstalk on the PCB and internal to the package can cause variation in the signals.
   Additional effects *may not necessarily* be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:
   a. Effective board propagation constant (SEFF), which is a function of:
      – Dielectric constant (ε_r) of the PCB material
      – Type of trace connecting the components (stripline or microstrip)
      – Length of the trace and load of components on trace (Note that the board propagation constant multiplied by the trace length is a component of the flight time, but not necessarily equal to the flight time.)
4. Processor values specified in this table are examples only. Refer to the appropriate processor datasheet for the specification values.

Table 53. Example T_{FLT_MIN} Calculations[1] (Frequency Independent)

Driver	Receiver	THOLD	ClkSKEW	TCO_MIN	Recommended TFLT_MIN
Processor[2]	Processor[2]	0.8	0.2	-0.1	1.2
Processor[2]	Intel® 82820 MCH	0.28	0.2	-0.1	.58
82820 MCH	Processor[2]	0.8	0.2	0.5	.5

NOTES:

1. All times in nanoseconds.
2. Processor values specified in this table are examples only. Refer to the appropriate processor datasheet for the specification values.

3.2.2. Determine the Desired General Topology, Layout, and Routing

After calculating the timing budget, determine the approximate location of the processor and the chipset on the baseboard (see Section 2.10).

3.2.3. Pre-Layout Simulation

3.2.3.1. Methodology

Analog simulations are recommended for high-speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working "solution space" that satisfies the flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the device pads for signal quality and at the device pins for timing analysis. However, simulation results at the device pins may later be used to correlate simulation performance against actual system measurements.

3.2.3.2. Sensitivity Analysis

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others (e.g., driver strength, package, Z_0, S_0) are held constant. This allows the sensitivity of the proposed bus topology to varying parameters to be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect the flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all sweeps that pass timing and signal quality tests. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

3.2.3.3. Monte Carlo Analysis

Perform a Monte Carlo Analysis to refine the passing solution space region. A Monte Carlo Analysis involves randomly varying parameters independently of one another, over their tolerance ranges. This analysis is designed to ensure that no region of failing flight time and signal quality exists between the extreme corner cases run in pre-layout simulations. For the example topology, vary the following parameters during Monte Carlo simulations:

- Lengths L1 through L3
- Termination resistance RTT on processor Intel PGA370 socket 1
- Termination resistance RTT on processor Intel PGA370 socket 2
- Z0 of traces on processor Intel PGA370 socket 1
- Z0 of traces on processor Intel PGA370 socket 2
- S0 of traces on processor Intel PGA370 socket 1
- S0 of traces on processor Intel PGA370 socket 2
- Z0 of traces on baseboard
- S0 of traces on baseboard
- Fast and slow corner processor I/O buffer models for Intel PGA370 socket 1
- Fast and slow corner processor I/O buffer models for Intel PGA370 socket 2
- Fast and slow package models for processor Intel PGA370 socket 1
- Fast and slow package models for processor Intel PGA370 socket 2
- Fast and slow corner Intel 82820 MCH I/O buffer models
- Fast and slow Intel 82820 MCH package models

3.2.3.4. Simulation Criteria

Accurate simulation requires that the actual range of parameters be used in the simulation. Intel has consistently measured the cross-sectional resistivity of PCB copper to be approximately 1 $\Omega \cdot mil^2$/inch, not the 0.662 $\Omega \cdot mil^2$/inch value for annealed copper that is published in reference material. Using the 1 $\Omega \cdot mil^2$/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions—given appropriate variations in the other network parameters—can generate the worst-case noise margin. Therefore, Intel recommends simulating the networks from all driver locations and analyzing each receiver for each possible driver.

Analysis has shown that **both** fast and slow corner conditions must be run for both rising-edge and falling-edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts from a higher V_{OL}. So, Intel **highly recommends** checking for minimum and maximum flight time violations with both the fast and slow corner models. The fast and slow corner I/O buffer models are contained in the processor and Intel 820 chipset electronic models provided by Intel.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. This is performed, generally, by editing the simulator's net description or topology file.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z0 and S0. Intel therefore recommends that PCB parameters be controlled as tightly as possible, with sampling of the allowable Z0 and S0 simulated. The Intel PGA370-socketed Pentium III processor's nominal effective line impedance (Z_{EFF}) is 60 Ω ± 15%. Intel recommends a baseboard nominal effective line impedance of 60 Ω ± 15% for the recommended layout guidelines to be effective. Intel also recommends both running uncoupled simulations using the Z_0 of the package stubs as well as performing fully coupled simulations if increased accuracy is needed or desired. Accounting for crosstalk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This led to the development of full-package models for the component packages.

3.2.4. Place and Route Board

3.2.4.1. Estimate Component-to-Component Spacing for AGTL+ Signals

Estimate the number of layers that will be required. Then determine the expected interconnect distances between each component on the AGTL+ bus. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency.

Table 52 and Table 53 assume values for CLKSKEW and CLKJITTER parameters that are controlled by the system designer. To minimize the system clock skew, Intel recommends clock buffers that allow their outputs to be tied together. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margins.

3.2.4.2. Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Also stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information, including the following general guidelines:

- Distribute V_{TT} with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the V_{TT} trace with the same topology as the AGTL+ traces.
- Keep the overall length of the bus as short as possible, but do not forget the minimum component-to-component distances required to meet hold times.
- Plan to minimize crosstalk with the following guidelines developed for the example topology given. (Signal spacing recommendations were based on fully coupled simulations. Spacing may be decreased based upon the amount of coupled length.)
  - Use a spacing-to-line width-to-dielectric thickness ratio of at least 3:1:2. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%.
  - Minimize the dielectric process variation used in PCB fabrication.
  - Eliminate parallel traces between layers not separated by a power or ground plane.

Table 54contains the trace width:space ratios assumed for this topology. The crosstalk cases considered in this guideline involve three types: intragroup AGTL+, intergroup AGTL+, and AGTL+ to non-

AGTL+. Intragroup AGTL+ crosstalk involves interference between AGTL+ signals within the same group. (See Section 3.4 for a description of the different AGTL+ group types.) Intergroup AGTL+ crosstalk involves the interference of AGTL+ signals in a particular group with AGTL+ signals in a different group. An example of AGTL+-to-non-AGTL+ crosstalk is when CMOS and AGTL+ signals interfere with each other.

Table 54. Trace Width Space Guidelines

Crosstalk Type	Trace Width:Space Ratio
Intragroup AGTL+ (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

The spacing between the various bus agents causes variations in trunk impedance and stub locations. These variations cause reflections that can cause constructive or destructive interference at the receivers. Noise may be reduced by providing minimal spacing the agents. Unfortunately, tighter spacing results in reduced component placement options and lower hold margins. Therefore, adjusting the inter-agent spacing may be one way to change the network's noise margin, but mechanical constraints often limit the usefulness of this technique. Always be sure to validate signal quality after making any changes in agent locations or changes to inter-agent spacing.

Six AGTL+ signals can be driven simultaneously by more than one agent. These signals may require more attention during the layout and validation portions of the design. When a signal is asserted (i.e., driven low) by two or more agents on the same clock edge, the two falling-edge wavefronts will meet at some point on the bus and can sum to form a negative voltage. The ringback from this negative voltage can easily cross into the overdrive region. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

This document addresses AGTL+ layout for both one-way and two-way 133 MHz/100 MHz processor/ Intel 820E chipset systems. Power distribution and chassis requirements for cooling, connector location, memory location, etc., may constrain the system topology and component placement location, thereby constraining the board routing. These issues are not addressed directly in this document. Section 1.2 contains a listing of several documents that address some of these issues.

3.2.4.3. Host Clock Routing

For Intel 820E chipset/FC-PGA clock routing guidelines, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at http://developer.intel.com/design/chipsets/designex/298178.htm.

3.2.4.4. APIC Data Bus Routing

Intel recommends using the in-line topology shown in the following two figures for the APIC data signals, PICD[1:0]. For dual-processor systems, the network should be dual-end terminated with 300 Ω to 330 Ω resistors. For Intel 820E chipset/FC-PGA APIC (PICD[1:0]) routing guidelines, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at http://developer.intel.com/design/chipsets/designex/298178.htm.

Figure 74. PICD[1,0] Uniprocessor Topology

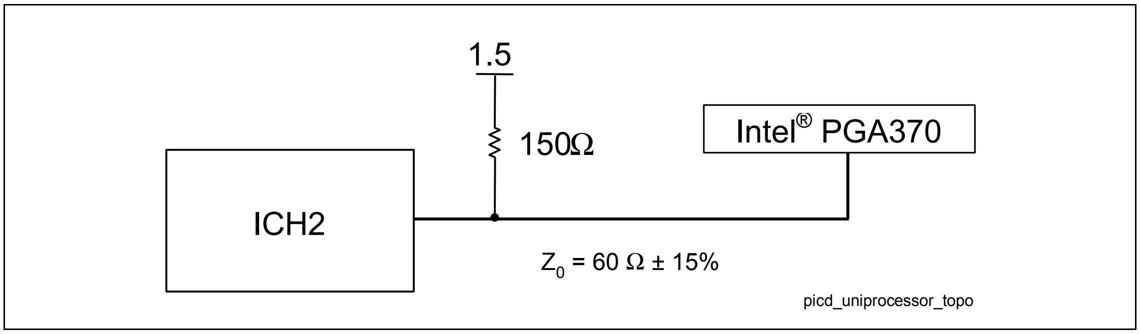
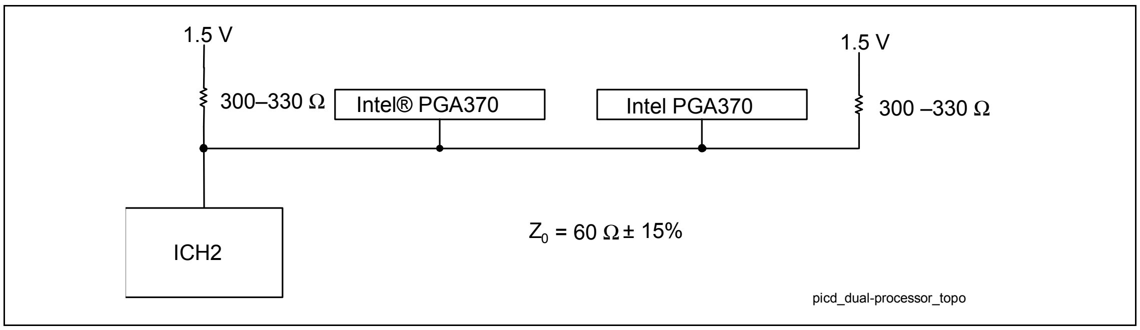


Figure 75. PICD[1,0] Dual-Processor Topology



3.2.5. Post-Layout Simulation

After layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout satisfies the timing and noise requirements. A small amount of “tuning” may be required. Experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. Post-layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity at the device pads and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings at the device pins, so simulation results at the device pins should be used later to correlate the simulation performance with actual system measurements.

3.2.5.1. Intersymbol Interference

Intersymbol interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol interference occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and high in consecutive cycles. (The opposite case also is valid.) When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycles. ISI effects do not necessarily span only 3 cycles, so it may be necessary to simulate beyond 3 cycles for certain designs. After simulating and quantifying the ISI effects, adjust the timing budget accordingly to take into consideration these conditions.

3.2.5.2. Crosstalk Analysis

AGTL+ crosstalk simulations can consider as non-coupled the processor core package, the Intel 82820 MCH package, and the Intel PGA370 socket. Simulate the traces as lossless for worst-case crosstalk and lossy where more accuracy is needed. Evaluate both odd-mode and even-mode crosstalk conditions.

AGTL+ crosstalk simulation involves the following cases:

- Intragroup AGTL+ crosstalk
- Intergroup AGTL+ crosstalk
- Non-AGTL+ to AGTL+ crosstalk

3.2.5.3. Monte Carlo Analysis

Perform a Monte Carlo Analysis on the extracted baseboard. Vary all parameters recommended for pre-layout Monte Carlo Analysis within the regions in which they are expected to vary. The ranges for some parameters will be reduced relative to those in the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full minimum and maximum ranges in the final baseboard design. Instead, baseboard lengths should now have an actual route, with length tolerances specified by the baseboard fabrication manufacturer.

3.2.6. Validation

Build systems and validate the design and simulation assumptions.

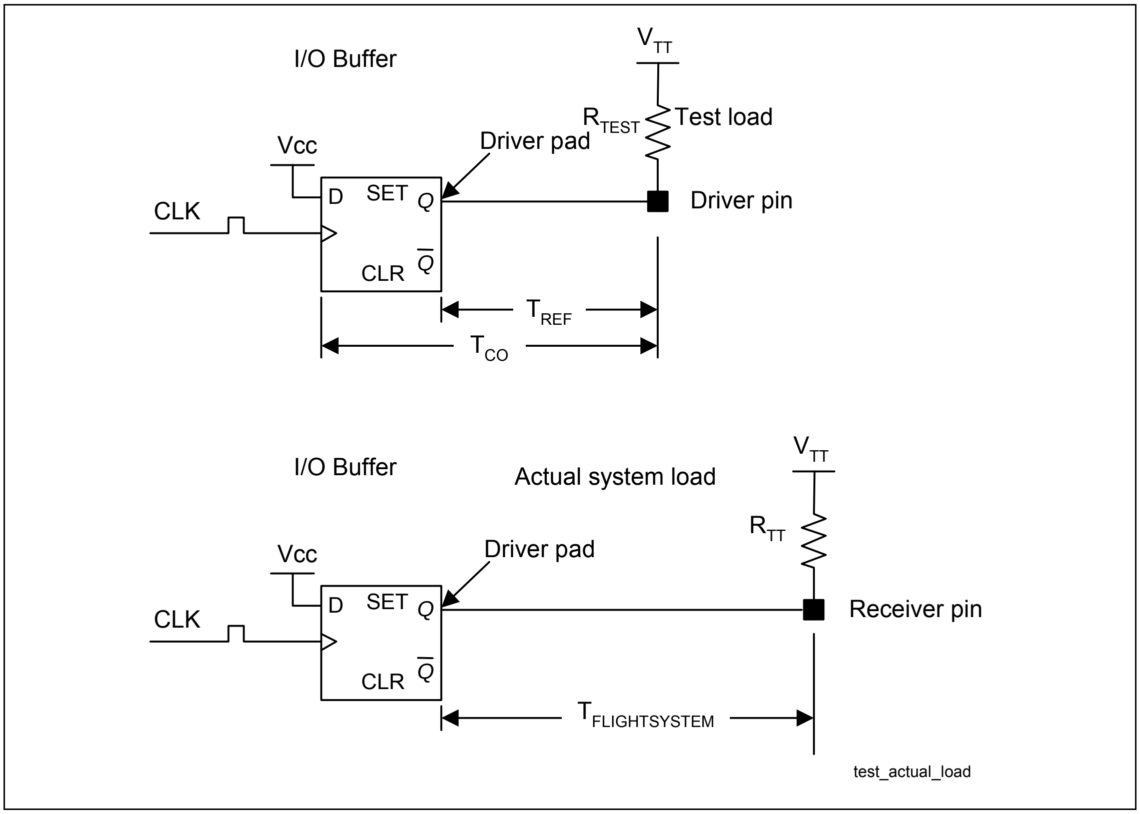
3.2.6.1. Measurements

Note that the AGTL+ specification for signal quality is at the component pad. The expected method of signal quality determination is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin with actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond with the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

3.2.6.2. Flight Time Simulation

As defined in Section 3.1, flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver and the output pin of the driver crossing V_{REF}, assuming it drives a test load. The timings in the tables and topologies discussed in this guideline assume that the actual system load is 50 Ω and is equal to the test load. Although the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 29 Ω since the driver effectively "sees" a 56 Ω termination resistor in parallel with a 60 Ω transmission line on the Intel PGA370 socket.

Figure 76. Test Load vs. Actual System Load



The previous figure shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. T_{CO} timings are specified at the driver pin output. $T_{FLIGHT-SYSTEM}$ usually is reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers (T_{CO}, $T_{FLIGHT-SYSTEM}$) include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid double counting. T_{REF} is defined as the time required for the driver output pin to reach the measurement voltage, V_{REF}, starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load for T_{CO}. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following valid delay equation is satisfied:

Equation 8. Valid Delay Equation

$$\text{Valid delay} = T_{CO} + T_{FLIGHT-SYS} - T_{REF} = T_{CO-MEASURED} + T_{FLIGHT-MEASURED}$$

This valid delay equation yields the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

3.2.6.3. Flight Time Hardware Validation

When a measurement is made in the actual system, T_{CO} and flight time do not need T_{REF} correction since these are the actual numbers. These measurements include all of the effects pertaining to the driver-system interface, and the same is true for T_{CO}. Therefore, the sum of the measured T_{CO} and the measured flight time must be equal the valid delay calculated previously.

3.3. Theory

3.3.1. AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines the following:

- Termination voltage (V_{TT})
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT})
- Processor termination resistance (R_{TT})
- Input low voltage (V_{IL})
- Input high voltage (V_{IH})
- NMOS on resistance (RON_N)
- PMOS on resistance (RON_P)
- Edge rate specifications
- Ringback specifications
- Overshoot/undershoot specifications.
- Settling limit

3.3.2. Timing Requirements

The system timing for AGTL+ depends on many things. The following elements combine to determine the maximum and minimum frequencies supportable by the AGTL+ bus:

- Timing range for each agent in the system
  - Clock to output [T_{CO}] (Note that the system load is likely to differ from the "specification" load, so the T_{CO} observed in the system might differ from the T_{CO} of the specification.)
  - Minimum required setup time to clock [T_{SU_MIN}] for each receiving agent
- Range of flight time between each component, including
  - Propagation velocity for the loaded printed circuit board [S_{EFF}]
  - Board loading effect on the effective T_{CO} in the system
- Amount of skew and jitter in system clock generation and distribution
- Changes in flight time due to crosstalk, noise, and other effects

3.3.3. Crosstalk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies traditionally used in personal computer designs, so designers using AGTL+ must be more aware of crosstalk than they may have been in previous designs.

Crosstalk is caused through capacitive and inductive coupling between networks. Crosstalk appears as both backward and forward crosstalk. Backward crosstalk creates an induced signal in a victim network that propagates in a direction opposite to that of the aggressor's signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network. Therefore, it sends signals in both directions on the aggressor's network. Figure 77 shows a driver on the aggressor network and a receiver on the victim network, neither of which is at a network end. The signal propagating in each direction causes crosstalk on the victim network.

Figure 77. Aggressor and Victim Networks

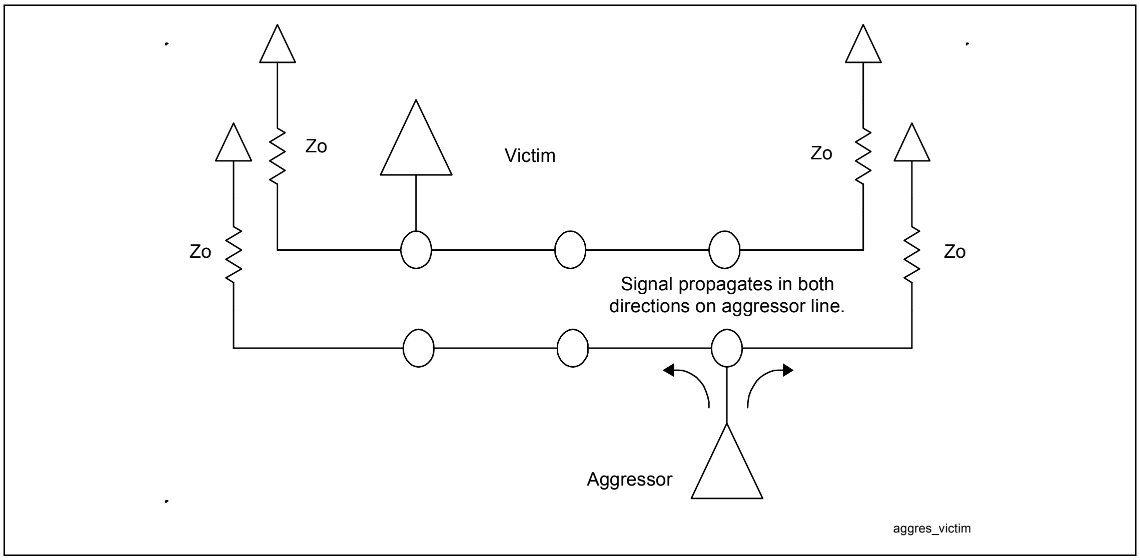
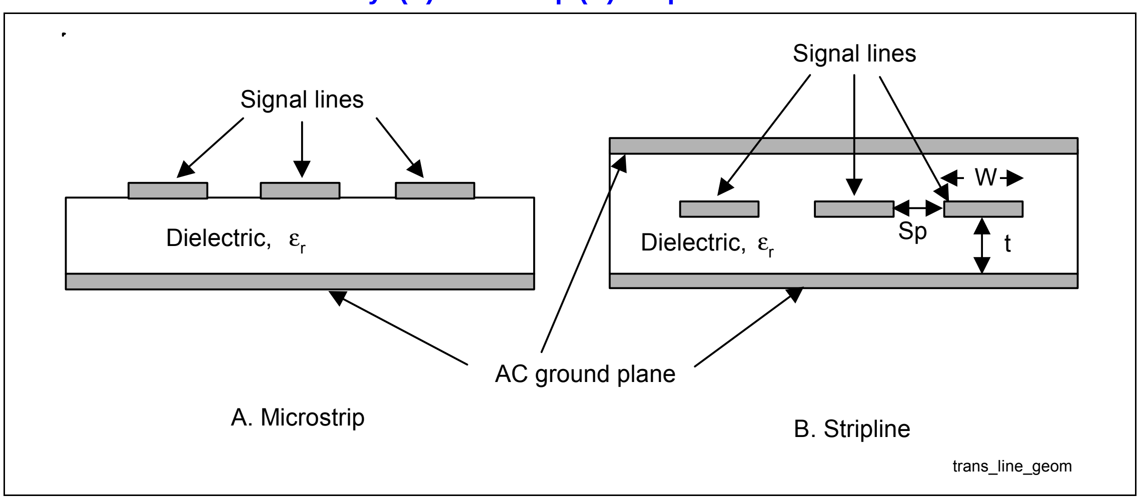


Figure 78. Transmission Line Geometry: (A) Microstrip (B) Stripline



Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because crosstalk coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors at least five line widths away from the victim. The maximum crosstalk occurs when all aggressors are switching in the same direction at the same time.

The crosstalk that occurs internally in the IC packages also can affect the signal quality.

Backward crosstalk is present in both stripline and microstrip geometry's (see Figure 78). Stripline geometry differs from microstrip geometry in that the former requires stripping a layer away to see the signal lines. The backward-coupled amplitude is proportional to the backward crosstalk coefficient, the aggressor's signal amplitude, and the coupled length of the network, up to a maximum that depends on the rise/fall time of the aggressor's signal. Backward crosstalk reaches a maximum (and remains constant) when the propagation time on the coupled network length exceeds one-half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor to be from 0% to 100% voltage swing and the fall time on an unloaded coupled network, then:

Length for max. backward crosstalk = (½ × fall time) / Board delay per unit length

The following example calculation results when the fast corner fall time is 3 V/ns and the board delay is 175 ps/inch (2.1 ns/foot):

Fall time = 1.5 V / 3 V/ns = 0.5 ns

Length for max. backward crosstalk = (½ × 0.5 ns × 1000 ps/ns) / 175 ps/in = 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This causes backward crosstalk from segments on two sides of a driver. The pulses from the backward crosstalk travel toward each other, meet, and **add** at certain moments and positions on the bus. This can double the voltage (i.e., noise) from crosstalk.

3.3.3.1. Potential Termination Crosstalk Problems

It may not be suitable to utilize commonly used "pull-up" resistor networks for AGTL+ termination. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14-pin and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

3.4. More Details and Insight

3.4.1. Textbook Timing Equations

The “textbook” equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations of timing margin based on the component parameters. These equations are as follows:

Equation 9. Intrinsic Impedance

$Z_0 = (L_0 / C_0)^{1/2}$ (Ω)

Equation 10. Stripline Intrinsic Propagation Speed

$S_{0\_STRIPLINE} = 1.017 \times \varepsilon_r^{1/2}$ (ns/ft)

Equation 11. Microstrip Intrinsic Propagation Speed

$S_{0\_MICROSTRIP} = 1.017 \times (0.475 \times \varepsilon_r + 0.67)^{1/2}$ (ns/ft)

Equation 12. Effective Propagation Speed

$S_{EFF} = S_0 \times (1 + (C_D / C_0))^{1/2}$ (ns/ft)

Equation 13. Effective Impedance

$Z_{EFF} = Z_0 / (1 + (C_D / C_0))^{1/2}$ (Ω)

Equation 14. Distributed Trace Capacitance

$C_0 = S_0 / Z_0$ (pF/ft)

Equation 15. Distributed Trace Inductance

$L_0 = 12 \times Z_0 \times S_0$ (nH/ft)

The symbols for Equations 8–15 are as follows:

- S_0 Speed (in ns/ft) of the signal on an unloaded PCB. This is referred to as the board propagation constant.
- $S_{0\_MICROSTRIP}$, $S_{0\_STRIPLINE}$ Speed (in ns/ft) of the signal on an unloaded microstrip or stripline trace on the PCB
- Z_0 Intrinsic impedance (in Ω) of the line. This is a function of the dielectric constant (ε_r), line width, line height, and line space from the plane(s). The equations for Z_0 are not included in this document. For these equations, see the *MECL System Design Handbook* by William R. Blood, Jr.
- C_0 Distributed trace capacitance of the network (in pF/ft)
- L_0 Distributed trace inductance of the network (in nH/ft)
- C_D Sum of the capacitance of all devices and stubs, divided by the length of the network’s trunk, not including the portion connecting the end agents to the termination resistors (in pF/ft)
- S_{EFF} and Z_{EFF} Effective propagation constant and impedance of the PCB when the board is “loaded” with the components

3.4.2. Effective Impedance and Tolerance/Variation

The impedance of the PCB must be controlled when the PCB is fabricated. The best impedance control specification method for each situation must be determined. The use of stripline transmission lines (where the trace is between two reference planes) is likely to yield better results than microstrip (where the trace is on an external layer, using an adjacent plane for reference, with solder mask and air on the other side of the trace). This is due partly to the difficulty of precisely controlling the dielectric constant of the solder mask as well as the difficulty of limiting the plated thickness of microstrip conductors, which can substantially increase crosstalk.

The recommended effective line impedance (Z_{EFF}) is 60 Ω ± 15%, where Z_{EFF} is defined by Equation 13. Effective Impedance.

3.4.3. Power/Reference Planes, PCB Stack-Up, and High-Frequency Decoupling

3.4.3.1. Power Distribution

Designs using the Pentium III processor require several different voltages. The following paragraphs describe some effects of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

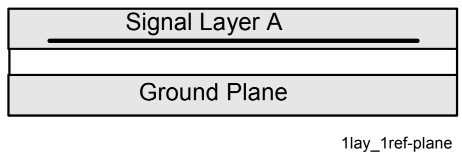
The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes is used as an "AC ground" reference for traces to control trace impedance on the board, then the plane must be AC-coupled to the system ground plane. This method may require more total layers in the PCB than other methods. Copper with a thickness of 1-ounce/ft^2 is recommended for all power and reference planes.

A second method of power distribution is to use partial planes in the immediate area needing power, and to place these planes on a routing layer, on an as-needed basis. These planes still must be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing the area that can be used to route traces. These partial planes also may change the impedance of adjacent trace layers. (For instance, the impedances may have been calculated for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.)

3.4.3.2. Reference Planes and PCB Stack-Up

It is **strongly recommended** that baseboard stack-up be arranged such that AGTL+ signals are referenced to a ground (V_{SS}) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path, that can lead to large SSO effects that degrade the timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will subject the platform to a risk that is highly unpredictable in pre-layout simulation. The following figure shows the ideal case, where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 79. One Signal Layer and One Reference Plane



When it is not possible to route the entire AGTL+ signal on a single V_{SS} referenced layer, there are methods of reducing the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 80). Figures 81 through 83 show other methods of minimizing layer switch discontinuities, but they may be less effective than the following figure. In this case, the signal still references the same type of reference plane (i.e., ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

Figure 80. Layer Switch with One Reference Plane

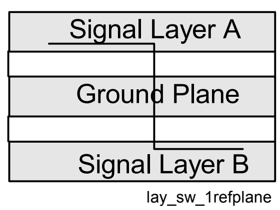
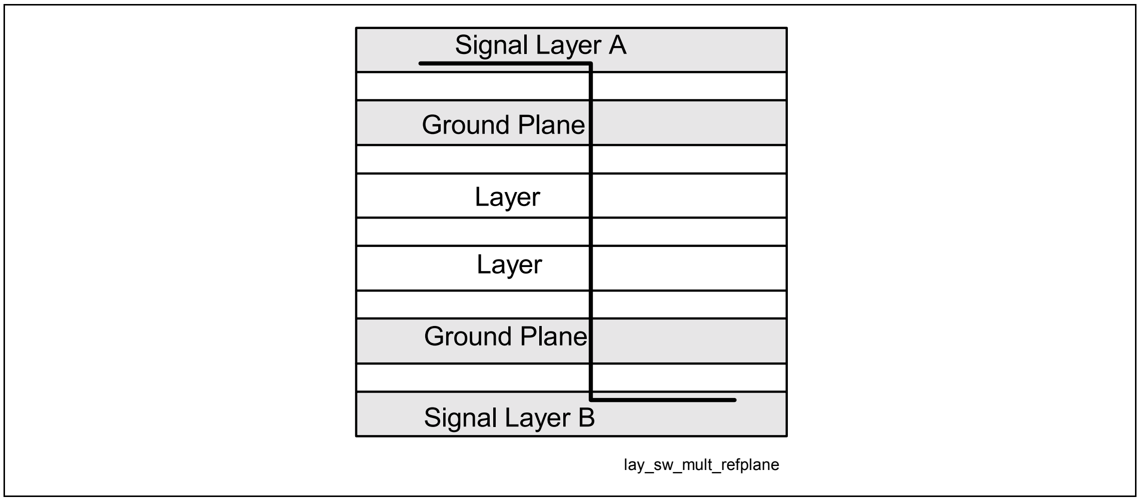


Figure 81. Layer Switch with Multiple Reference Planes (Same Type)



When routing and stack-up constraints require that an AGTL+ signal reference V_{CC} or multiple planes, special care must be taken to minimize the SSO effect on timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur, as shown in the following two figures. Again, such decoupling should be in the vicinity of the signal transition via and should use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps, it is advisable to space the V_{SS} and V_{CC} vias as closely as possible and/or use dual vias, since the via inductance may sometimes exceed the actual capacitor inductance.

Figure 82. Layer Switch with Multiple Reference Planes

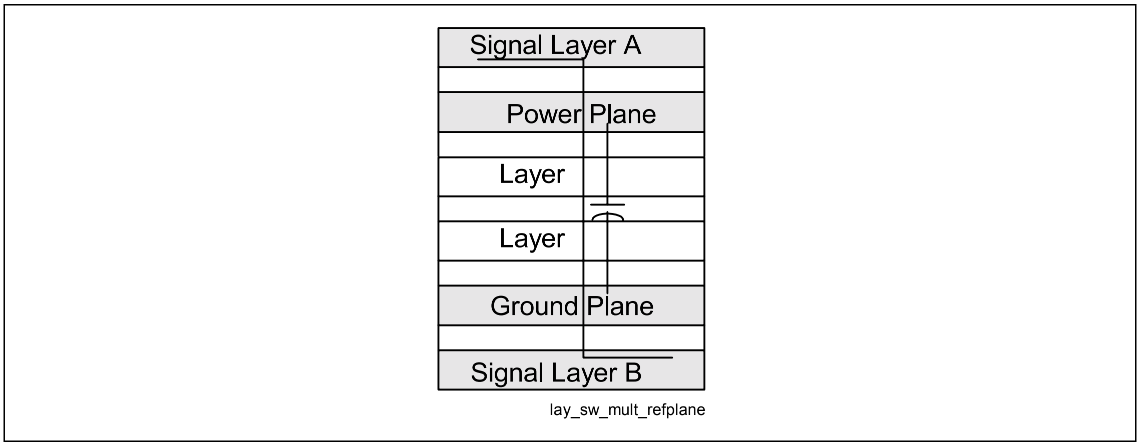
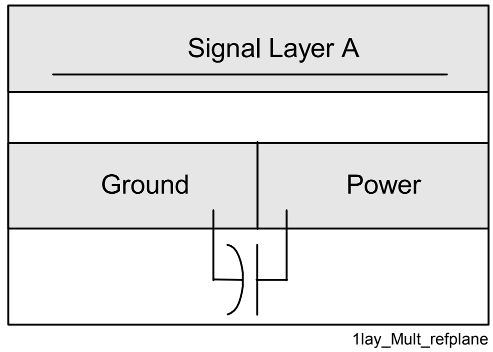


Figure 83. One Layer with Multiple Reference Planes



3.4.3.3. High-Frequency Decoupling

This section contains several high-frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities also may occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across VCC_{CORE} and ground within the Intel PGA370 socket cavity and mounted on the primary side of the motherboard will minimize discontinuity in the signal's reference plane at this junction. For the Intel 820E chipset/FC-PGA decoupling guidelines, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at http://developer.intel.com/design/chipsets/designex/298178.htm.

Transmission line geometry also influences the return path of the reference plane. The following decoupling recommendations take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling among all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 82820 MCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

3.4.4. Clock Routing

Analog simulations are required to ensure that the clock net signal quality and skew are acceptable. The system clock skew must be minimized. (The calculations and simulations for the example topology in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure that these same values are valid assumptions. Each processor's datasheet specifies the clock signal quality requirements. To help meet these specifications, comply with the following general guidelines:

- Tie the clock driver outputs if the clock buffer supports this mode of operation.
- Match the electrical length and type of traces on the PCB. (Microstrip and stripline may have different propagation velocities.)
- Maintain consistent impedance for the clock traces.
  - Minimize the number of vias in each trace.
  - Minimize the number of different trace layers used to route the clocks.
  - Keep other traces away from clock traces.
- Lump the loads at the end of the trace if multiple components are to be supported by a single clock output.
- Have equal loads at the end of each network.

The ideal way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero-skew clock driver. When deviations from the ideal are required, a good compromise is to go from a single layer to a pair of layers adjacent to power/ground planes. The fewer number of layers on which the clocks are routed, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length and parallel ground trace for the **total length of each** clock ensures a low-inductance ground return and produces the minimum current path loop area. (The parallel ground trace will have lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

For the Intel 820E chipset/FC-PGA clock routing guidelines, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at http://developer.intel.com/design/chipsets/designex/298178.htm.

3.5. Definitions of Flight Time Measurements/Corrections and Signal Quality

Acceptable signal quality must be maintained over all operating conditions to ensure reliable operation. Signal quality is defined by four parameters: overshoot, undershoot, settling limit, and ringback. Timings are measured at the pins of the driver and receiver, while signal integrity is observed at the receiver chip pad. When signal integrity at the pad violates the following guidelines and adjustments must be made to flight time, the adjusted flight time obtained at the chip pad can be assumed to have been observed at the package pin, usually with a small timing error penalty.

3.5.1. V_{REF} Guard Band

To account for noise sources that may affect the way an AGTL+ signal becomes valid at a receiver, V_{REF} is shifted by ΔV_{REF} for measuring the minimum and maximum flight times. The V_{REF} guard band region is bounded by $V_{REF} - \Delta V_{REF}$ and $V_{REF} + \Delta V_{REF}$. ΔV_{REF} has a value of 100 mV, which accounts for the following noise sources:

- Motherboard coupling
- V_{TT} noise
- V_{REF} noise

3.5.2. Ringback Levels

The example topology covered in this guideline assumes a ringback tolerance allowed to within 200 mV of 2/3 V_{TT}. Since V_{TT} is specified with an approximate total tolerance of ±11%, this implies a 2/3 V_{TT} (V_{REF}) range, from approximately 0.89 V to 1.11 V. This sets the absolute ringback limits as follows:

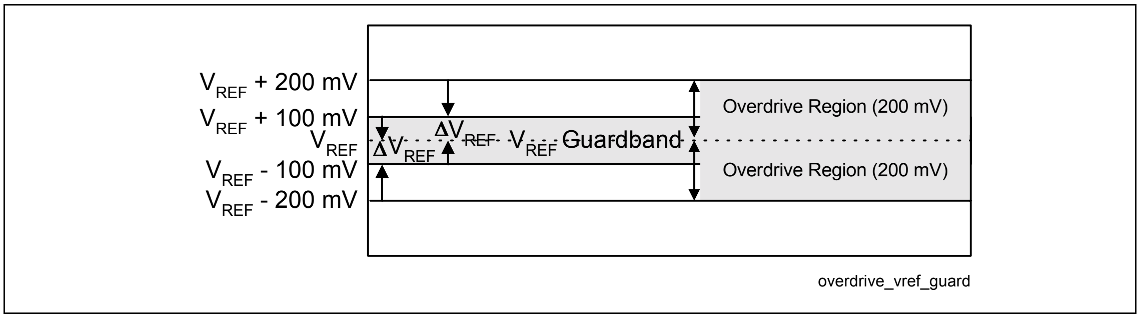
- 1.3 V (1.1 V + 200 mV) for rising-edge ringback
- 0.69 V (0.89 V – 200 mV) for falling-edge ringback

A violation of these ringback limits requires flight time correction as documented in the *Intel® Pentium® III Processor Developer's Manual*.

3.5.3. Overdrive Region

The overdrive region is the voltage range at a receiver, from V_{REF} to V_{REF} + 200 mV, for a low-to-high-going signal, and from V_{REF} to V_{REF} – 200 mV for a high-to-low-going signal. The overdrive regions encompass the V_{REF} guard band, so when V_{REF} is shifted by ΔV_{REF} for timing measurements, the overdrive region **does not** shift by ΔV_{REF}. Figure 84 depicts this relationship. Corrections for edge rate and ringback are documented in the *Intel® Pentium® II Processor Developer's Manual*. However, there is an exception to the documented correction method: The *Intel® Pentium® III Processor Developer's Manual* states that extrapolations should be made from the last crossing of the overdrive region back to V_{REF}. Simulations performed on this topology should extrapolate back to the appropriate V_{REF} guard band boundary, and not to V_{REF}. So, for maximum rising-edge correction, extrapolate back to $V_{REF} + \Delta V_{REF}$. For maximum falling-edge corrections, extrapolate back to $V_{REF} - \Delta V_{REF}$.

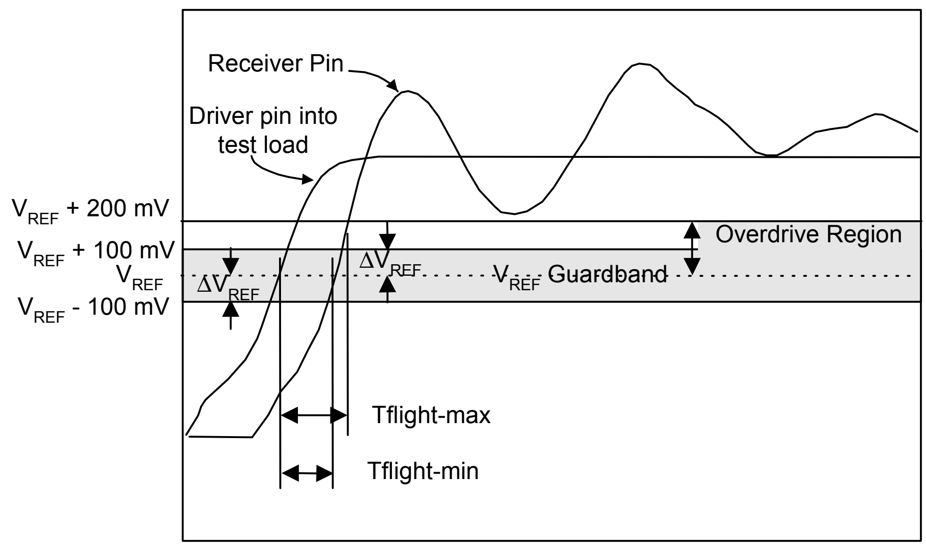
Figure 84. Overdrive Region and V_{REF} Guard Band



3.5.4. Flight Time Definition and Measurement

Timing measurements consist of minimum and maximum flight times, to take into account the fact that devices can turn on or off anywhere in a V_{REF} guard band region. This region is bounded by $V_{REF} - \Delta V_{REF}$ and $V_{REF} + \Delta V_{REF}$. The minimum flight time for a rising edge is measured from the time the driver crosses V_{REF} when terminated to a test load, to the time when the signal first crosses $V_{REF} - \Delta V_{REF}$ at the receiver (see Figure 85). Maximum flight time is measured to the point where the signal first crosses $V_{REF} + \Delta V_{REF}$, assuming that the ringback, edge rate, and monotonicity criteria are met. Similarly, minimum flight time measurements for a falling edge are taken at the $V_{REF} + \Delta V_{REF}$ crossing, and maximum flight time is taken at the $V_{REF} - \Delta V_{REF}$ crossing.

Figure 85. Rising-Edge Flight Time Measurement



3.6. Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and allocating the necessary time for correctly designing a board layout will give the designer the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

4. Clocking

4.1. Clock Generation

Two clock generator components are required in an Intel 820E chipset-based system. The Direct RDRAM clock generator (DRCG) generates clock for the Direct RDRAM interface, while the CK133 component generates clocks for the rest of the system. Clock synthesizers that meet the Intel CK98 Clock Specification are suitable for an Intel 820E chipset-based system. The CK133 generates the clocks listed in the following table.

Table 55. Intel® 820E Chipset Platform System Clocks

Number	Name on CK133	Used for	Routed to	Name on Receiver	Frequency	Voltage
4	CPUCLK[0–3]	System bus clock	2 processors	CLK	100/133 MHz	2.5 V
			MCH	HCLKIN		
			ITP	BCLK		
3	APIC[0–2]	APIC bus clock	2 processors	PICCLK	33 MHz	2.5 V
			ICH2	APICCLK		
8	PCICLK[1–7,F]	PCI bus clock	5 PCI devices	CLK	33 MHz	3.3 V
		PCI, LPC, FWH Flash BIOS bus clock	ICH2	PCICLK		
		FWH Flash BIOS I/F clock	FWH Flash BIOS	CLK		
		LPC I/F clock	LPC	CLK		
4	3V66[0–3]	Hub interface/AGP bus clock	MCH	CLK66	66 MHz	3.3 V
		Hub interface clock	ICH2	CLK66		
		AGP bus clock	AGP device/ slot	CLK		
		Unused	N/A	N/A		
2	REF[0–1]	Internal ICH2 logic	ICH2	CLK14	14 MHz	3.3 V
		Internal super I/O logic	Super I/O	Vendor specific		
1	48MHz	USB	ICH2	CLK48	48 MHz	3.3 V
2	CPU_DIV2[0–1]	DRCG reference clock	DRCG	REFCLK	50/66 MHz	2.5 V
		Unused	N/A	N/A		

The CK133 is a mixed-voltage component. Some of the output clocks are 3.3 V, and some of the output clocks are 2.5 V. As a result, the CK133 device requires both 3.3 V and 2.5 V. These power supplies should be a clean as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

The MCH uses the same clock for hub interface and AGP. It is important that the hub interface/AGP clocks are routed so as to ensure that the skew requirements are satisfied as follows:

- Between the MCH hub interface/AGP clock and the AGP connector (or device)
- Between the MCH hub interface/AGP clock and the ICH2 hub interface clock

The DRCG reference clock operates at one-half the processor clock frequency. It is an input into the DRCG and is used to generate the Direct RDRAM clock-to-master differential pair (CTM, CTM#).

The DRCG generates one pair of differential Direct RDRAM clocks (CTM, CTM#) from the reference clock generated by the CK133. In addition, the DRCG uses phase information provided by the MCH to phase-align the Direct RDRAM clock with the processor clocks. This phase alignment information is provided to the DRCG via the SYNCLKN and PCLKM pins.

Figure 86. Intel® 820E Chipset Platform Clock Distribution

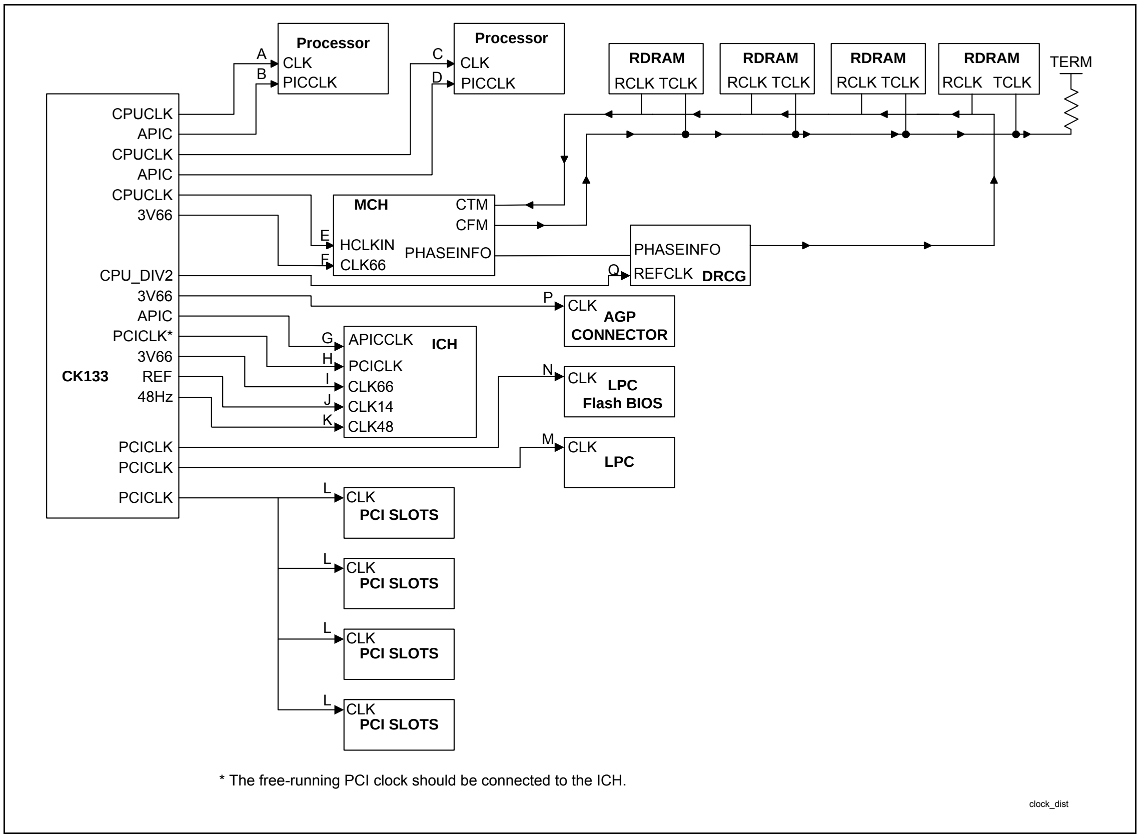


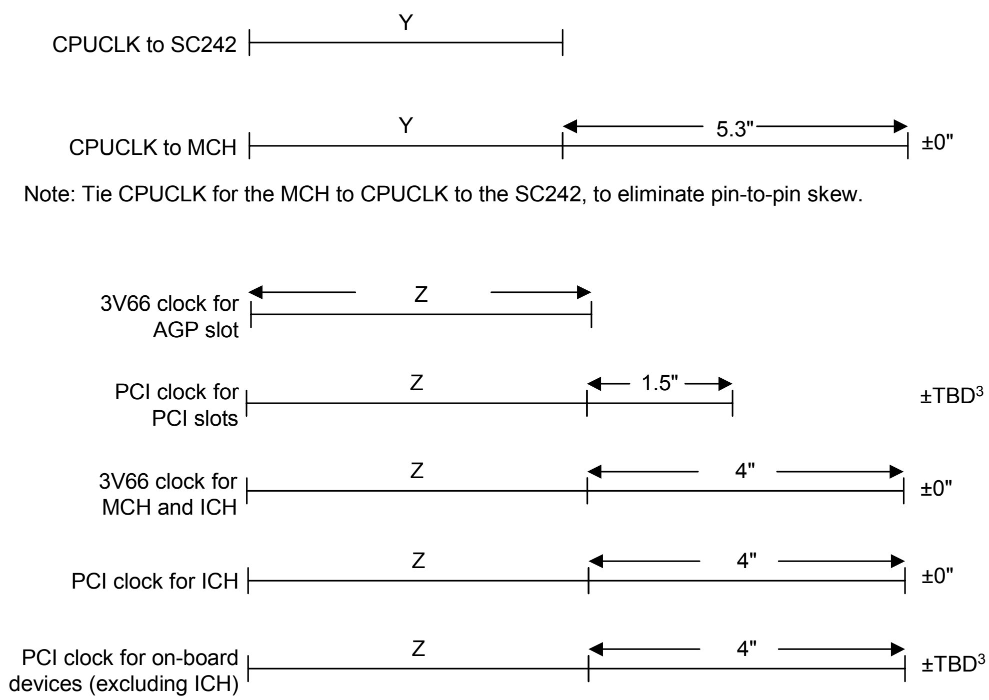
Table 56. Intel® 820E Chipset Platform Clock Skews

Clock Symbols (see Figure 86)	Relationship	Skew						Notes
		Pin-to-Pin (ps)		Board (ps)		Total (ps)		
		Min.	Max.	Min.	Max.	Min.	Max.	
A leads C A leads E (or C leads E)	PGA370 HCLK to PGA370 HCLK (DP only) and PGA370 HCLK to MCH HCLK (DP only)	-175	+175	-125	+125	-300	+300	1, 7
A leads E	PGA370 HCLK to MCH HCLK (UP only)	0	0	-125	+125	-125	+125	2, 3, 7
P leads F	MCH CLK66 to AGP graphics device AGPCLK	0	0	-125	+125	-125	+125	4, 8
L leads another L (or L leads H)	PCICLK to PCICLK	-500	+500	-1500	+1500	-2000	+2000	
I leads H	ICH2 CLK66 leads ICH2 PCICLK	+1500	+4000	-500	+500	+1000	+4500	
F leads I	ICH2 CLK66 to MCH CLK66	-250	250	-125	+125	-375	+375	8
Worst-case skew between H, L, M, and N	Worst-case FWHCLK, LPCCLK, PCICLK	-500	+500	-1500	+1500	-2000	+2000	5
B leads D B leads G	processor PICCLK leads processor PICCLK and processor PICCLK leads ICH2 APICCLK	-250	+250	-125	+125	-375	+375	6

NOTES:
1. DP only
2. UP: MCH and processor clock drivers are tied together to eliminate pin-to-pin skew. -175 and +175 pin-to-pin skew apply only to DP.
3. UP only
4. Clock drivers tied together to eliminate pin-to-pin skew.
5. The skew between any PCICLK clocks on any two inputs in the system
6. The skew between any APIC clocks on any two inputs in the system
7. If SSC is enabled, an additional ±40 ps must be added to the pin-to-pin skew.
8. If SSC is enabled, an additional ±60 ps must be added to the pin-to-pin skew.

The following figure shows the Intel 820E chipset clock length routing guidelines.

Figure 87. Intel® 820E Chipset Clock Routing Guidelines[1,2]



Note:
1. Tie 3V66 clock for MCH to 3V66 clock for AGP connector, to eliminate pin-to-pin skew.
2. These calculations are based on 150-ps/in trace velocity.
3. TBD value derived from PCI Revision 2.2 Specification, which allows for max. ±2-ns clock skew.

820_clk_route

Table 57. Intel® 820E Chipset Platform System Clock Cross-Reference

CK133/DRCG Pin Name	Component	Pin Name
PCICLK	PCI slot	CLK
	PCI slot	CLK
	PCI slot	CLK
	PCI slot	CLK
	PCI slot	CLK
	ICH2	PCICLK-F
	LPC super I/O	CLK
	FWH Flash BIOS	CLK
3V66	MCH	GCLKIN
	ICH2	CLK66
	AGP connector (on-board device)	CLK
48MHz	ICH2	CLK48
CPUCLK	Processor	BCLK
	Processor	BCLK
	MCH	HCLKIN
CPU_div2	DRCG	Refclk
APIC	Processor	PICCLK
	Processor	PICCLK
	ICH2	APICCLK
Clk/ClkB1	RDRAMs	
	MCH	CTM/CTM#
CFM/CFM#1,2	RDRAMs	
PclkM	MCH	HCLKOUT
SynclkN	MCH	RCLKOUT

NOTES:

1. Differential clocking pair
2. CFM/CFM# driven by MCH.

4.2. Component Placement and Interconnection Layout Requirements

The layout requirements for each interconnection are explained in detail in the following sections:

- Crystal to CK133
- CK133 to DRCG
- MCH to DRCG
- DRCG to RDRAM channel

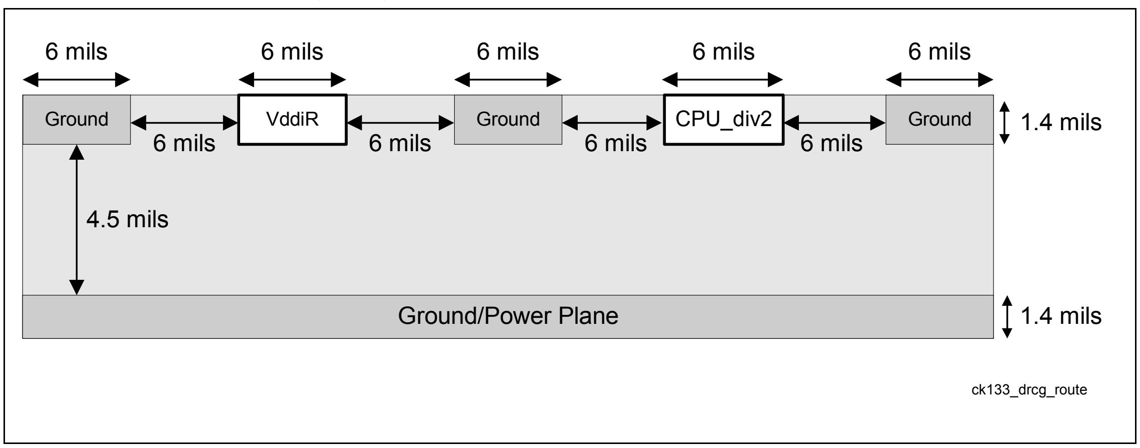
4.2.1. 14.318 MHz Crystal to CK133

The distance between the crystal and the CK133 should be minimized. The maximum trace length is 500 mils.

4.2.2. CK133 to DRCG

- Processor _div2
- VddIR – Used as a reference for 2.5 V signaling

Figure 88. CK133-to-DRCG Routing Diagram

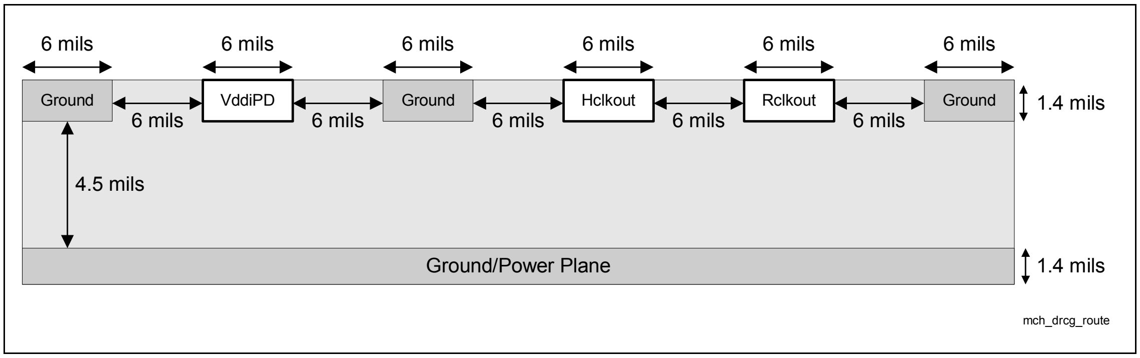


VddIR and CPU_div2 must be routed as shown in Figure 88. Note that the VddIR pin can be connected directly to 2.5 V near the DRCG if the 2.5 V plane extends near the DRCG. However, if a 2.5 V trace must be used, it should originate at the CK133 and be routed as shown.

4.2.3. MCH to DRCG

- PclkM
- PclkN
- VddIPD

Figure 89. MCH-to-DRCG Routing Diagram

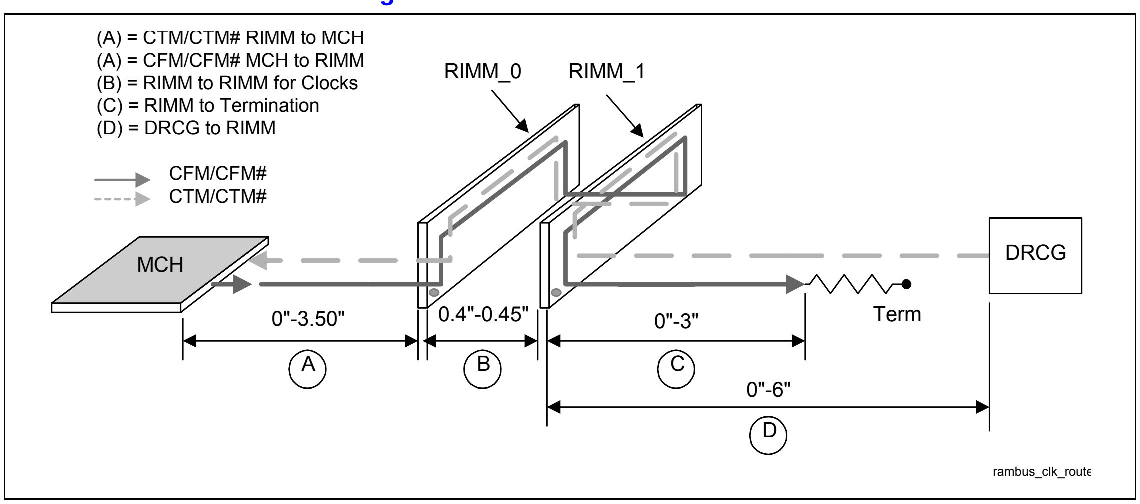


Hclkout, Rclkout, and VddIPD should be routed as shown in Figure 89. Note that the VddIPD pin can be connected directly to 1.8 V near the DRCG, if the 1.8 V plane extends near the DRCG. However, if a 1.8 V trace must be run, it should originate at the MCH and be routed as shown.

The maximum length for Hclkout and Rclkout is 6 inches. Additionally, Hclkout and Rclkout must be length-matched (to each other) within 50 mils. These signals should be routed on the same layer. If the signals must switch layers, then **both** signals should change layers together.

If VddIPD is connected to the 1.8 V plane using a via (e.g., if a trace is not run from the MCH), Hclkout and Rclkout must still be routed differentially and ground-isolated.

Figure 90. Direct RDRAM* Clock Routing Dimensions



4.2.4. DRCG-to-RDRAM Channel

The Direct RDRAM clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance-matched transmission lines. Direct RDRAM clocks begin at the end of the Direct RDRAM channel and propagate to the controller as CTM/CTM# (see Figure 90), where they loop back as CFM/CFM#. The following table lists the placement guidelines.

Table 58. Placement Guidelines for Motherboard Routing Lengths (Direct RDRAM* Clock Routing Length Guidelines)

Clock	From	To	Length (inches)	Section (see Note)
CTM/CTM#	DRCG	Last RIMM connector	0.000 – 6.000	D
	RIMM	RIMM	0.400 – 0.450	B
	1st RIMM connector	Chipset	0.000 – 3.500	A
CFM/CFM#	Chipset	1st RIMM connector	0.000 – 3.500	A
	RIMM	RIMM	0.400 – 0.450	B
	Last RIMM connector	Termination	0.000 – 3.000	C

NOTES: Refer to Figure 90.

Trace Geometry

In Sections A and D (previous figure), the clock signals (CTM/CTM# and CFM/CFM#) must be 14 mil wide and routed as shown in Figure 91. For all other sections (B and C), the clock signals must be routed with 18 mil-wide traces. A 22 mil ground isolation trace must be routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via every 1 inch. A 6 mil gap is required between the clock signals and the ground isolation traces. For section A in the previous Figure 90, 0.021 inch of CLK per 1 inch of RSL trace length must be added to compensate for the clock's faster trace velocity, as described in Section 2.7.2.1. The CTM/CTM# and the CFM/CFM# differential signal pairs must be length-matched to ±2 mils in line section A. For line section B, use the trace length methods in Section 2.7.2.1. For section D, the trace length matching for CTM/CTM# is ±2 mils, and for section C, ±2 mil trace length matching is required for the CFM/CFM# signals.

The CTM/CTM# signals must be ground-referenced (with a continuous ground island/plane) from the DRCG to the last RIMM.

4.2.5. Trace Length

For section A in Figure 90 (first RIMM to MCH, and MCH to first RIMM), CTM/CTM# and CFM/CFM# must be length-matched within ±2 mils. (Exact trace length matching is recommended.) Package trace compensation (as described in Section 2.7.2.1), via compensation, and RSL signal layer alternation must also be completed on the clock signals. Additionally, 0.021 inch of CLK per 1 inch of RSL trace length must be added to compensate for the clock's faster trace velocity, as described in Section 2.7.2.1.

For line section B (Figure 90) (RIMM to RIMM), the clock signals must be matched within ±2 mils to the trace length of every RSL signal. Exact length matching is preferred.

For line section D (DRCG to last RIMM), the CTM/CTM# must be length-matched within ±2 mils. (Exact matching is recommended.) For section C, ±2 mil trace length matching is required for the CFM/CFM# signals.

Note: The total trace length matching for the entire CTM/CTM# signal trace (sections A+B+D) and for the CFM/CFM# signal trace (sections A+B) is ±2 mils. (Exact length matching is recommended.)

Figure 91. Differential Clock Routing Diagram (Sections A, C & D)

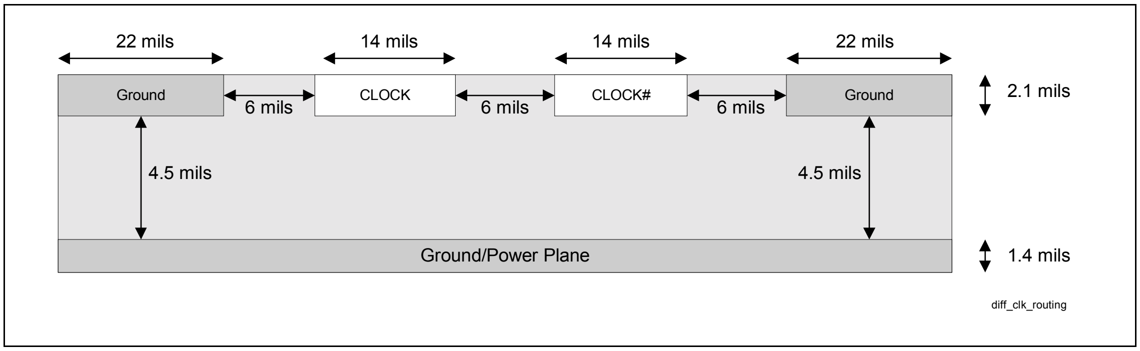
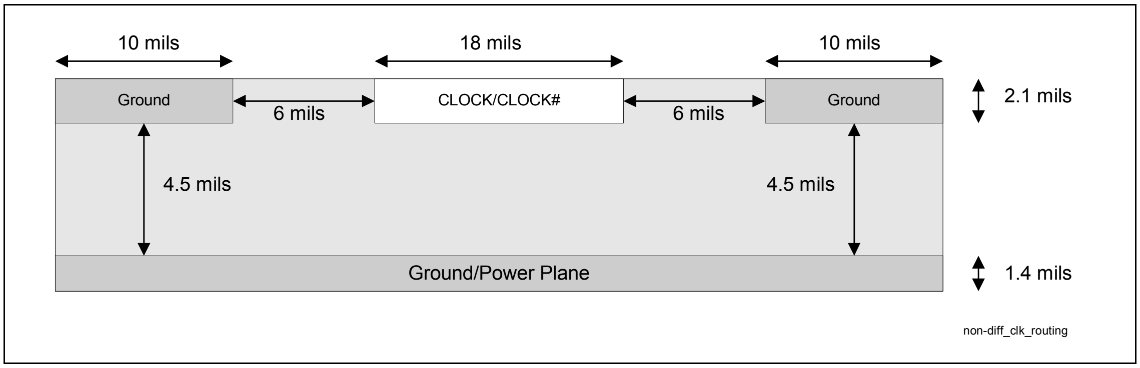
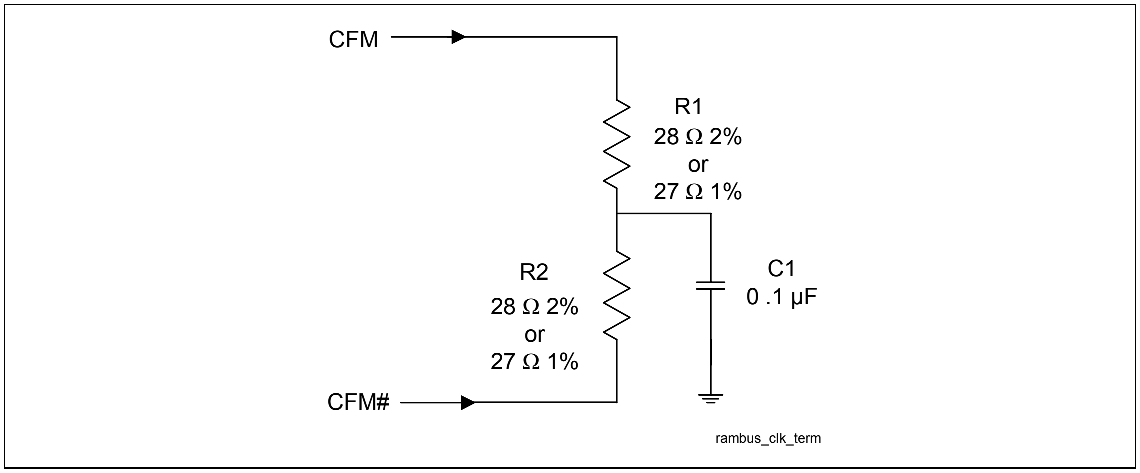


Figure 92. Non-Differential Clock Routing Diagram (Section B)



The CFM/CFM# differential pair signals require termination using either 27 Ω, 1% or 28 Ω, 2% resistors and a 0.1 µF capacitor, as shown in the following figure.

Figure 93. Termination for Direct RDRAM* Clocking Signals CFM/CFM#



4.3. DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in the following figure. The values for the elements are listed in Table 59.

Figure 94. DRCG Impedance Matching Network

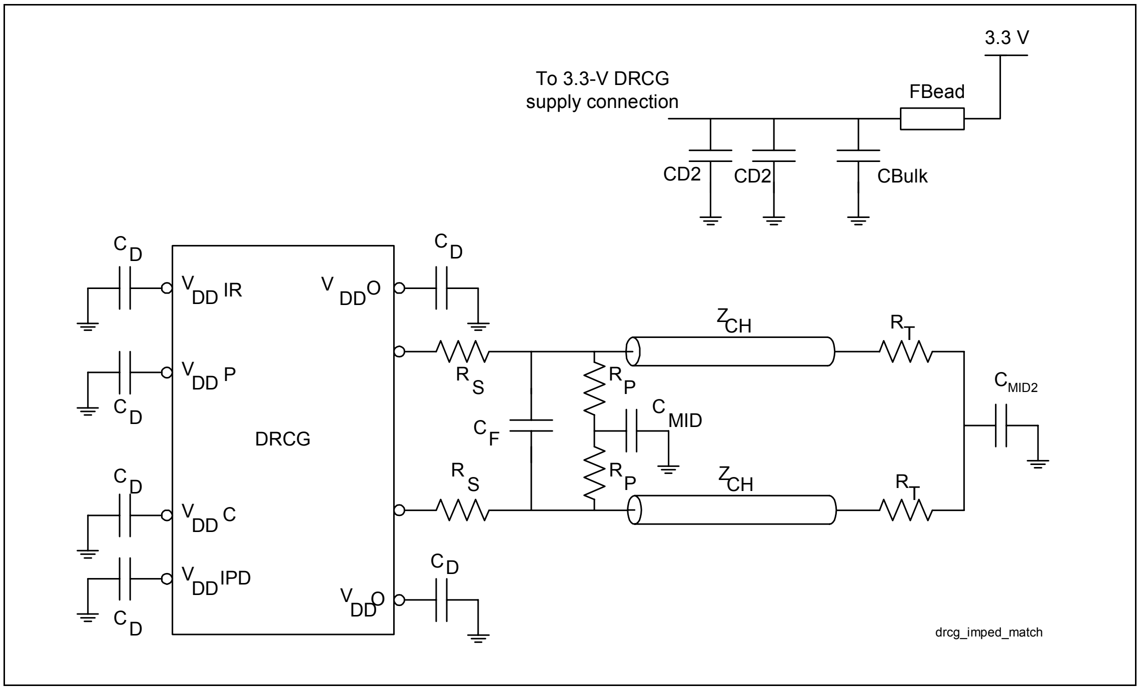


Table 59. External DRCG Component Values[1,2]

Component	Nominal Value	Notes
CD	0.1 µF	Decoupling caps to ground
RS	39 Ω	Series termination resistor
RP	51 Ω	Parallel termination resistor
CMID, CMID2	0.1 µF	Virtual ground caps
RT	27 Ω	End of channel termination
CF	4 pF	Do not stuff
Fbead	50 Ω at 100 MHz	Ferrite bead
CD2	0.1 µF	Additional 3.3 V decoupling caps
Cbulk	10 µF	Bulk cap on device side of ferrite bead

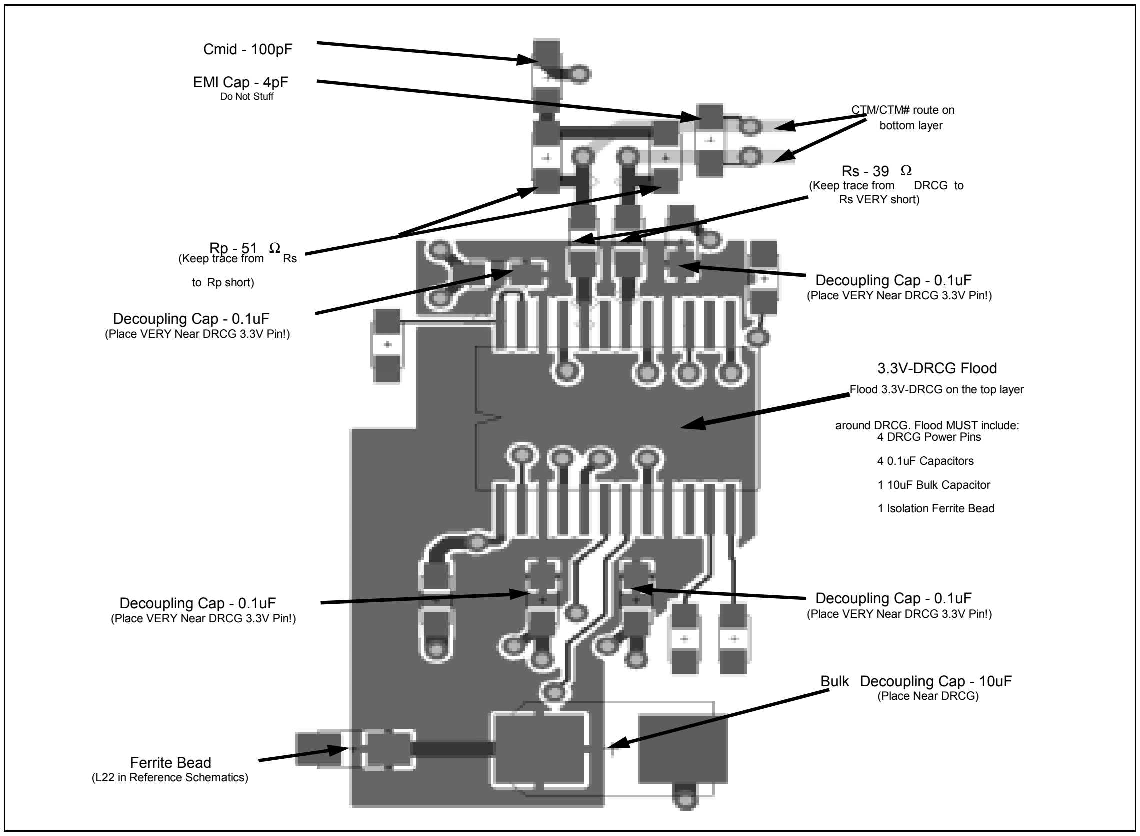
NOTES:

1. The ferrite bead and 10 µF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system.
2. For DRCG decoupling, 0.1 µF capacitors are better than 0.01 µF or 0.001 µF caps.

The circuit in Figure 94 must match the impedance of the DRCG to the 28 Ω channel impedance. For more detailed information, refer to the *Direct Rambus Clock Generator Specification*.

4.3.1. DRCG Layout Example

Figure 95. DRCG Layout Example



4.4. AGP Clock Routing Guidelines

The AGP clock must be routed with 20 mil spacing to all other signals, and it must meet the length guidelines in Figure 87.

4.5. Clock Routing Guidelines for Intel® PGA370 Designs

For the Intel 820E chipset/FC-PGA clock routing guidelines, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at http://developer.intel.com/design/chipsets/designex/298178.htm.

4.6. Series Termination Resistors for CK133 Clock Outputs

All used outputs require series termination resistors. The recommended resistor values are defined by simulations. The stub length to the CK133 of these resistors can be compromised to make room for decoupling caps. As a rule, keep all resistor stubs within 250 mils of the CK133. If routing rules allow, Rpacks can be used, if power dissipation is not exceeded for the Rpack.

4.7. Unused Outputs

All unused clock outputs must be tied to ground through a series resistor that has approximately the impedance of the output buffer (shown in the following table). These resistors are designed to terminate unused outputs to eliminate EMI.

Table 60. Unused Output Termination

Buffer Name	V_{CC} Range (V)	Impedance (Ω)	If Unused Output Termination to V_{SS} (Ω)
CPU, CPU_Div2, IOAPIC	2.375 – 2.625	13.5 – 45	30
48 MHz, REF	3.135 – 3.465	20 – 60	40
PCI, 3V66	3.135 – 3.465	12 – 55	33

4.8. Decoupling Recommendation for CK133 and DRCG

Some CK133 vendors may integrate the XTAL_IN and XTAL_OUT frequency adjust capacitors. However, pads should be placed on the board for these external capacitors for testing/debug.

To further reduce jitter and voltage supply noise, it is advisable to add a ferrite filter with 2 caps (10 µF and 0.1 µF) on both the 2.5 V and 3.3 V planes, close to the clock devices. This applies to both DRCG and CK133.

4.9. DRCG Frequency Selection and the DRCG+

4.9.1. DRCG Frequency Selection Table and Jitter Specification

To provide additional flexibility in board design, Intel has enabled a variation of the DRCG, called the *DRCG+*. The device has the same specifications, pinout, and form-factor mentioned in the document for the existing DRCG device. Two modifications were made to the DRCG+.

1. The DRCG+ Mult[0:1] select table was changed to modify two of the multiplier ratios. The DRCG+ will support 133/356 MHz using a 66 MHz DRCG+ input clock and a 16/3 multiplier. An additional 9/2 multiplier allows 133/300 MHz (not supported by the Intel 820E chipset). Support for the 300 MHz and 400 MHz memory bus is unchanged. The following table lists the DRCG ratios.

Mult[0:1]	DRCG	DRCG+
0:0	4:1	9:2
0:1	6:1	6:1
1:0	8:3	16:3
1:1	8:1	8:1

2. The Intel 820E chipset supports the following ratios and can be supported by the DRCG and DRCG+ or derivative devices. Contact your DRCG vendor for information on DRCG, DRCG+, and derivative products.

100 MHz Host Bus		133 MHz Host Bus	
Frequency	Multiplier	Frequency	Multiplier
100 / 300	6:1	133 / 266	4:1
100 / 400	8:1	133 / 356	16:3
		133 / 400	6:1

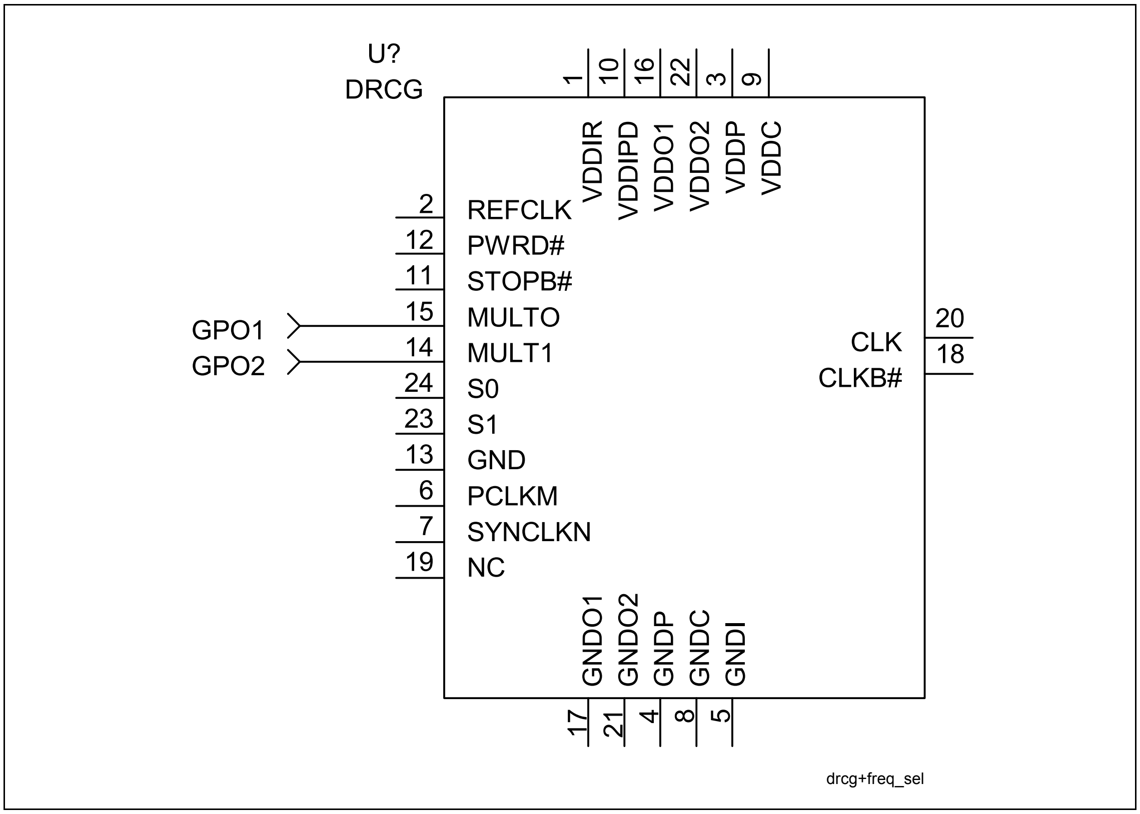
3. The jitter timing specifications were expanded to encompass both the component specification (for DRCG or derivative products) and the channel specification. Follow the component specification when measuring jitter at the DRCG output resistor. Follow the channel jitter guidelines when measuring jitter at the MCH or at the termination for CFM/CFM# on the RDRAM interface.

Output Frequency (MHz)	Component Jitter Specification	Channel Jitter Guidelines
400	50 ps	100 ps
356	60 ps	110 ps
300	70 ps	120 ps
266	80 ps	130 ps

4.9.2. DRCG+ Frequency Selection Schematic

The DRCG+ frequency can be selected using two GPIOs connected to the MULT[0:1] pins, as shown in the following figure. This allows selection of all frequencies supported by the Intel 820E chipset.

Figure 96. DRCG+ Frequency Selection



5. System Manufacturing

5.1. Stack-Up Requirement

The Intel 820E chipset platform requires a board stack-up with a 4.5 mil prepreg. This change in dimension (previously, typically 7 mils) is required because of the signaling environment used for the Direct RDRAM, AGP 2.0, and hub interface. The RDRAM channel is designed for 28 Ω, and mismatched impedance will cause signal reflections that will reduce the voltage and timing margins. For example, with a 2× clock during 400 MHz operation, which equals a 1.25 ns sampling window, only 100 ps is allotted for the total channel timing error. Channel error results not only from PCB impedance, but also from PCB and Z_0 process variation. Therefore, it is critical to attain the required 28 Ω impedance.

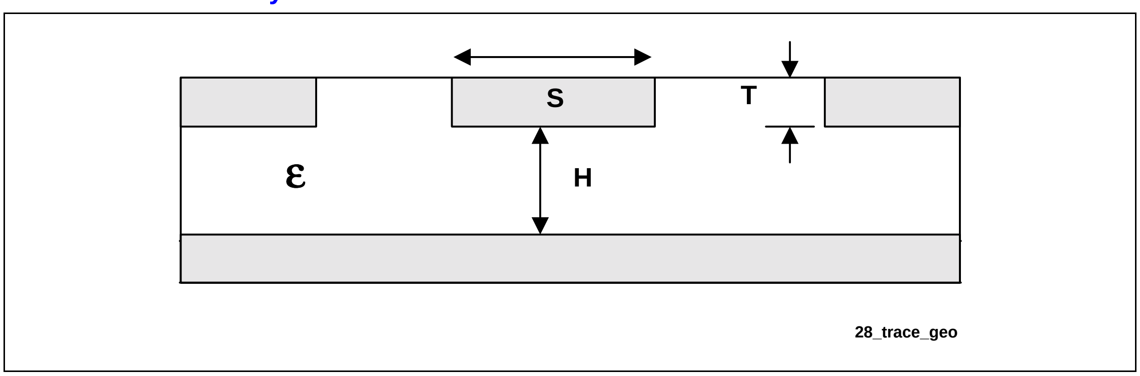
5.1.1. PCB Materials

PCB tolerances determine the Z_0 variation. These tolerances include the trace width, prepreg thickness, plating thickness, and dielectric constant. The prepreg type affects the H tolerance and ε_r, including single-ply, 2-ply, and resin content.

To design to the correct Z_0 variation, the PCBs typically must meet the following specs (see Table 62):

- Height tolerance: ±10% (~0.4 mil)
- Width tolerance: ±2.5% (~0.4 mil)
- ε_r tolerance: ±5% (~0.2)
- Stack-up requirement: 28 Ω ± 10%

Figure 97. 28 Ω Trace Geometry



5.1.2. Design Process

To meet the tight tolerances required, a good design process is as follows:

- Specify the material to be used.
- Calculate the board geometries for the desired impedance or use the example stack-up provided.
- Build test boards and coupons.
- Measure the board impedance using a TDR and follow *Intel's Impedance Test Methodology Document* (located on the developer.intel.com web site).
- Measure geometries with cross section.
- Adjust design parameters and/or material, as required.
- Build a new board and remeasure the key parameters. Be prepared to generate one or two board iterations.

This process will require iteration, as follows: design, build, test, modify, build, test….

5.1.3. Test Coupon Design Guidelines

To deliver reliable systems at increased bus frequencies, it is critical to characterize and understand the trace impedance. Incorporating a test coupon design into the motherboard makes testing simpler and more accurate. The test coupon pattern must match the probe type being used.

The test coupon location is listed in order of preference, as follows:

- 1st choice (ideal location) = Memory section of the motherboard
- 2nd choice = Any section of the motherboard
- 3rd choice = Separate location in the panel

The *Intel Printed Circuit Board (PCB) Test Methodology Document (order 298179)* should be used to ensure boards are within the 28 Ω ± 10% requirement. The *Intel Controlled Impedance Design and Test Document* should be used for the test coupon design and implementation. These documents can be found at: http://developer.intel.com/design/chipsets/memory/rdram.htm(Select "Application Notes".)

5.1.4. Recommended Stack-Up

Though numerous stack-up variations are possible, the following starting point is recommended:

W = 18 mils, H = 4.5 mils, T = 2.0, 1-ply 2116 prepreg

For other possibilities see the following table and the following figures:

Table 61. 28 Ω Stack-Up Examples

Sample	Zo	H	W	T	SM (max.)	Resin %
1	27.1	4.3	18.0	2.1	0.6	53.0
2	28.1	3.8	18.5	1.6	1.2	72.0
3	28.6	4.8	19.0	2.5	0.7	61.0

5.1.5. Inner-Layer Routing

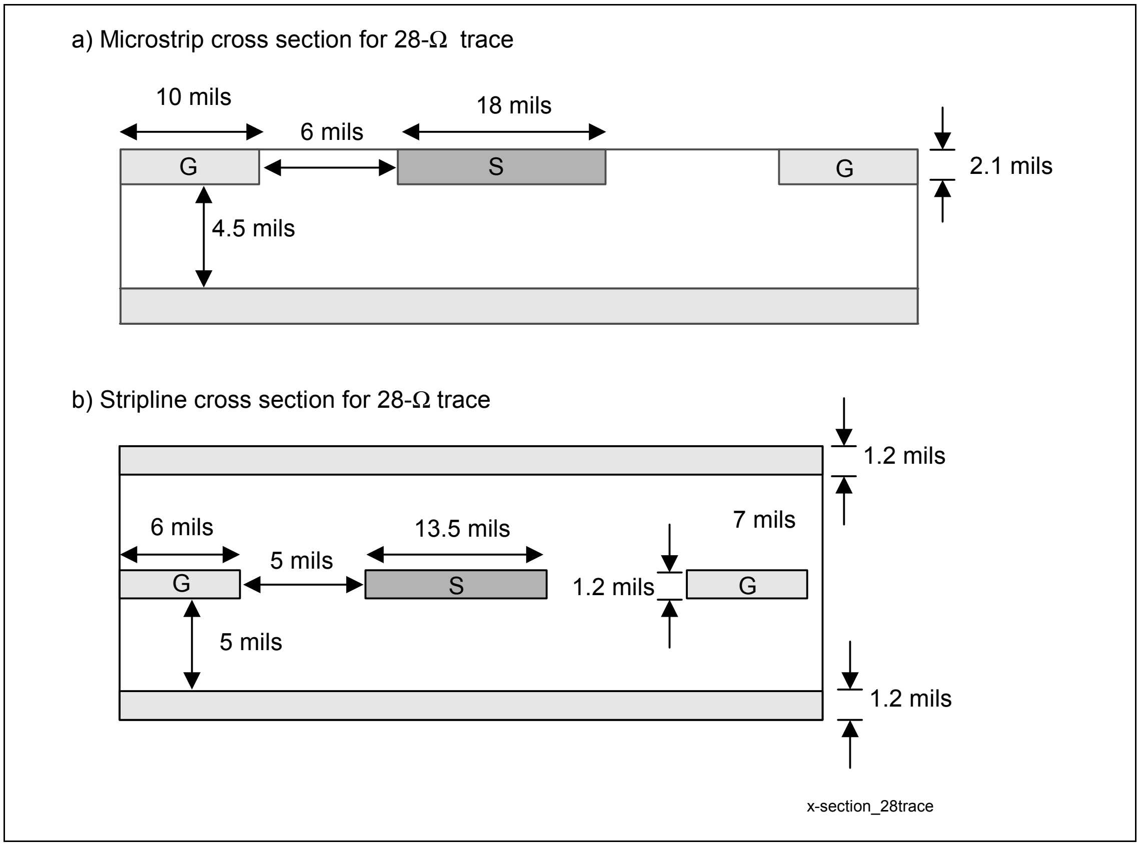
Inner-layer routing also has many possible stack-ups. For inner-layer routing, it is advisable to use the following starting point:

W = 13.5 mils, H1 = 7 mils, H2 = 5, T = 1.2

If these parameters are used, the initial TDR should fall within the acceptable limit, 28 Ω ± 10%.

Figure 98 shows examples of both stripline and microstrip cross sections.

Figure 98. Microstrip (a) and Stripline (b) Cross Section for 28 Ω Trace



Note: Do not forget ground floods and stitching.

5.1.6. Impedance Calculation Tools

3D field solvers, such as those by HP, Ansoft, Sonnet, and Polar, are most accurate when calculating the impedance. Z calculators based on equations (zcalc) also are fairly accurate. The differences are listed in the following table.

Table 62. 3D Field Solver vs. ZCALC

	#1	#2	#3	#4	#5	#6
H	4.5	4.5	4.2	4.8	4.5	4.5
W	18	18	18	18	17	19
W1	18.1	18.1	18.1	18.1	17.1	19.1
T	1.4	2.8	1.4	1.4	1.4	1.4
εr	4.5	4.5	4.5	4.5	4.5	4.5
Z0 (3D)	29.0	28.4	27.6	30.4	30.2	27.9
Z0 (zcalc)	29.1	28.7	27.7	30.4	30.2	28.0

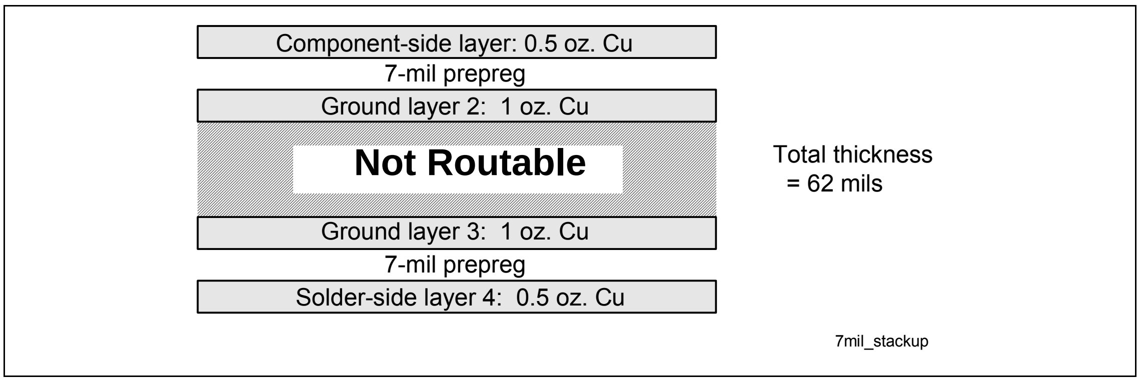
5.1.7. Testing Board Impedance

The *Intel Printed Circuit Board (PCB) Test Methodology document (order# 298179-001)* should be used to ensure boards are within the 28Ω +/- 10% requirement. This document can be found at http://developer.intel.com.

5.1.8. Board Impedance/Stack-up Summary

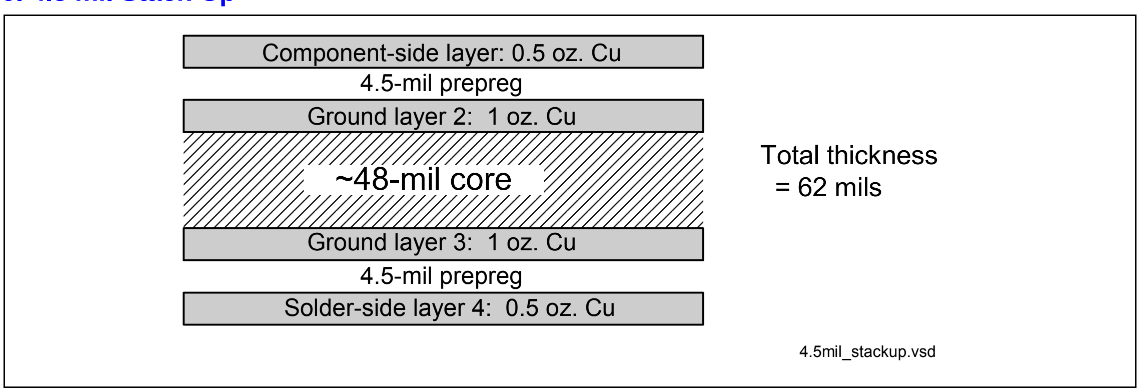
1. 7628 cloth (1-ply, 0.007 inch when cured with 40% resin) is the most popular and highest-volume in PCB production today. This stack-up will make routing impossible.
   - Fab construction (4 layers)
   - $Z_o = 70\ \Omega \pm 15\%$

Figure 99. 7 mil Stack-Up (Not Routable)



2. 2116 cloth (1-ply, 0.0045 inch when cured with 53% resin) is the second-highest-volume cloth in production today. Because of the impedance and layout requirements of traces for Direct RDRAM, AGP 2.0, and the hub interface, this stack-up is recommended for Intel 820E chipset platform design.
   - Fab construction (4 layers)
   - $Z_o = 60\ \Omega \pm 10\%$

Figure 100. 4.5 mil Stack-Up



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6. System Design Considerations

6.1. Power Delivery

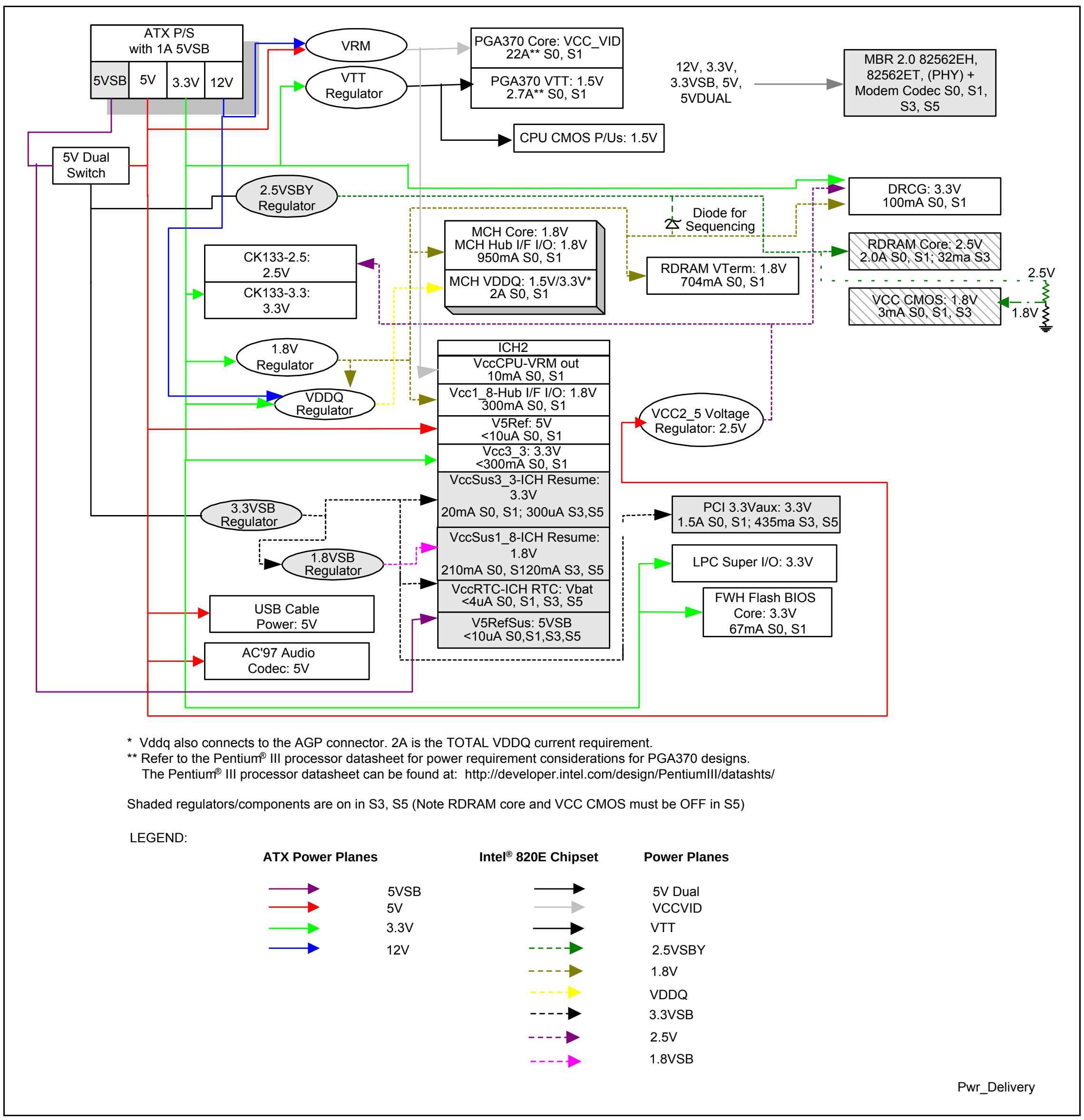
6.1.1. Terminology and Definitions

Term	Definition
Suspend to RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board to satisfy the S3 ACPI power management state.
Full-power operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state and the S1 (processor Stop Grant state) state.
Suspend operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend to RAM (S3) and Soft-Off (S5).
Power rails	An ATX power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, and 5 V_{SB}. In addition to these power rails, several other power rails are created with voltage regulators on the Intel 820E chipset reference board.
Core power rail	These power rails are on only during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The following core power rails are distributed directly from the ATX power supply: ±5 V, ±12 V, and +3.3 V.
Standby power rail	These power rails are on during the suspend operation. (These rails also are on during full-power operation.) These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is 5 V_{SB} (5 V standby). Other standby rails are created with voltage regulators on the motherboard.
Derived power rail	A derived power rail is any power rail generated from another power rail using an on-board voltage regulator. For example, 3.3 V_{SB} usually is derived (on the motherboard) from 5 V_{SB} using a voltage regulator. (On the Intel 820E chipset reference board, 3.3 V_{SB} is derived from 5V_DUAL.)
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during the suspend operation and is derived from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

6.1.2. Power Delivery of Intel® 820E Chipset Customer Reference Board

Figure 101 shows the power delivery architecture for the Intel 820E Chipset Reference Board. This power delivery architecture supports the Instantly Available PC Design Guidelines via the Suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include main memory, the ICH2 resume well, PCI wake devices (via 3.3 V_{AUX}), and USB. (USB can be powered only if sufficient standby power is available.) To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device's power requirements, both in the suspend and full-power states. The power requirements must be compared with the power budget available from the power supply. Due to the requirements of main memory and PCI 3.3 V_{AUX}—and possibly other devices in the system—it is necessary to create a dual power rail.

Figure 101. Intel® 820E Chipset Power Delivery Example



This design guide provides only examples. Many power distribution methods achieve similar results. When deviating from these examples in any way, it is critical to consider the effects of the change.

In addition to the power planes provided by the ATX power supply, an instantly available Intel 820E chipset-based system (using Suspend to RAM) requires that seven power planes be generated on the board. The requirements for each power plane are documented in this section. In addition to on-board voltage regulators, the Intel 820E chipset reference board has a 5 V dual switch.

5 V Dual Switch

This switch powers the 5 V dual plane from the 5 V core ATX supply during full-power operation. During Suspend to RAM, the 5 V dual plane will be powered from the 5 V standby power supply. Note: The voltage on the 5 V dual plane is not 5 V! The resistive drop through the 5 V dual switch must be considered. Therefore, no components should be connected directly to the 5 V dual plane. On the ICH2 reference board, only the voltage regulators (for lower-voltage regulation) are connected to the 5 V dual plane.

Note: This switch is not required in an Intel 820E chipset-based system that does not support Suspend to RAM (STR).

VCCVID

This power plane is used to power the Intel PGA370 socket processor.

Refer to the latest revisions of the following documents:

- *VRM 8.4 DC-DC Converter Design Guidelines*
- For the Intel 820E chipset/FC-PGA Vcc_vid requirements, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at: http://developer.intel.com/design/chipsets/designex/298178.htm

Note: This regulator is required in *all* designs.

VTT

This power plane is used to power the AGTL+ dual-ended termination and the 1.5 V power delivery to the Intel PGA370 socket processor.

Refer to the latest revision of the following document:

- For the Intel 820E chipset/FC-PGA VTT requirements, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at:

  http://developer.intel.com/design/chipsets/designex/298178.htm

Note: This regulator is required in *all* designs.

VCC 2.5

The Pentium III processor for the Intel PGA370 socket does not use this signal.

2.5 VBSY

The 2.5 V_{SBY} power plane is used to power the RDRAM core and the VCMOS rail on the RDRAMs. The RDRAM core requires an approximately 4.5-A *maximum average DC current* at 2.5 V. In the Intel 820E chipset reference board, the *2.5 V_{SBY}* plane is derived from the *5 V dual* power plane using a switching regulator. During the maximum load-step of 2 A, the maximum voltage fluctuation must be less than 50 mV. The maximum tolerance for 2.5 V is 125 mV. However, during any 10 µs period, the voltage cannot fluctuate more than 50 mV. The high-frequency bypassing requirements are satisfied using capacitors on the RIMM itself. Low-frequency bypass requirements vary depending on the voltage regulator used. By using a switching regulator with a relatively slow response time, the low-frequency bypass recommendation is eight 100 µF bulk capacitors (0.1-Ω ESR) near the RIMM connectors. By using a linear regulator with a substantially faster response time, the low-frequency bypass requirement could be reduced.

The *VCMOS* rail requires a maximum of 3 mA at 1.8 V. This rail *must* be powered during *Suspend to RAM*. Therefore, the *VCMOS* rail cannot be connected to the MCH core power. Because the current requirements of *VCMOS* are so low, a resistor divider can be used to generate *VCMOS* from *2.5 V_{SBY}*. The resistor divider should be 36 Ω (top) / 100 Ω (bottom). Additionally, it should be bypassed with a 0.1-µF chip capacitor.

The Intel reference board uses a switching regulator from *5 V dual*. It may be possible to use a linear regulator to regulate from 3.3 V_{SB}. However, the thermal characteristics must be considered. Additionally, a *low-dropout* linear regulator would be necessary. If 2.5 *V_{SBY}* is regulated from 3.3 V_{SB}, the 3.3 V_{SB} regulator must be able to supply enough current for all the 3.3 V_{SB} device requirements *as well as* the 2.5 V_{SBY} requirements.

Refer to the 1.8 V power plane information for 1.8 V and 2.5 V power sequencing requirements.

Note: This regulator is required in *all* designs. However, in systems that do not support STR, the 2.5 V rail is powered from either the 3.3 V or 5 V core well.

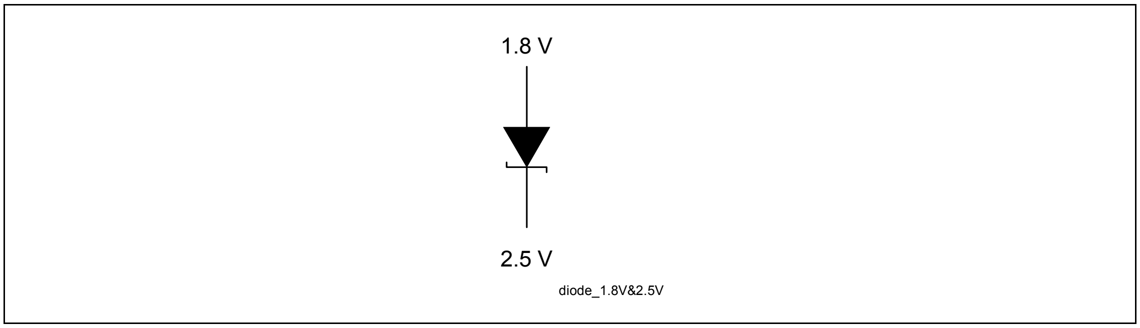
1.8 V

The 1.8 V plane powers the MCH core, the ICH2 hub interface's I/O buffers, and the RDRAM termination resistors. This power plane has a total power requirement of approximately 1.7 A. The 1.8 V plane should be decoupled with a 0.1 µF and 0.01 µF chip capacitor at *each* corner of the MCH and with a single 1 µF and 0.1 µF capacitor at the ICH2.

Note: This regulator is required in *all* designs.

Power *must not* be applied to the RDRAM termination resistors (V_{TERM}) before applying power to the RDRAM core (2.5 V_{SBY} in this design). This can be guaranteed by placing a Schottky diode between 1.8 V and 2.5 V, as shown in the Figure 102:

Figure 102. 1.8 V and 2.5 V Power Sequencing (Schottky Diode)



V_{DDQ}

The V_{DDQ} plane is used to power the MCH AGP interface and the graphics component AGP interface. Refer to the *AGP Interface Specification*, Revision 2.0 (http://www.agpforum.org).

For long-term component reliability, the following power sequence is strongly recommended while the AGP interface of the MCH is running at 3.3 V. If the AGP interface is running at 1.5 V, the following power sequence recommendations no longer apply. The power sequence recommendations are as follows:

1. During the power-up sequence, the 1.8 V must ramp up to 1.0 V *before* the 3.3 V ramps up to 2.2 V.
2. During the power-down sequence, the 1.8 V *cannot* ramp below 1.0 V *before* the 3.3 V ramps below 2.2 V.
3. The same power sequence recommendation applies when entering and exiting the S3 state, because MCH power is completely off during the S3 state.

System designers must keep this requirement in mind while designing the voltage regulators and selecting the power supply. For further details regarding the voltage sequencing requirements, refer to the latest revision of the *Intel® 820 Chipset: Intel® 82820 Memory Controller Hub (MCH) Datasheet* (http://developer.intel.com/design/chipsets/datashts/290630.htm?iid=PCG+820blue&).

Note: This regulator is required in *all* designs (unless the design does not support 1.5 V AGP, and therefore does not support 4× AGP).

3.3VSB

The 3.3 V_{SB} plane powers the I/O buffers in the resume well of the ICH2 and the PCI 3.3 V_{AUX} suspend power pins. The 3.3 V_{AUX} requirement states that during suspend, the system must deliver 375 mA to each *wake-enabled* card and 20 mA to each *non-wake-enabled* card. During *full-power* operation, the system must be able to supply 375 mA to *each* card. Therefore, the total current requirement is as follows:

- *Full-power operation*: 375 mA × number of PCI slots
- *Suspend operation*: (375 + 20) × (number of PCI slots – 1)

In addition to the PCI 3.3 V_{AUX}, the ICH2 suspend well power requirements must be considered, as shown in **Error! Reference source not found.**.

Note: This regulator is required in *all* designs.

1.8 VSB

The 1.8 V_{SB} plane powers the logic to the resume well of the ICH2. This should not be used for VCMOS. The VCMOS described in the 2.5 V_{SBY} section should be powered down in S5. However, the 1.8 V_{SB} requires power in S5. Refer to the 2.5 V_{SBY} section for information regarding powering the VCMOS (1.8 V) rail.

2.5 V

The 2.5 V plane supplies power to the CK133 and the DRCG system clock generator components.

6.1.3. ICH2 1.8 V / 3.3 V Power Sequencing

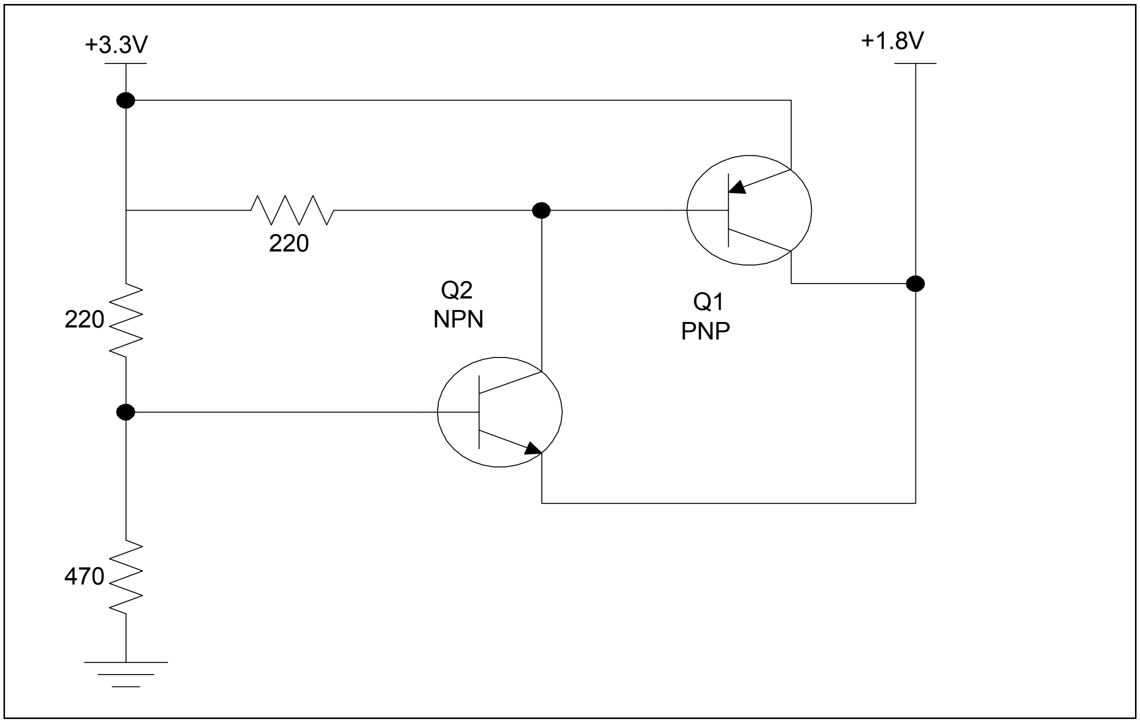
The ICH2 has two pairs of associated 1.8 V and 3.3 V supplies. These are (Vcc1_8, Vcc3_3) and ({VccSus1_8, VccSus3_3). The ICH2-m has a third pair (VccLAN1_8, VccLAN3_3). These pairs are assumed to power up and power down together. *The difference between the two associated supplies must never be greater than 2.0 V.* The 1.8 V supply may come up before the 3.3 V supply without violating this rule. (Although this generally is not practical in a desktop environment, since the 1.8 V supply is typically derived from the 3.3 V supply by means of a linear regulator.)

One serious consequence of violating this “2 V Rule” is electrical overstress of oxide layers, resulting in component damage.

Most ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic powered by the 1.8 V supplies. Thus, another consequence of faulty power sequencing arises if the 3.3 V supply comes up first. In this case the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals defined as “input-only” actually have output buffers that are disabled normally, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

Figure 103 is an example power-on sequencing circuit that ensures the 2 V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

Figure 103. Example 1.8V/3.3V Power Sequencing Circuit



When analyzing systems that may be "marginally compliant" with the 2 V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK (also LAN_PWROK in ICH2-m) signals, since these signals control the internal isolation logic between the various power planes, as follows:

- RSMRST# controls the isolation between the RTC well and the resume wells.
- PWROK controls the isolation between the resume wells and main wells.
- LAN_PWROK controls the isolation between the LAN wells and the resume wells (applies only to ICH2-m).

If one of these signals goes high while one of its associated power planes is active and the other is not, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging, internal currents.

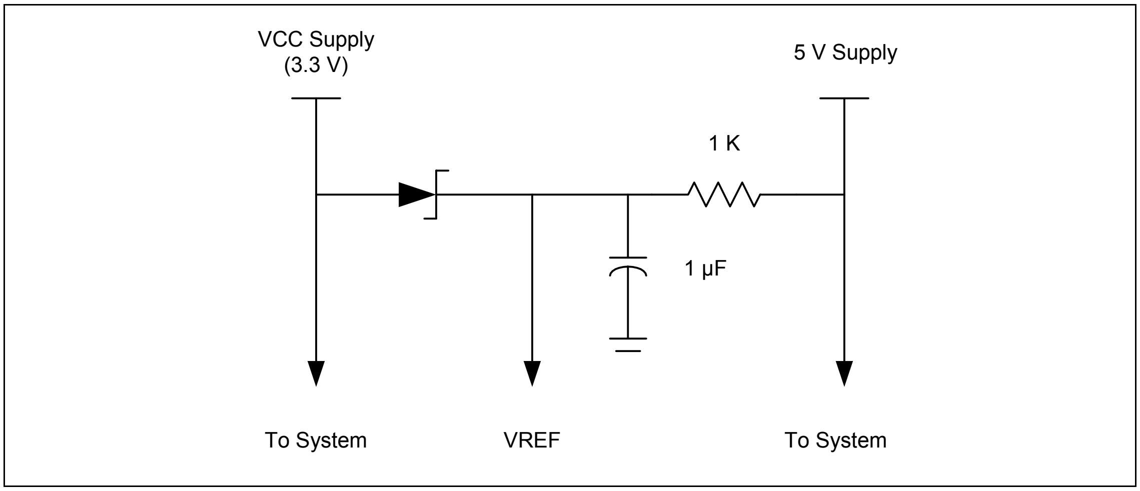
6.1.4. 3.3V/V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before or simultaneously to Vcc3_3. It must also power down after or simultaneous to Vcc3_3. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 104 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USBOC. If these signals are not needed during suspend, V5REF_Sus can be hooked to the VccSus3_3 rail.

Figure 104. Example 3.3V/5V REF Sequencing Circuitry



6.1.5. Excessive Power Consumption by 64/72-Mbit RDRAM

Some 64/72-Mbit RDRAM devices interpret non-broadcast, device-directed commands as broadcast commands. These commands are the SET_FAST_CLOCK, SET_RESET, and CLEAR_RESET commands. RDRAM devices consume more current during these initialization steps than during normal operation. If these devices accept device-directed commands as broadcast commands, the device cannot be reset/initialized serially. All devices must be reset/initialize simultaneously. This will result in excessive current draw during the initialization of memory. The amount of excessive current will depend on the number of devices and the frequency used. The worst-case current draw is 7.5 A, in a system with 32 devices and a frequency of 400 MHz. There are two potential solutions:

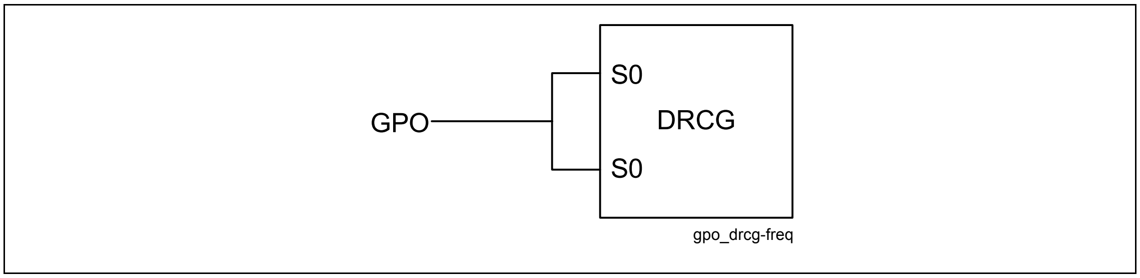
1. Reduce the clock frequency during initialization (Section 6.1.5.1).
2. Increase the current capability of the 2.5 V voltage regulator (Section 6.1.5.2).

6.1.5.1. Option 1: Reduce the Clock Frequency During Initialization

Tie a single core well GPO with a default high state to both the S0 and S1 pins of the DRCG (i.e., tie S0 and S1 together and then connect to a GPO as shown in Figure 105). When the core power supply to the system is turned on, the DRCG enters a test mode and the output frequency will match the input REFCLK frequency. For details regarding this DRCG mode, refer to the latest DRCG specification. When the DRCG output clock is slowed down, the power consumed by the 2.5 V power supply is reduced. After the SetR/ClrR commands have been issued, the BIOS drives the GPO low to bring the DRCG back to normal operation.

Note: If a default-low GPO is used, during power-up all devices may come up in the standby state at full speed; this requires more power.

Figure 105. Use a GPO to Reduce DRCG Frequency



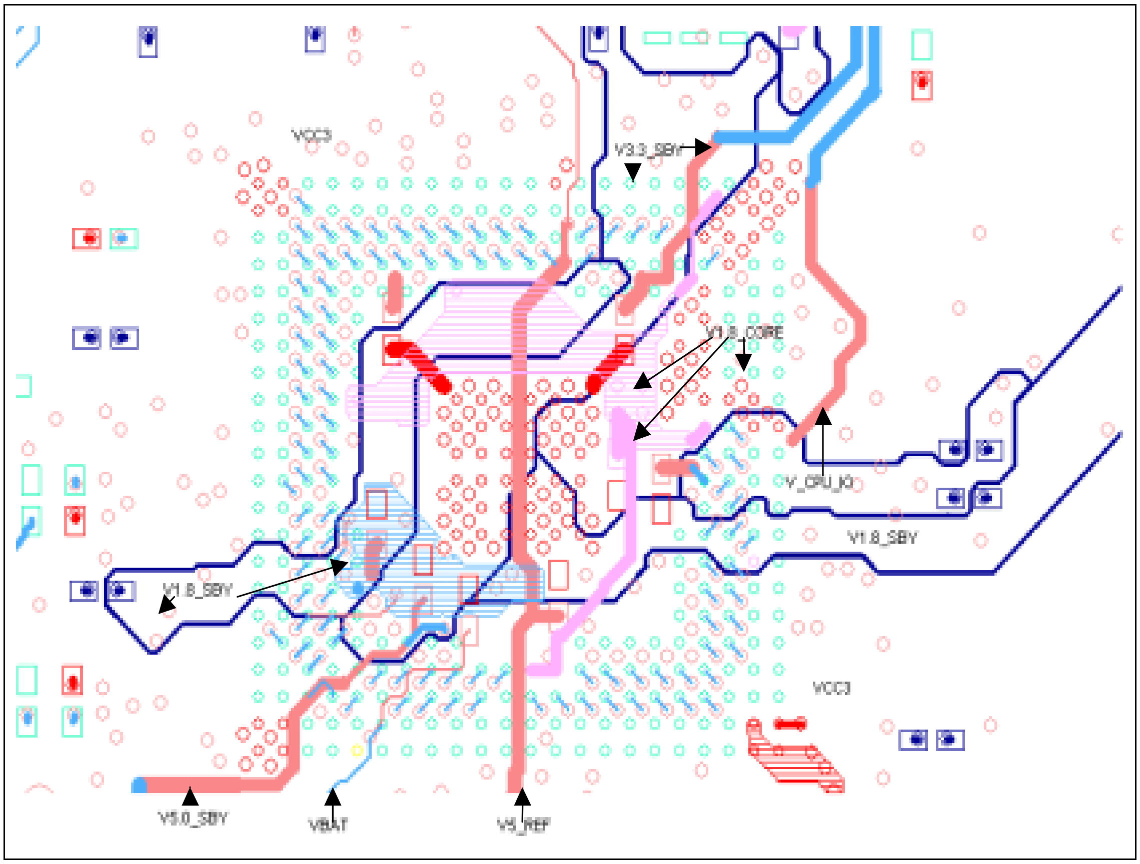
6.1.5.2. Option 2: Increase the Current Capability of the 2.5 V Voltage Regulator

The second implementation option requires that the 2.5 V power supply be modified to maintain the maximum amount of current required by a fully populated RDRAM channel (~7.5 A).

6.2. ICH2 Power Plane Split

The following *example* shows the power plane splits for the ICH2.

Figure 106. Example of ICH2 Power Plane Split



6.3. Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations of both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus. For thermal design considerations regarding the Pentium III processor using the Intel PGA370 socket, refer to the *Intel® 820 Chipset Design Guide Addendum for the Intel® Pentium® III Processor for the PGA370 Socket*. These guidelines can be downloaded from the Intel website at: http://developer.intel.com/design/chipsets/designex/298178.htm

The thermal design power numbers for the MCH and the ICH2 are listed in the following table.

Table 63. Intel® 820E Chipset Component Thermal Design Power

Component	Thermal Design Power (133/400 MHz)
MCH	3.5 W ± 15%
ICH2	1.5 W ± 15%

6.4. Glue Chip 3 (Intel® 820E Chipset Glue Chip)

To reduce the component count and BOM cost of the Intel 820E chipset platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, the overall board cost can be reduced.

Features

- PWROK signal generation
- Control circuitry for Suspend to RAM
- Power supply power-up circuitry
- RSMRST# generation
- Back-feed cutoff circuit for Suspend to RAM
- 5 V reference generation
- Flash FLUSH# / INIT# circuit
- HD single-color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for audio MIDI signal
- Audio disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from the vendors listed in the following table.

Table 64. Glue Chip Vendors

Vendor Intel	Contact	Contact Information
Fujitsu Microelectronics	Customer Response Center	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 Phone: 1-800-866-8600 Fax: 1-408-922-9179 E-mail: fmicrc@fmi.fujitsu.com
Mitel Semiconductor	Mitel Semiconductor	1735 Technology Drive Suite 240, San Jose, CA 95110 Phone: 408-451-4723 Fax: 408-451-4710 URL: http://www.mitelsemi.com

Appendix A: Reference Design Schematics (Uniprocessor)

This chapter provides the schematic diagrams for the Reference Board Uniprocessor design.

Reference Design Feature Set

- Intel 820E chipset
  - Memory controller hub (MCH)
  - I/O controller hub (ICH2)
  - FWH Flash BIOS
- Support for Coppermine FC-PGA processors
  - 100 MHz and 133 MHz system bus frequency
  - Debug port
- IOAPIC integrated into ICH2
- Direct RDRAM memory interface
  - 300 MHz, 356 MHz, and 400 MHz Direct RDRAM support
  - 2 RIMM sockets
- 5 PCI add-in slots
  - Via 5 REQ/GNT pairs (ICH2 supports 6 REQ#/GNT# pairs.)
  - Added 4 PCI interrupts (total of 8)
- AGP universal connector
  - 3.3 V: 1×, 2× signaling
  - 1.5 V: 1×, 2×, 4× signaling
- 2 IDE connectors with Ultra ATA/100/66/33, BMIDE, PIO support
- ICH2 2 USB controllers (total of 4 ports)
- ATX power connector
- LPC Ultra I/O
  - Floppy disk controller
  - 1 parallel port, 1 serial port
  - Keyboard controller
- Communications networking riser (CNR)
  - Support for up to 6-channel audio
- WfM support
- Integrated system management
  - SMBus slave interface access via SMLink
- Integrated power management
  - ACPI Rev. 1.0 compliant
  - APM Rev. 1.2 compliant
- Integrated LAN controller
- VRM 8.4-compliant voltage regulator
- Four-layer design

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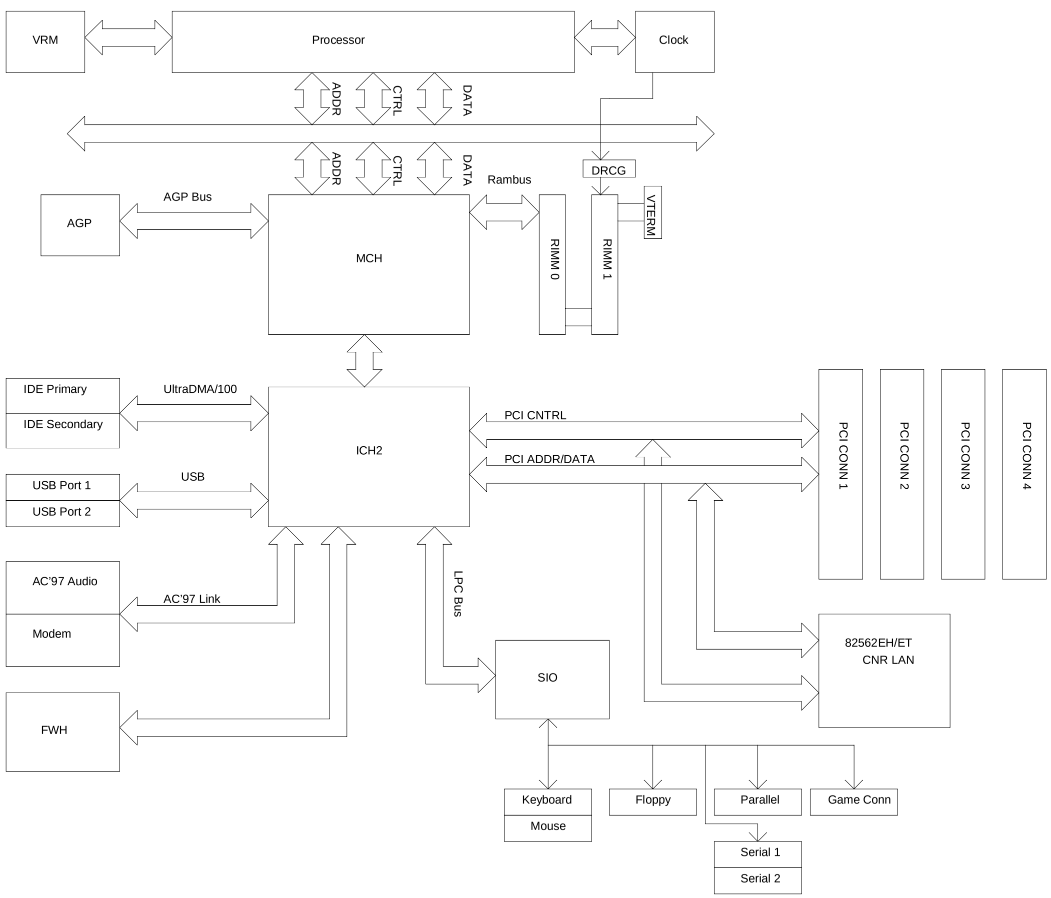
INTEL(R) 820E CHIPSET
FCPGA 2 RIMM ICH2 REFERENCE SCHEMATICS
REVISION 0.5

Note that these schematics are preliminary and are subject to change.

TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 5-23-2000_9:18	SHEET: 1 OF 40

Block Diagram



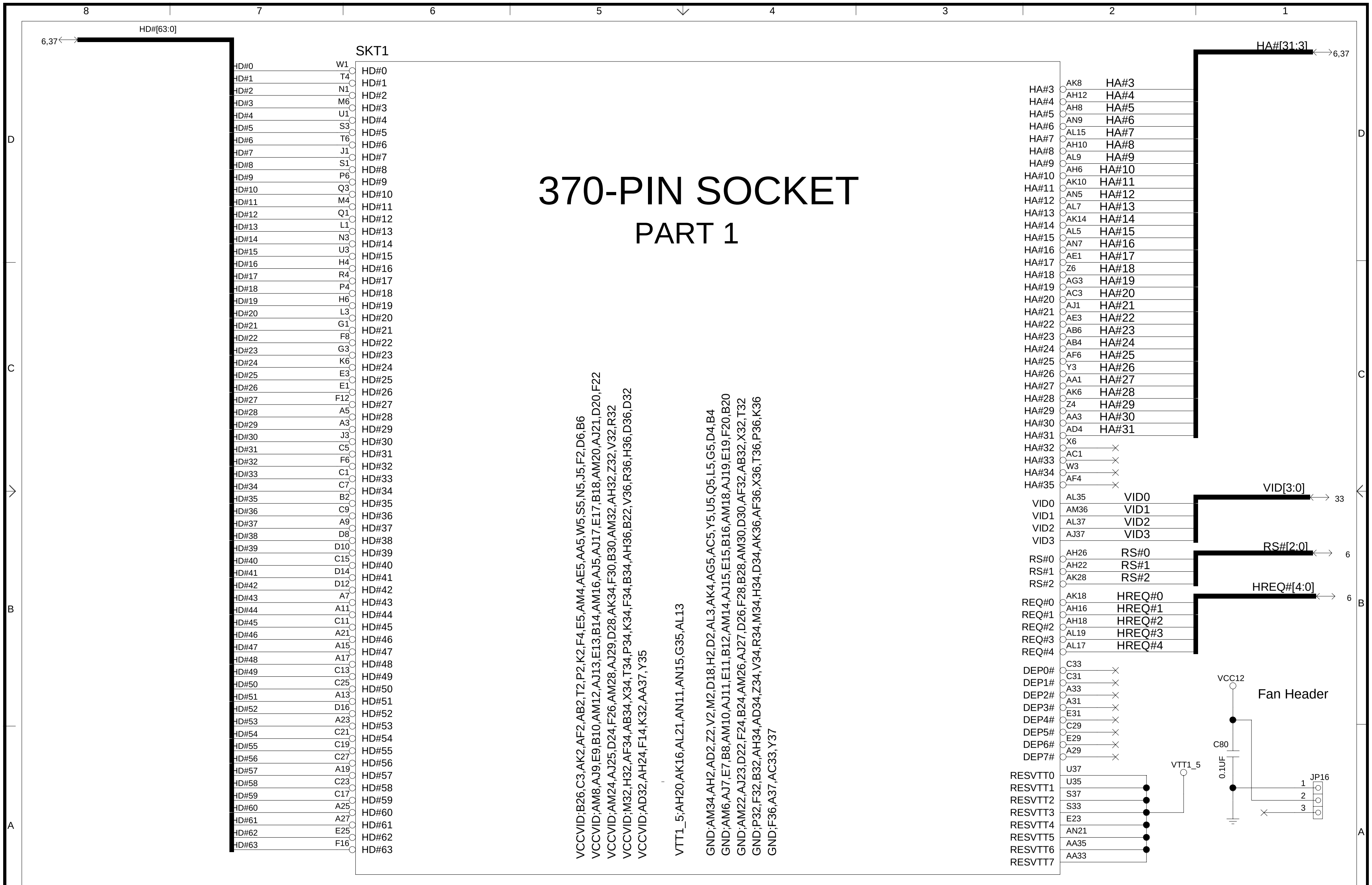
Device Table

REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U1	LM4880		14
U2	AD1881		13
U3	74LVC08A	A, B	36
U4, U6	GD75232		30
U8	82562		17
U10	82820 (MCH)		6, 7
U11	CK133		5
U12	DRCG		5
U13	82820 (ICH)		8, 9
U14	74LVC07A	A, B, C, D, E	7, 23, 34, 35
U15	74LVC14a	A, B, C, D, E	36
U16	FWH		10
U17	LPC47B27X		12
U18	74LS132	B, C	34, 36
U19	74LVC07A	A, C, D	23, 27
U20	74LVC06A	A, B, C	36
U21	74HC03		15
U25	82562EM		18
U26	FFB3904		23
U27	H1138_Argonite		20
U28	A03449-001		19

TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
BLOCK DIAGRAM
REV: 0.5

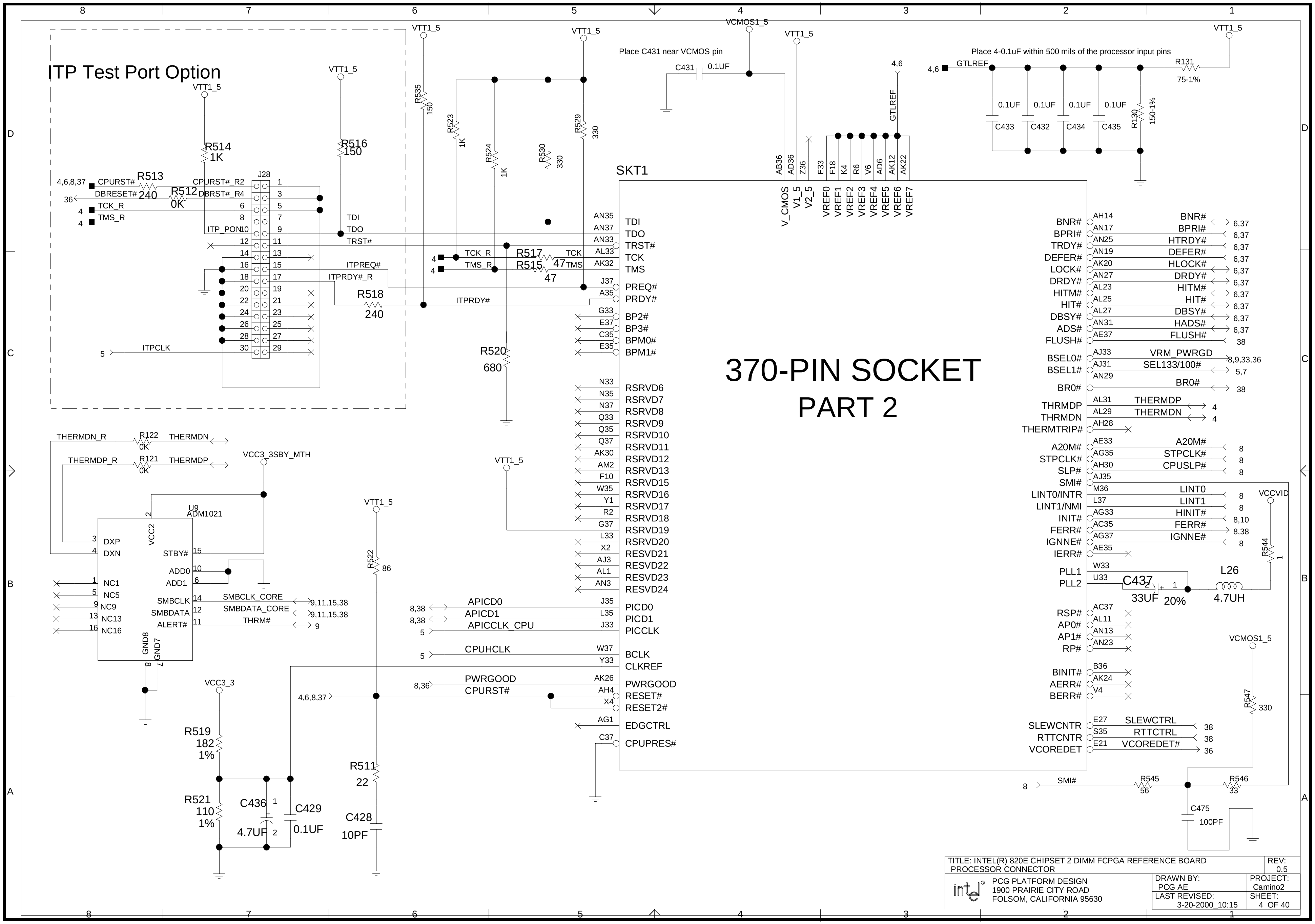
intel®
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY: PCG AE
PROJECT: Camino2
LAST REVISED: 5-23-2000_9:18
SHEET: 2 OF 40

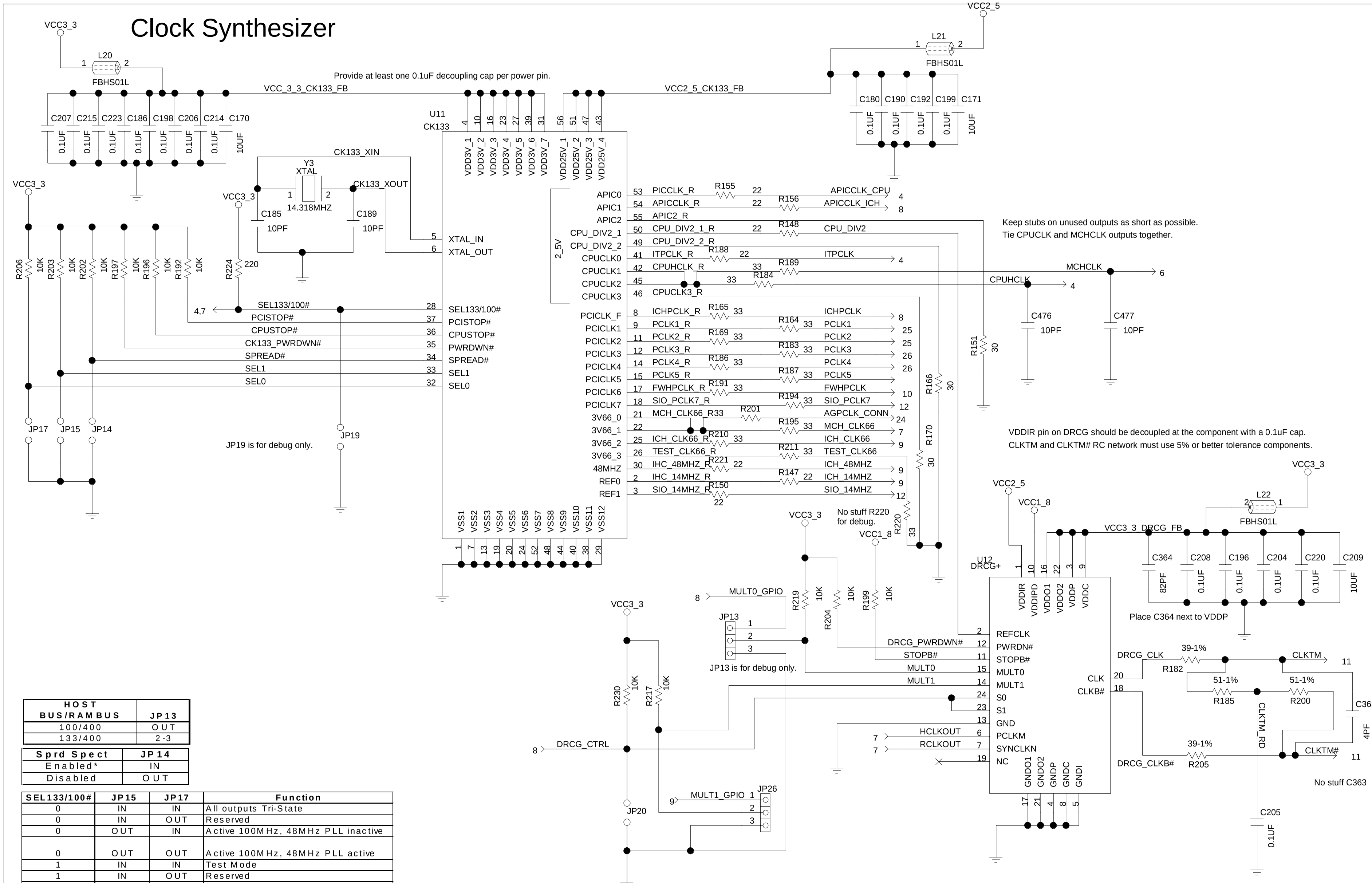


TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
PROCESSOR CONNECTOR

intel® PCG PLATFORM DESIGN, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 3 OF 40
		REV: 0.5


370-PIN SOCKET
PART 2
SKT1
ITP Test Port Option
Place C431 near VCMOS pin
Place 4-0.1uF within 500 mils of the processor input pins
U9
ADM1021
J28
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
PROCESSOR CONNECTOR
REV:
0.5
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PCG AE
PROJECT:
Camino2
LAST REVISED:
3-20-2000_10:15
SHEET:
4 OF 40

Clock Synthesizer



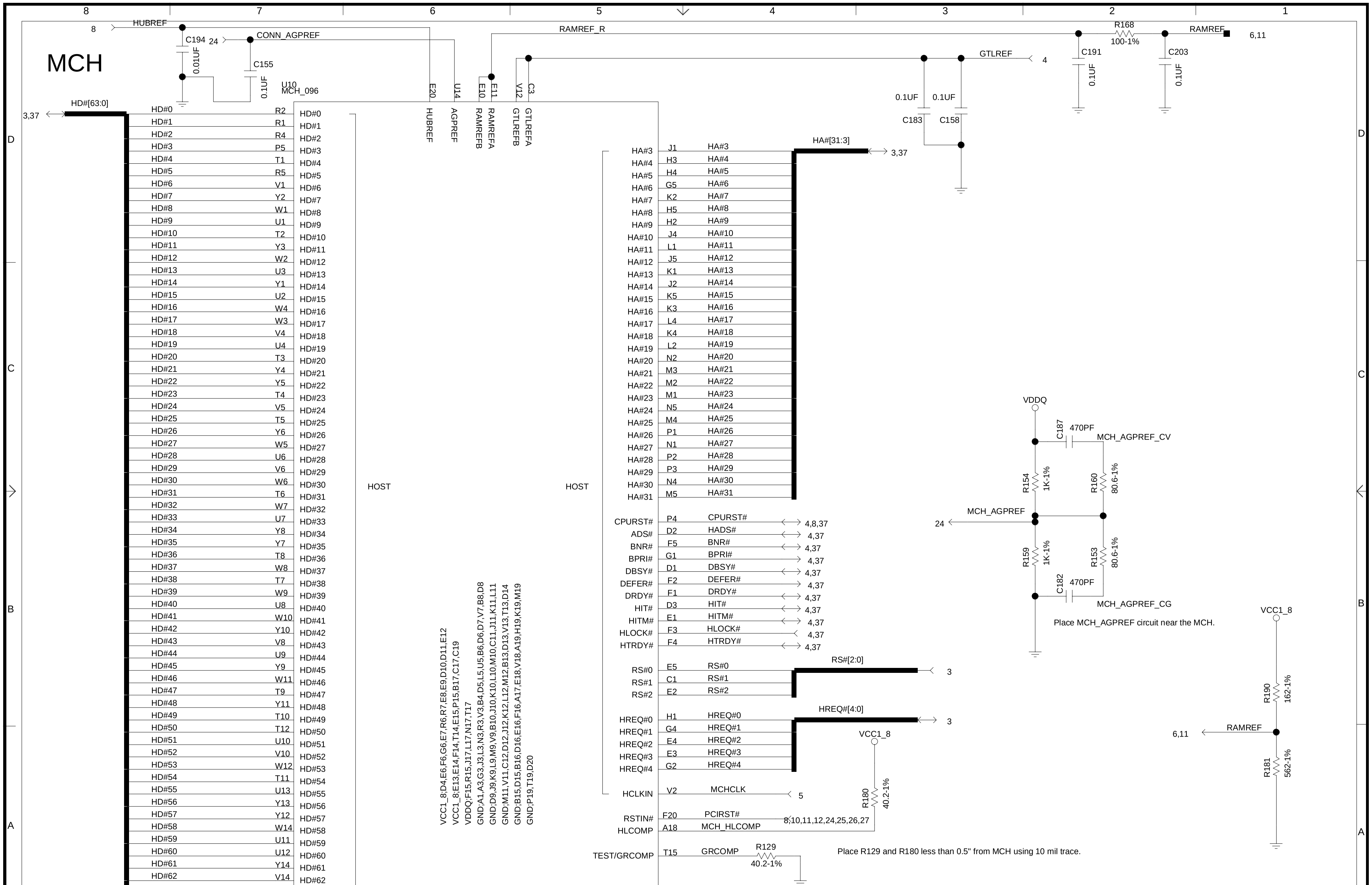
HOST BUS/RAMBUS	JP13
100/400	OUT
133/400	2-3

Sprd Spect	JP14
Enabled*	IN
Disabled	OUT

SEL133/100#	JP15	JP17	Function
0	IN	IN	All outputs Tri-State
0	IN	OUT	Reserved
0	OUT	IN	Active 100MHz, 48MHz PLL inactive
0	OUT	OUT	Active 100MHz, 48MHz PLL active
1	IN	IN	Test Mode
1	IN	OUT	Reserved
1	OUT	IN	Active 133MHz,48MHz PLL inactive
1	OUT	OUT	Active 133MHz,48MHz PLL active*

All jumpers may not be required, but are included for test purposes.

TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD CLOCK SYNTHESIZER		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_14:02	SHEET: 5 OF 40



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
MCH

REV: 0.5

PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

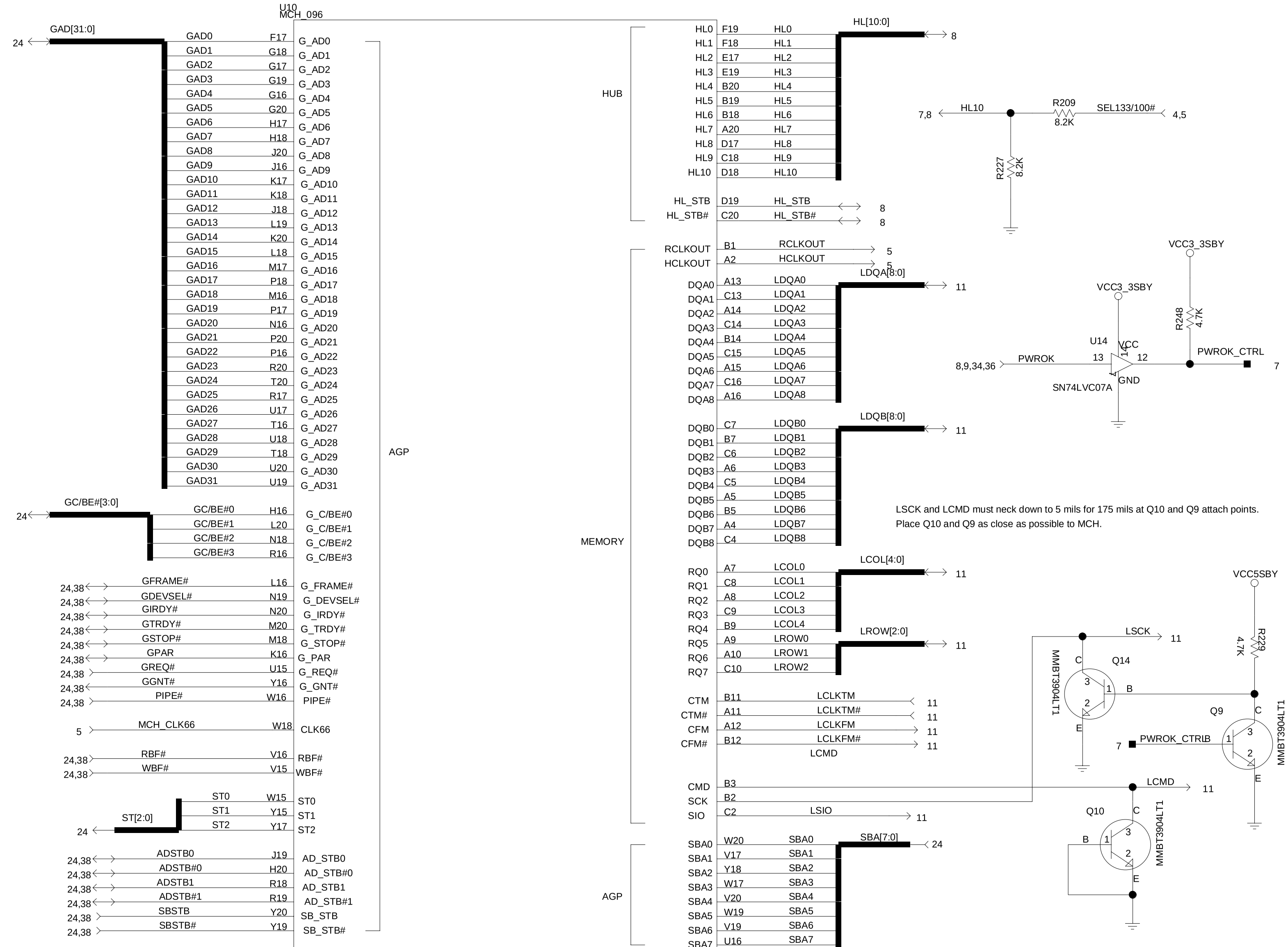
DRAWN BY: PCG AE

PROJECT: Camino2

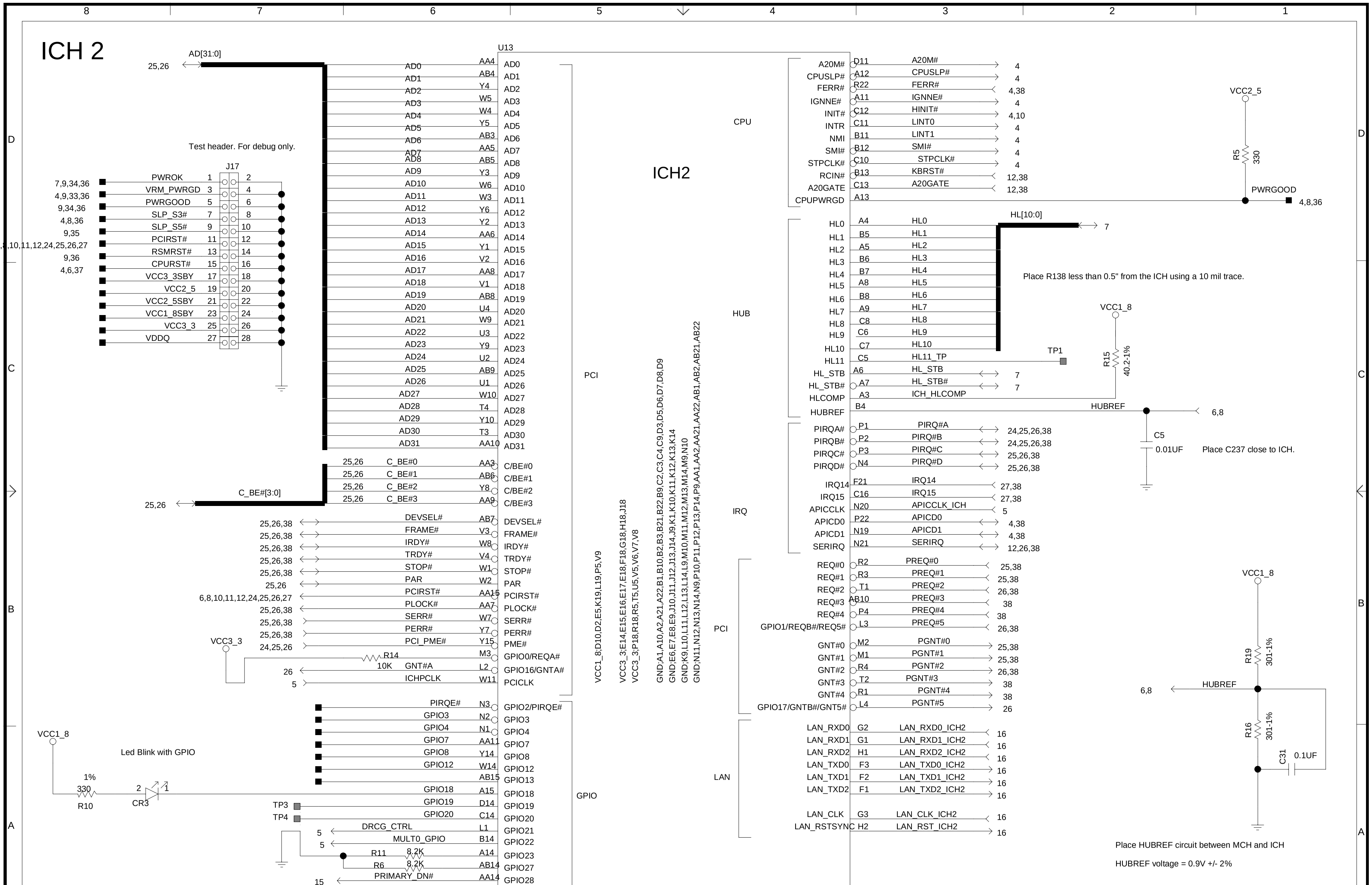
LAST REVISED: 3-20-2000_14:02

SHEET: 6 OF 40

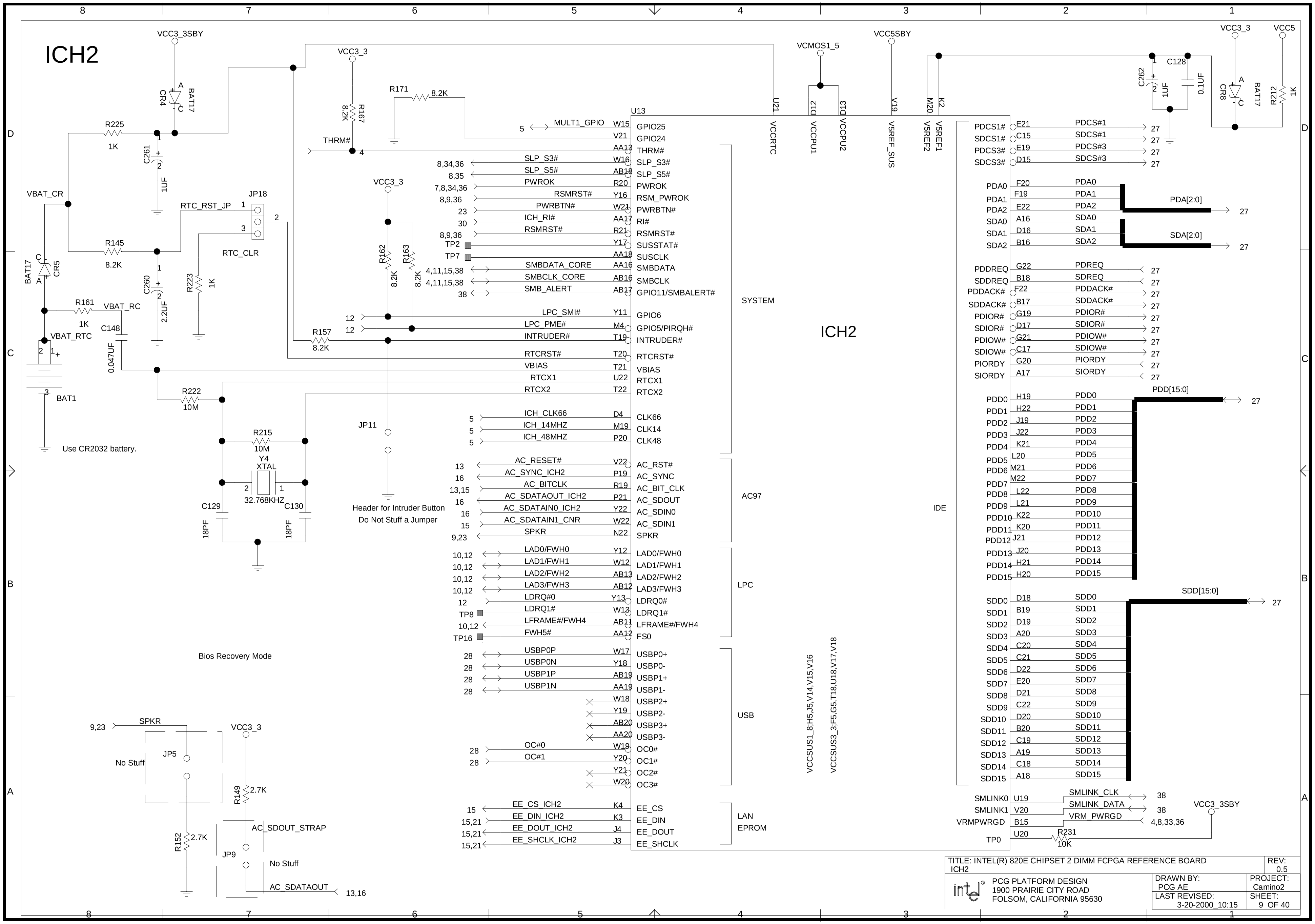
MCH



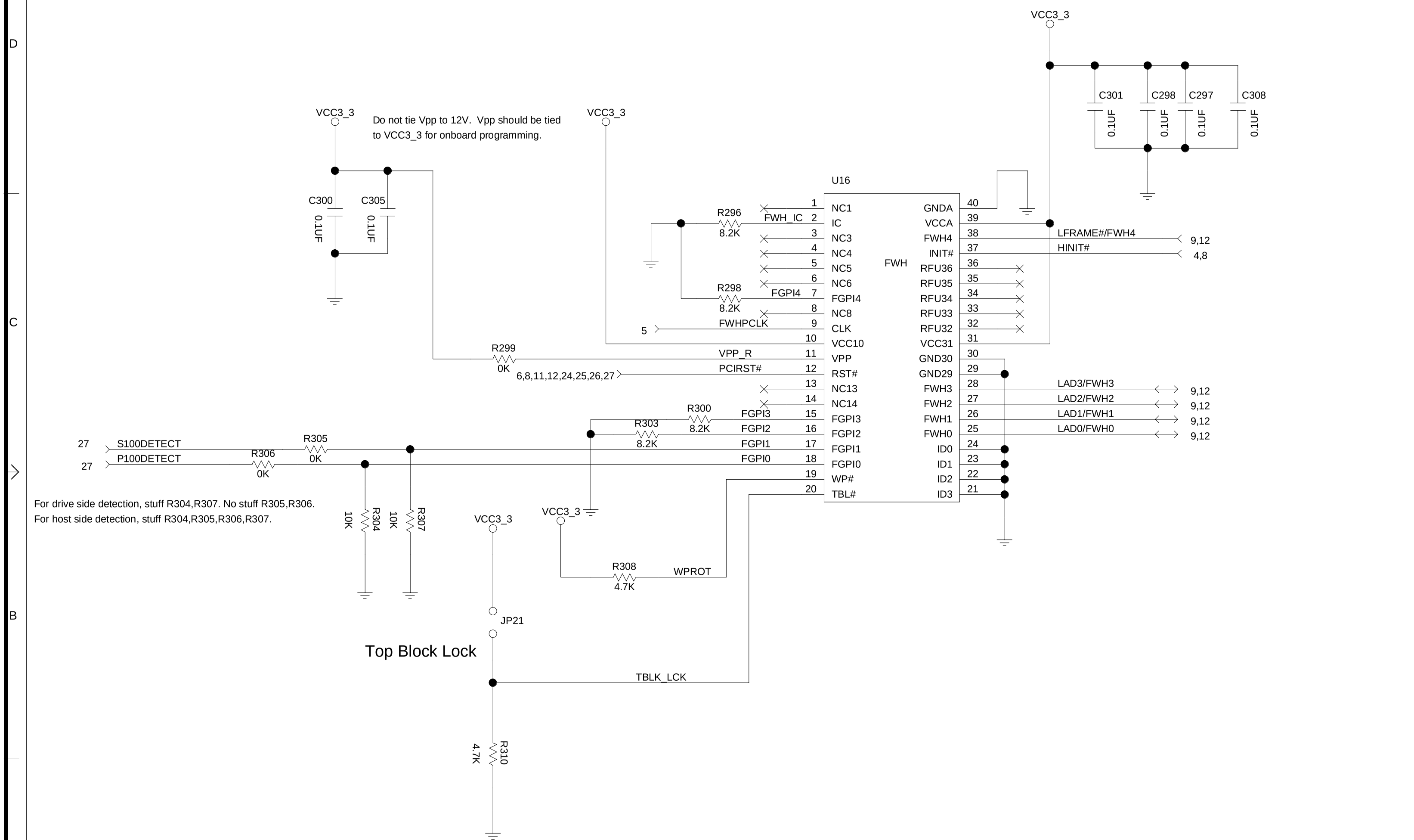
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD MCH		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_14:02	SHEET: 7 OF 40



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD ICH2		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_14:02	SHEET: 8 OF 40


ICH2
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
ICH2
REV:
0.5
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PCG AE
PROJECT:
Camino2
LAST REVISED:
3-20-2000_10:15
SHEET:
9 OF 40
U13
ICH2
SYSTEM
AC97
LPC
USB
LAN
EPROM
IDE
VCCSUS1_8;H5,J5,V14,V15,V16
VCCSUS3_3;F5,G5,T18,U18,V17,V18
Use CR2032 battery.
Header for Intruder Button
Do Not Stuff a Jumper
Bios Recovery Mode
No Stuff
VCC3_3SBY
VCC3_3
VCC5
VCC5SBY
VCMOS1_5
VCCRTC
VCCPU1
VCCPU2
V5REF_SUS
V5REF1
V5REF2
VBAT_CR
VBAT_RC
VBAT_RTC
RTC_RST_JP
RTC_CLR
JP18
JP11
JP5
JP9
BAT1
BAT17
32.768KHZ
XTAL
MULT1_GPIO
THRM#
SLP_S3#
SLP_S5#
PWROK
RSMRST#
PWRBTN#
ICH_RI#
SMBDATA_CORE
SMBCLK_CORE
SMB_ALERT
LPC_SMI#
LPC_PME#
INTRUDER#
RTCRST#
VBIAS
RTCX1
RTCX2
ICH_CLK66
ICH_14MHZ
ICH_48MHZ
AC_RESET#
AC_SYNC_ICH2
AC_BITCLK
AC_SDATAOUT_ICH2
AC_SDATAIN0_ICH2
AC_SDATAIN1_CNR
SPKR
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LDRQ#0
LDRQ1#
LFRAME#/FWH4
FWH5#
USBP0P
USBP0N
USBP1P
USBP1N
OC#0
OC#1
EE_CS_ICH2
EE_DIN_ICH2
EE_DOUT_ICH2
EE_SHCLK_ICH2
AC_SDOUT_STRAP
AC_SDATAOUT
PDA[2:0]
SDA[2:0]
PDD[15:0]
SDD[15:0]
SMLINK_CLK
SMLINK_DATA
VRM_PWRGD

FWH



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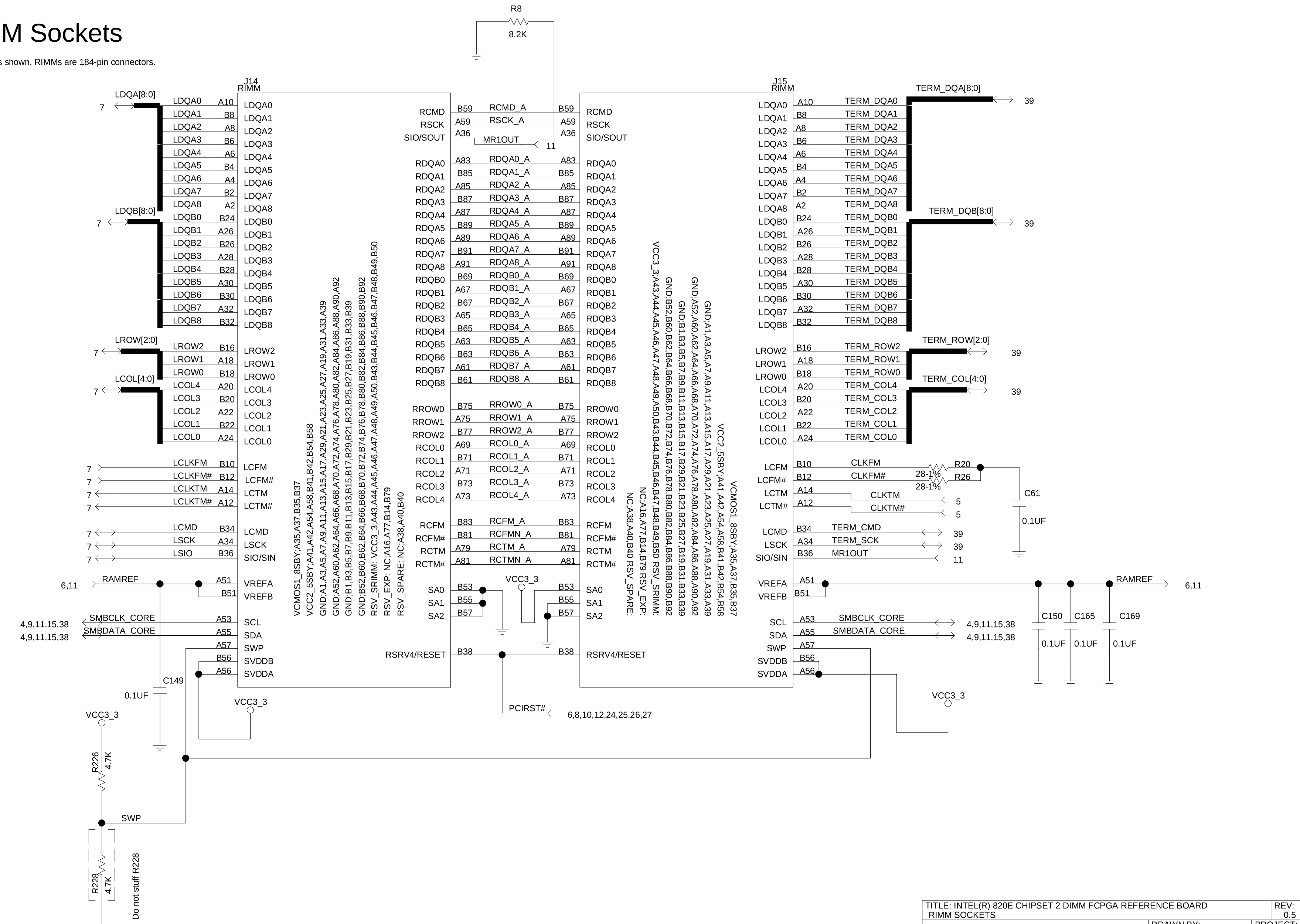
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 10 OF 40

RIMM Sockets

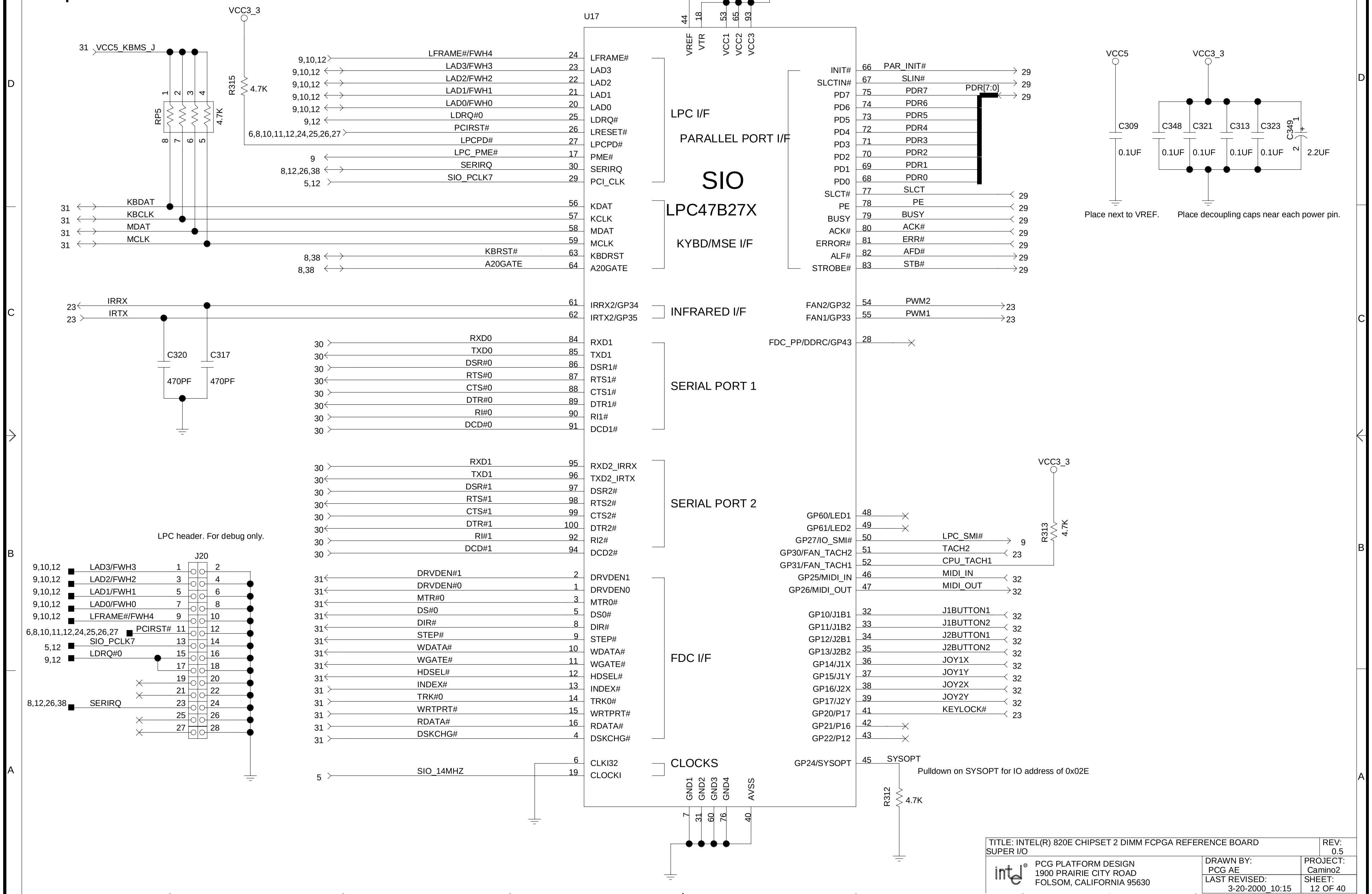
As shown, RIMMs are 184-pin connectors.



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
RIMM SOCKETS

intel® PCG PLATFORM DESIGN, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:29	SHEET: 11 OF 40
		REV: 0.5

Super I/O



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
SUPER I/O

REV: 0.5

intel®

PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

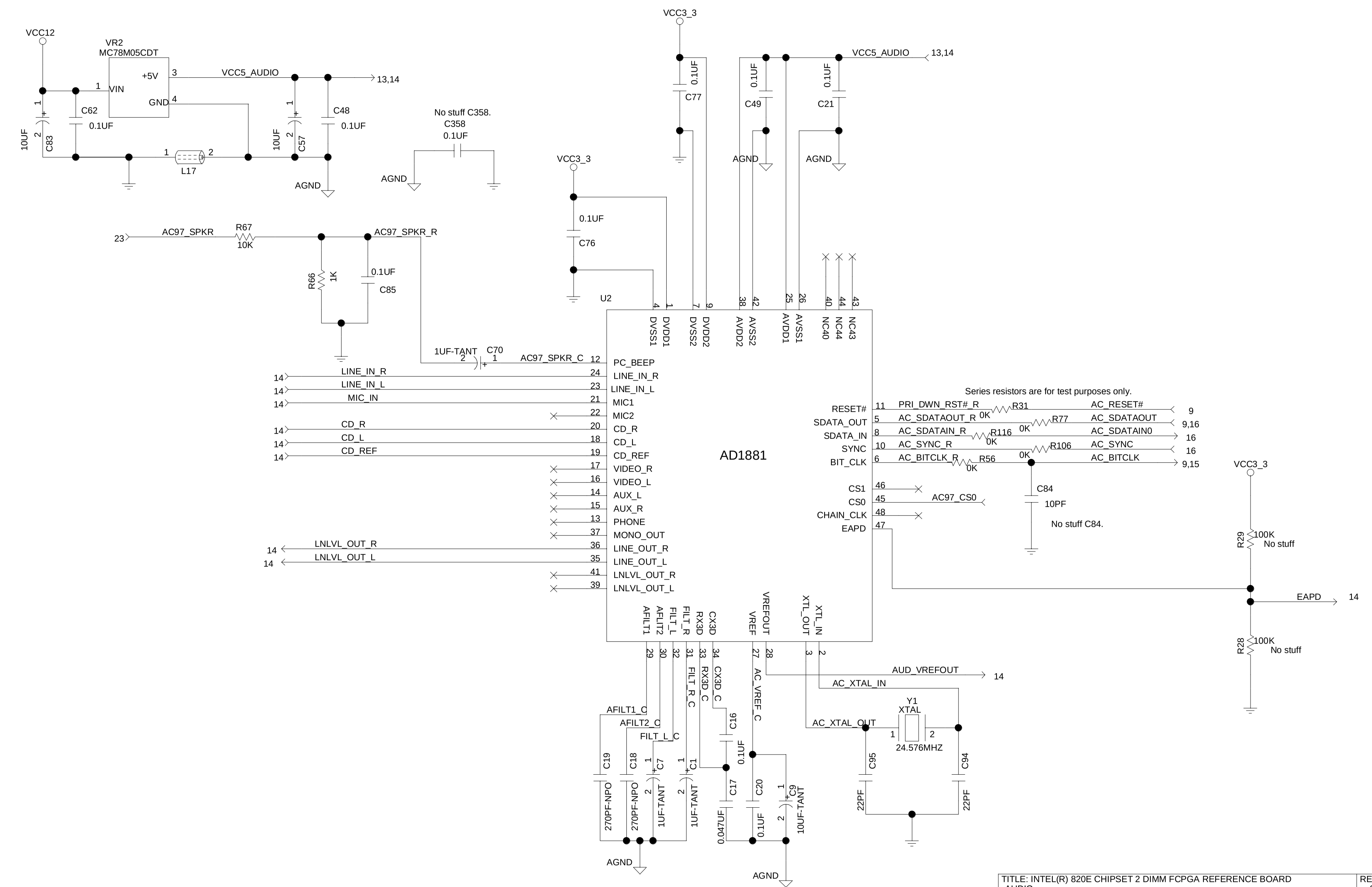
DRAWN BY: PCG AE

PROJECT: Camino2

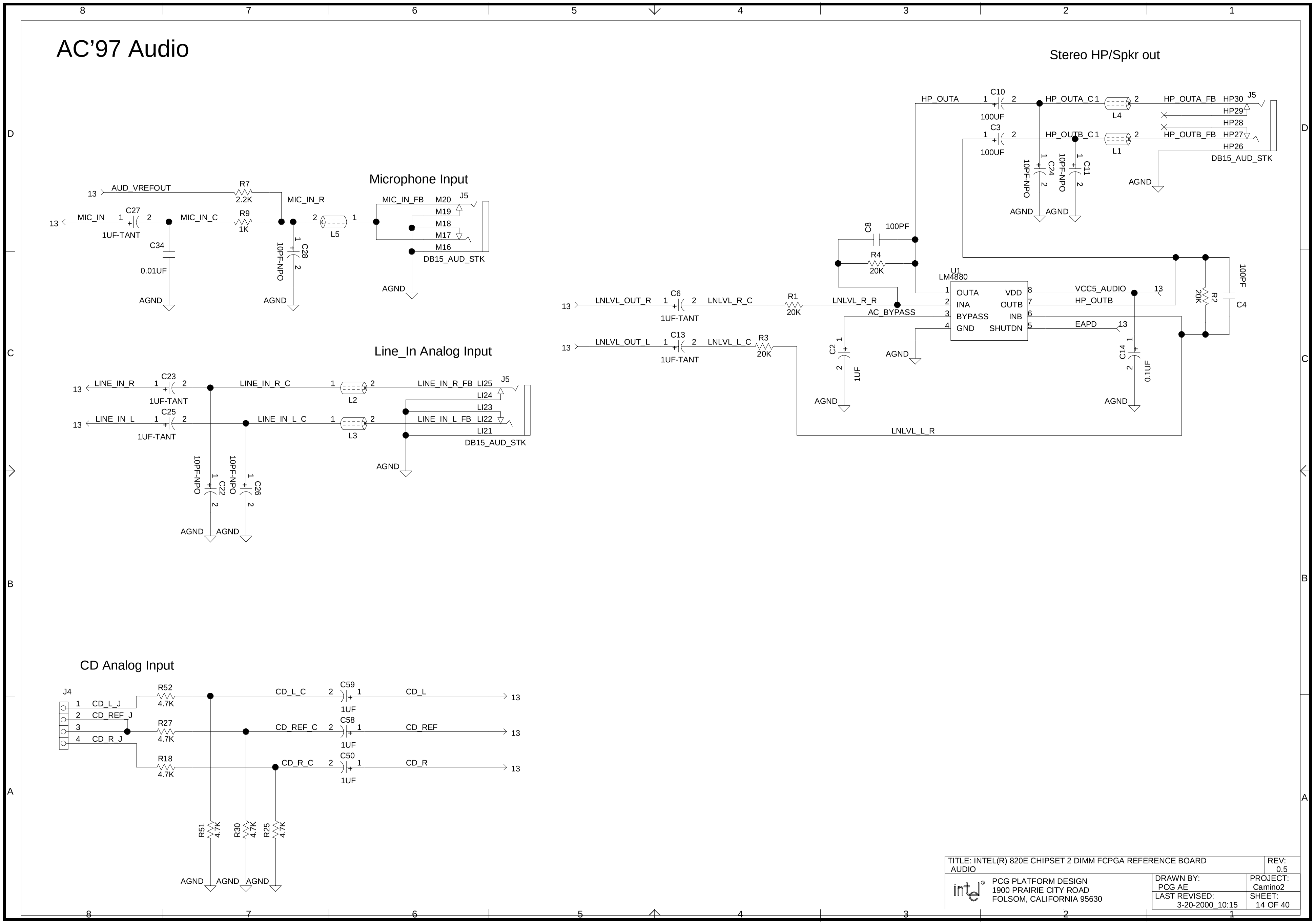
LAST REVISED: 3-20-2000_10:15

SHEET: 12 OF 40

AC'97 Audio

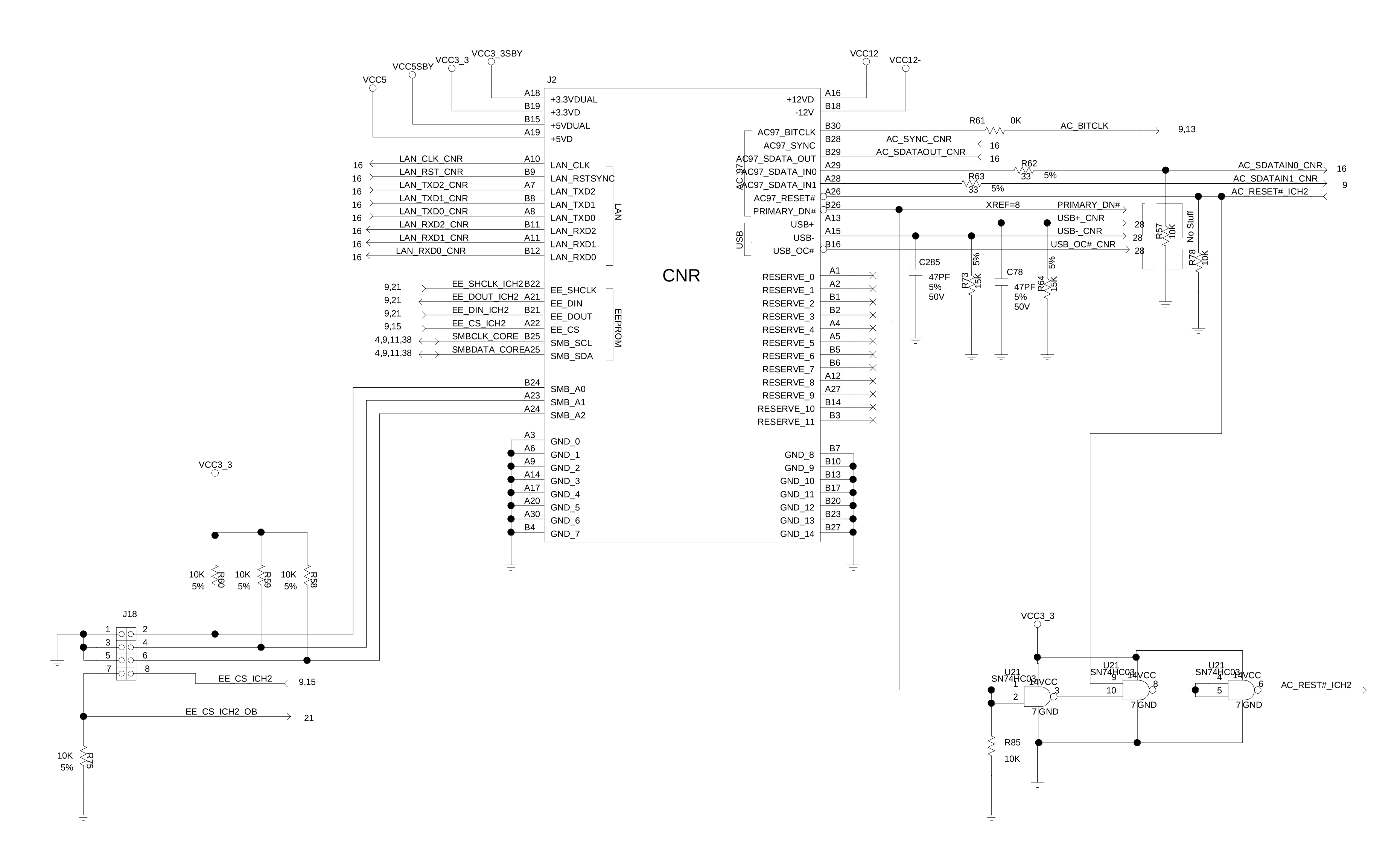


TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD AUDIO	REV: 0.5
PCG PLATFORM DESIGN, 1900 PRAIRIE CITY ROAD, FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE
PROJECT: Camino2	LAST REVISED: 3-20-2000_10:15
SHEET: 13 OF 40	



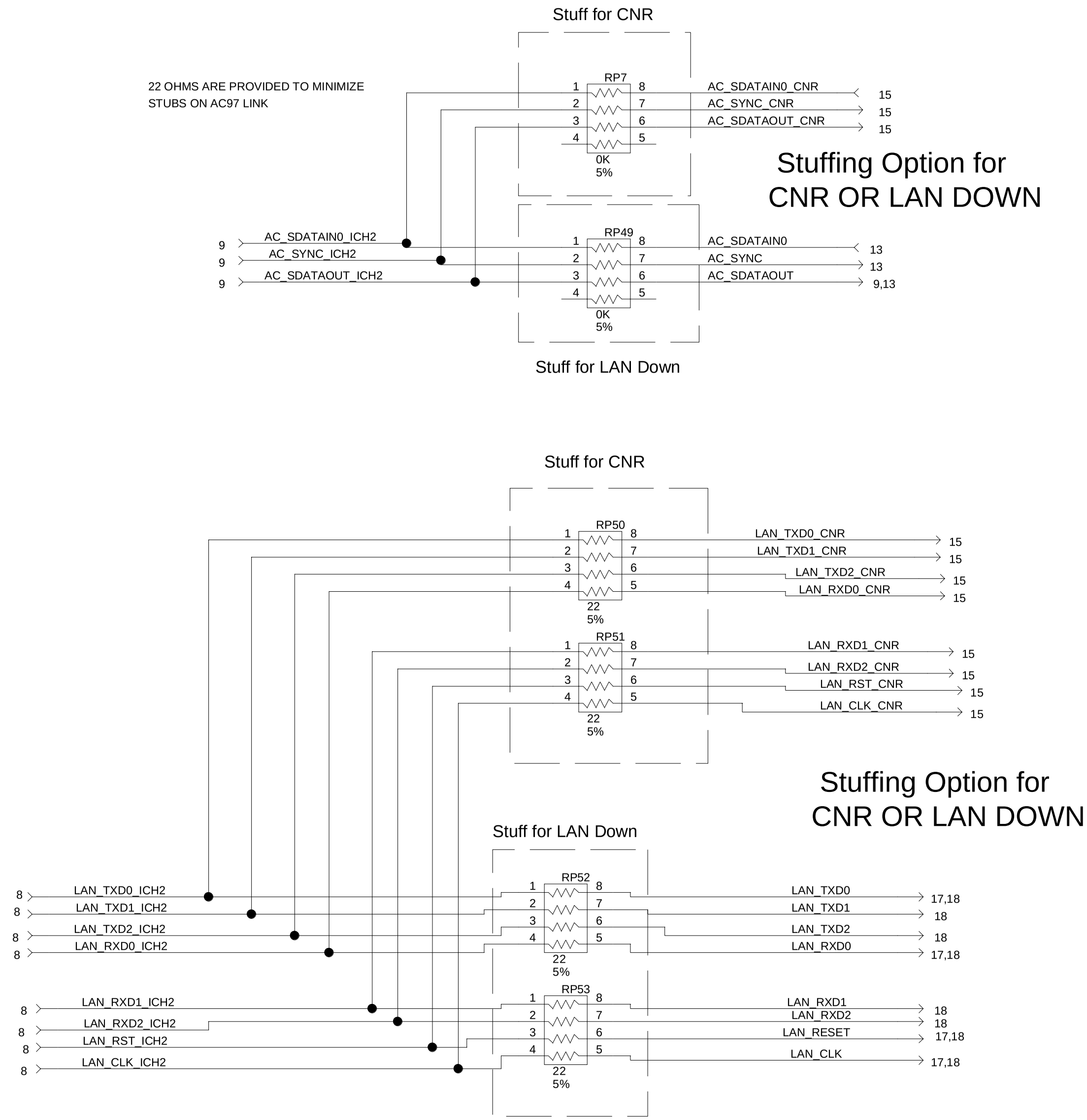
AC'97 Audio
Stereo HP/Spkr out
Microphone Input
Line_In Analog Input
CD Analog Input
HP_OUTA
C10
100UF
C3
100UF
HP_OUTA_C1
HP_OUTB_C1
L4
L1
HP_OUTA_FB
HP_OUTB_FB
HP30
HP29
HP28
HP27
HP26
J5
DB15_AUD_STK
C24
C11
10PF-NPO
AGND
C8
100PF
R4
20K
U1
LM4880
OUTA
INA
BYPASS
GND
VDD
OUTB
INB
SHUTDN
VCC5_AUDIO
HP_OUTB
EAPD
AC_BYPASS
R2
20K
C4
100PF
C2
1UF
C14
0.1UF
LNLVL_OUT_R
C6
1UF-TANT
LNLVL_R_C
R1
20K
LNLVL_R_R
LNLVL_OUT_L
C13
1UF-TANT
LNLVL_L_C
R3
20K
LNLVL_L_R
AUD_VREFOUT
R7
2.2K
MIC_IN_R
MIC_IN
C27
1UF-TANT
MIC_IN_C
R9
1K
C34
0.01UF
C28
10PF-NPO
L5
MIC_IN_FB
M20
M19
M18
M17
M16
LINE_IN_R
C23
1UF-TANT
LINE_IN_R_C
L2
LINE_IN_R_FB
LI25
LI24
LI23
LI22
LI21
LINE_IN_L
C25
1UF-TANT
LINE_IN_L_C
L3
LINE_IN_L_FB
C22
C26
J4
CD_L_J
CD_REF_J
CD_R_J
R52
4.7K
R27
4.7K
R18
4.7K
CD_L_C
CD_REF_C
CD_R_C
C59
1UF
C58
1UF
C50
1UF
CD_L
CD_REF
CD_R
R51
4.7K
R30
4.7K
R25
4.7K
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
AUDIO
REV:
0.5
intel
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY:
PCG AE
PROJECT:
Camino2
LAST REVISED:
3-20-2000_10:15
SHEET:
14 OF 40

Communication And Network Riser (CNR)



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD COMMUNICATION AND NETWORK RISER (CNR)		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED: 3-20-2000_14:56	PROJECT: Camino2 SHEET: 15 OF 40

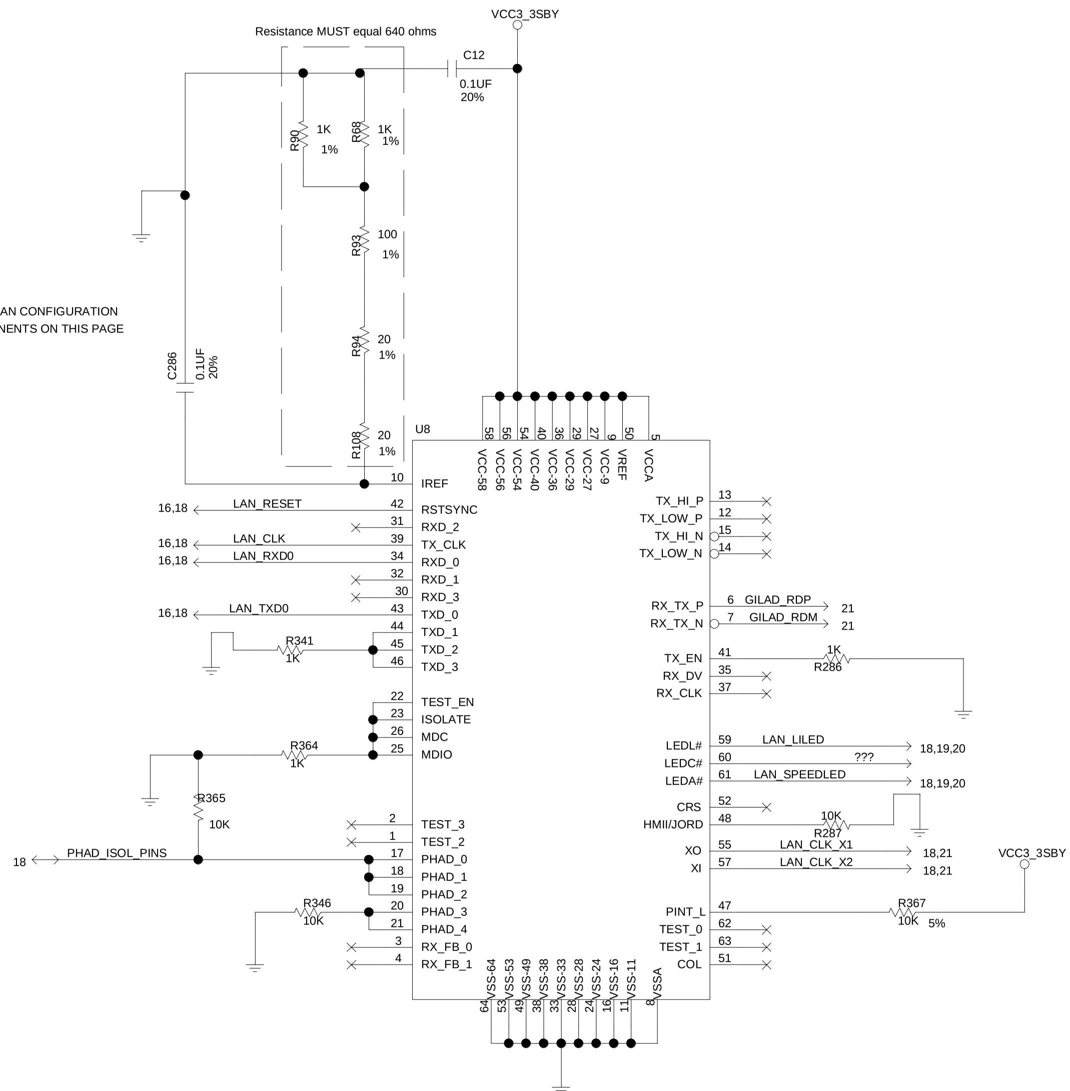
ICH2 AC97 AND CNR LINK STUFFING OPTIONS



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD ICH2 AC97 AND CNR STUFFING OPTIONS		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:29	SHEET: 16 OF 40

LAN (82562EH)

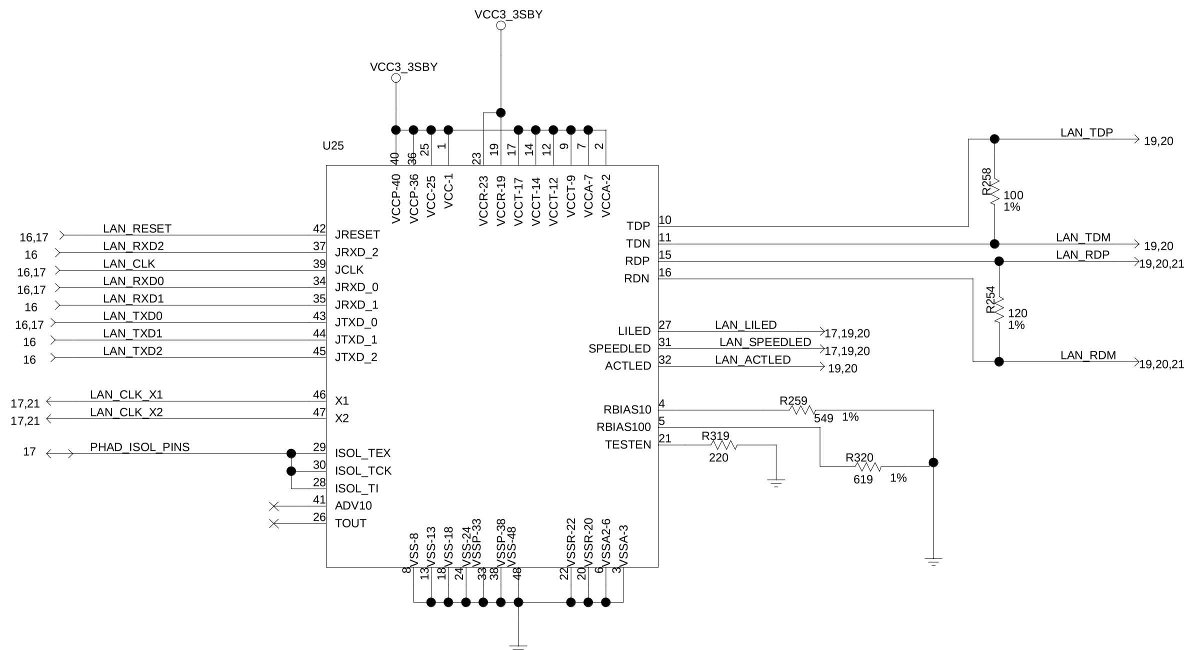
NOTE: FOR HOME LAN CONFIGURATION
STUFF ALL COMPONENTS ON THIS PAGE



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD LAN (82562EH)		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:29	SHEET: 17 OF 40

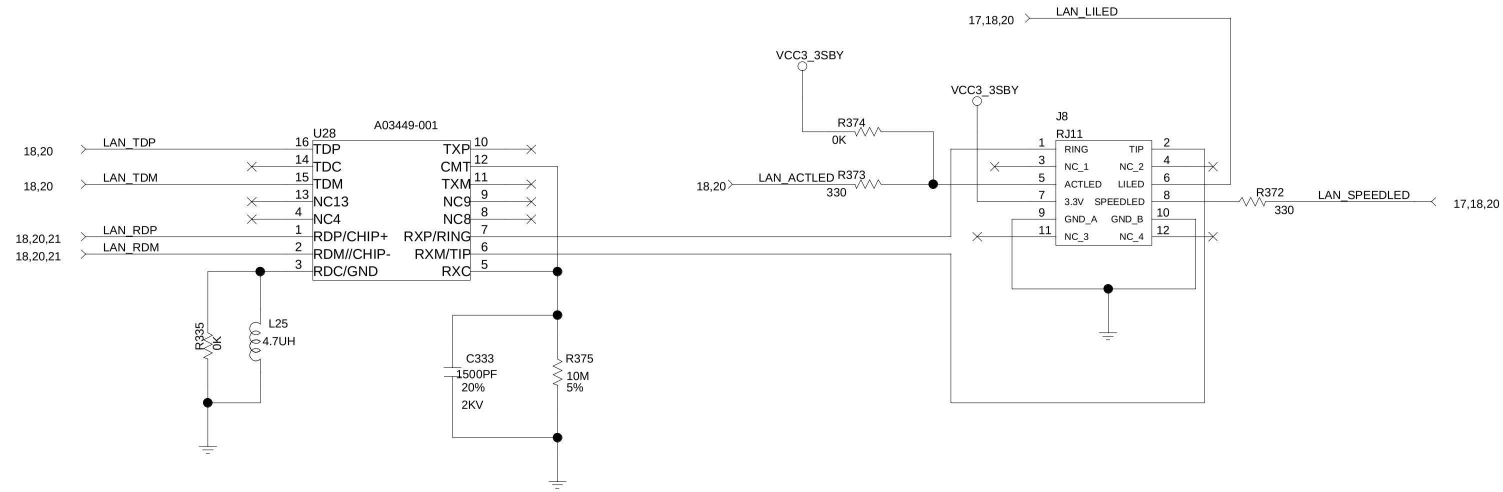
LAN (82562ET/EM)

NOTE: FOR HOME LAN CONFIGURATION
EMPTY ALL COMPONENTS ON THIS PAGE



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD LAN (82562ET)		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:29	SHEET: 18 OF 40

LAN (RJ11 For 82562EH)



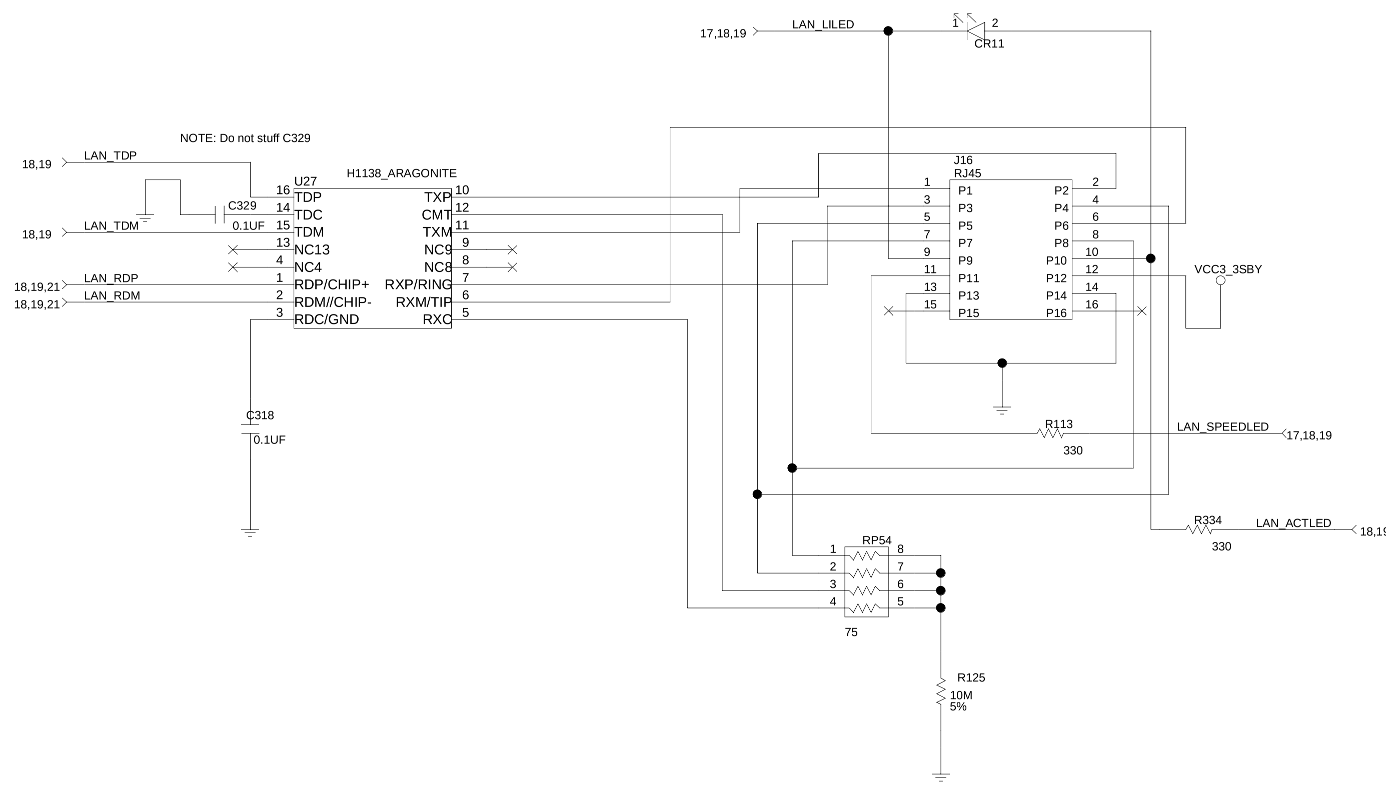
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
LAN (RJ11)

REV: 0.5

PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

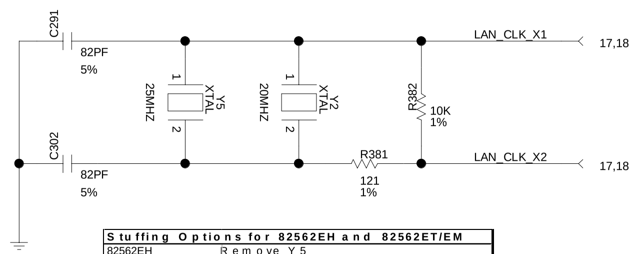
DRAWN BY: PCG AE
PROJECT: Camino2
LAST REVISED: 3-20-2000_14:53
SHEET: 19 OF 40

LAN (RJ45 For 82562ET/EM)

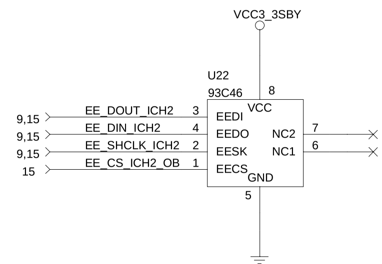


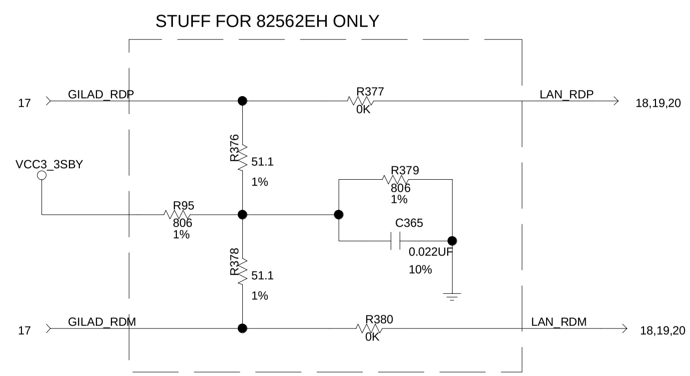
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD LAN (RJ45)	REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED: 3-20-2000_16:55 PROJECT: Camino2 SHEET: 20 OF 40

LAN



Stuffing Options for 82562EH and 82562ET/EM	
82562EH	Remove Y5
	C291 and C302=82pf
	R381=121ohms
82562ET/EM	Remove Y2
	C291 and C302=22pf
	R381=0 ohms
	Remove R382





STUFFING FOR EEPROM (U22)	
LAN OPTION	INTEL PART#
82562EH	A05482-001
82562ET	A05441-001
82562EM	A05723-001
82562EM with AOL	

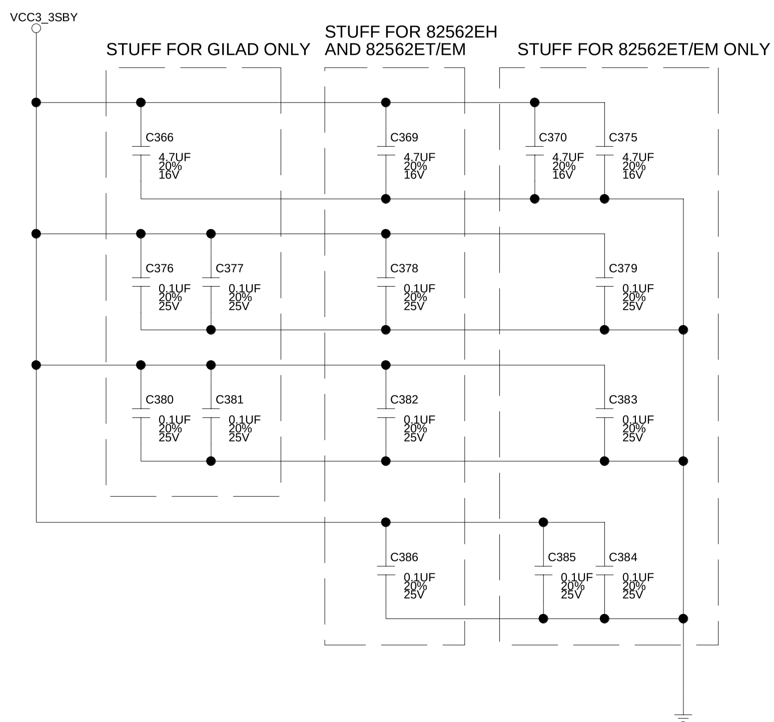
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
LAN
REV: 0.5

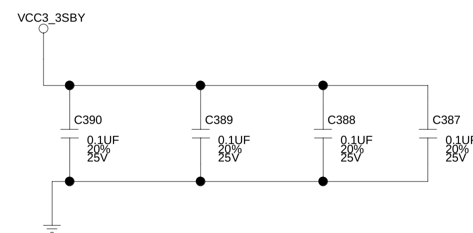
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

DRAWN BY: PCG AE
PROJECT: Camino2
LAST REVISED: 3-20-2000_11:31
SHEET: 21 OF 40

LAN

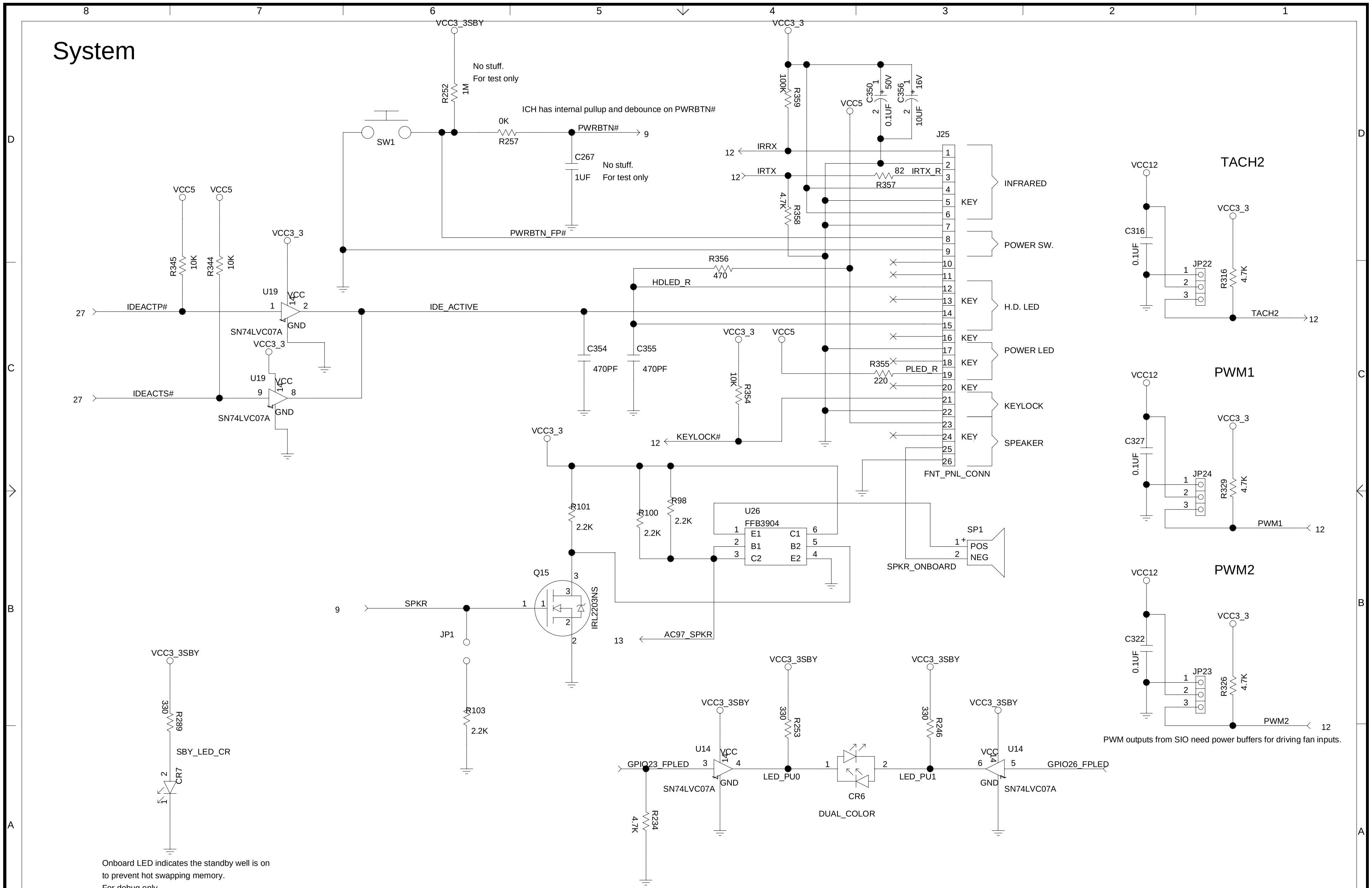
NOTES:
1: Bulk Caps (4.7uf) should be palced 1 per side around
Kennereth/+ and 0.1uf caps should be placed near PWR/GND
and high speed signals.
2: Include at least 0.1uf cap per EEPROM





TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD LAN		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED:	SHEET: 22 OF 40

System



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
SYSTEM

REV: 0.5

PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

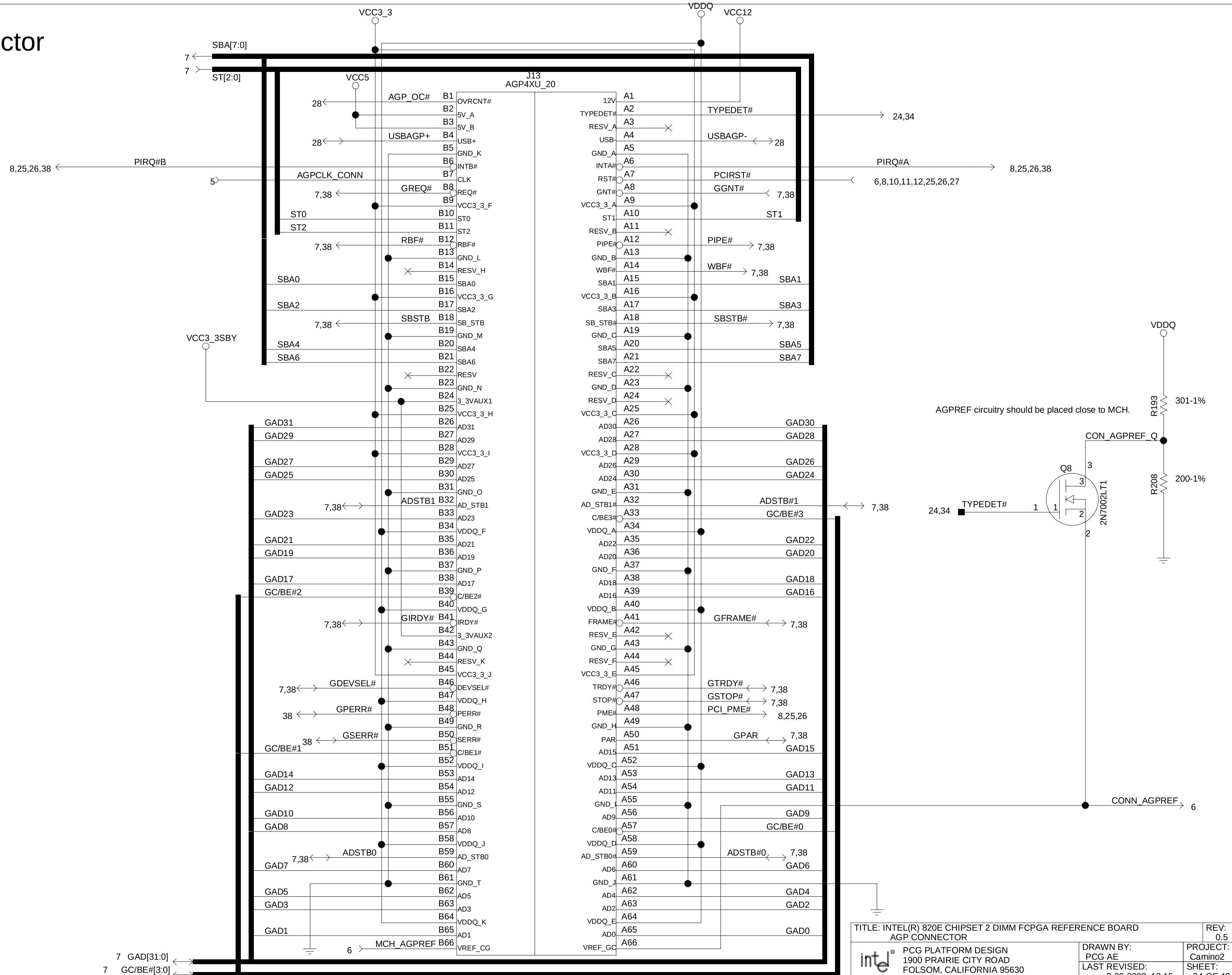
DRAWN BY: PCG AE

PROJECT: Camino2

LAST REVISED: 3-20-2000_11:31

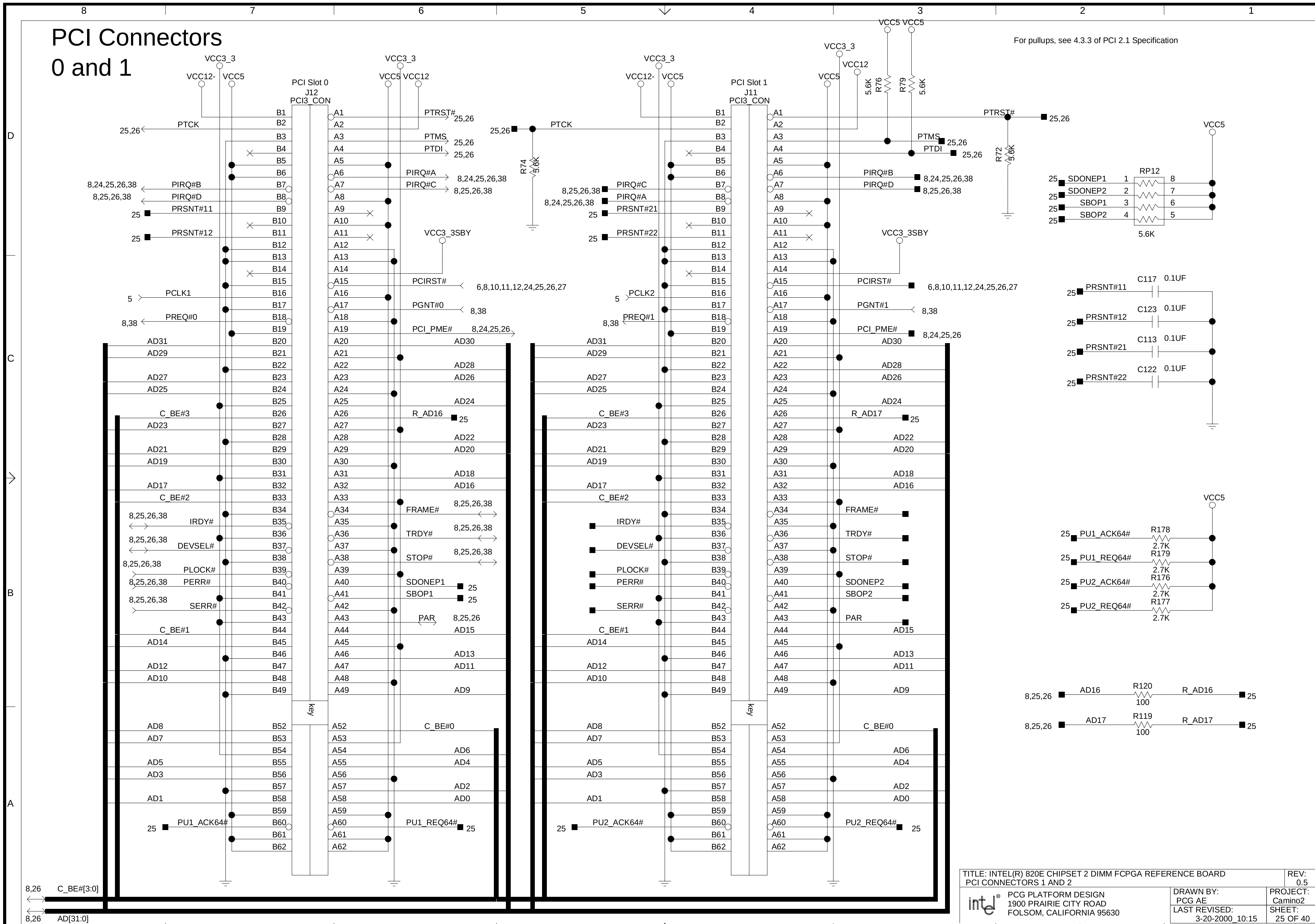
SHEET: 23 OF 40

AGP Connector



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
AGP CONNECTOR
REV: 0.5
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630
DRAWN BY: PCG AE
PROJECT: Camino2
LAST REVISED: 3-20-2000_10:15
SHEET: 24 OF 40

PCI Connectors 0 and 1



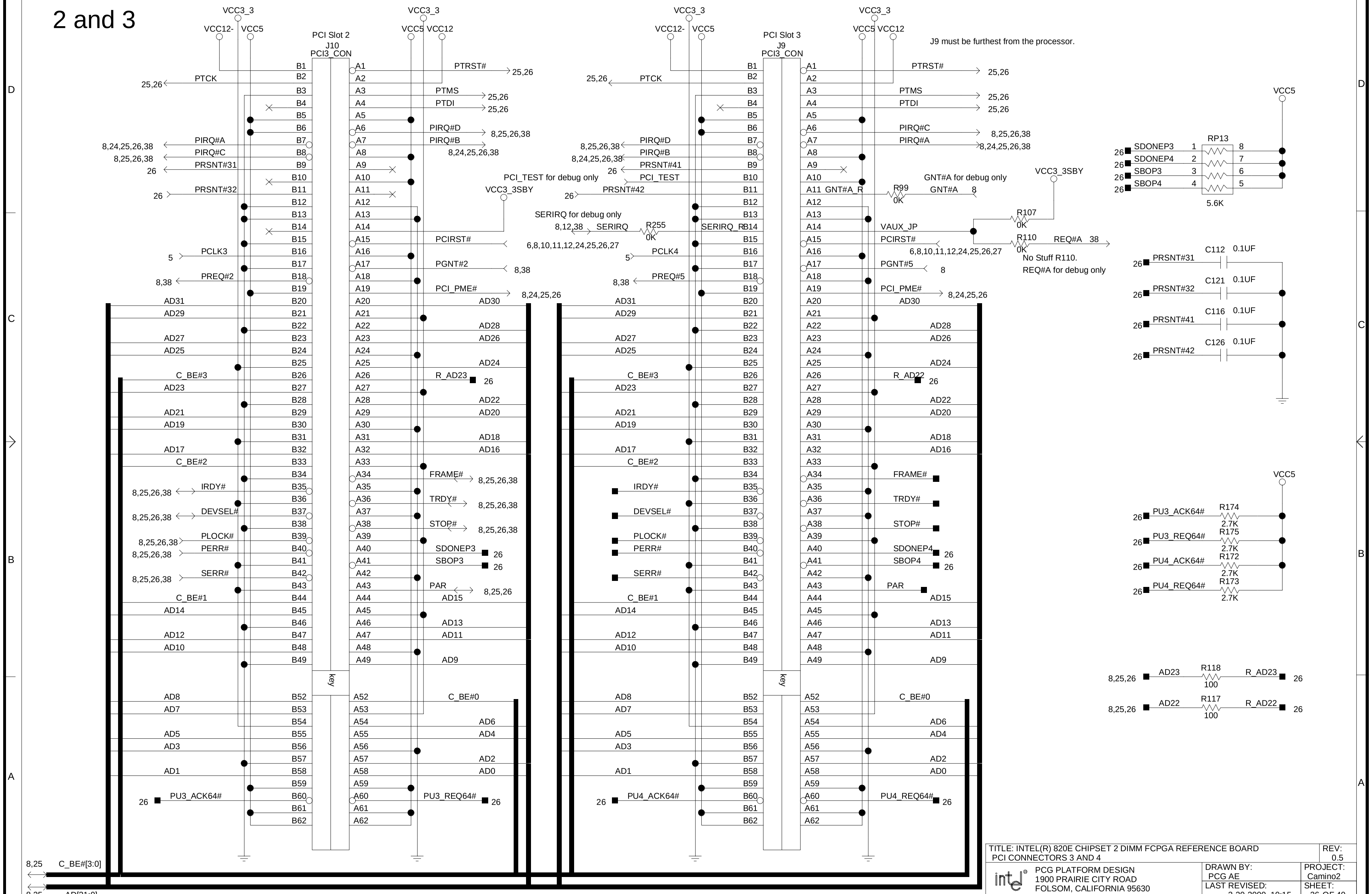
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
PCI CONNECTORS 1 AND 2

REV: 0.5

intel®
PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

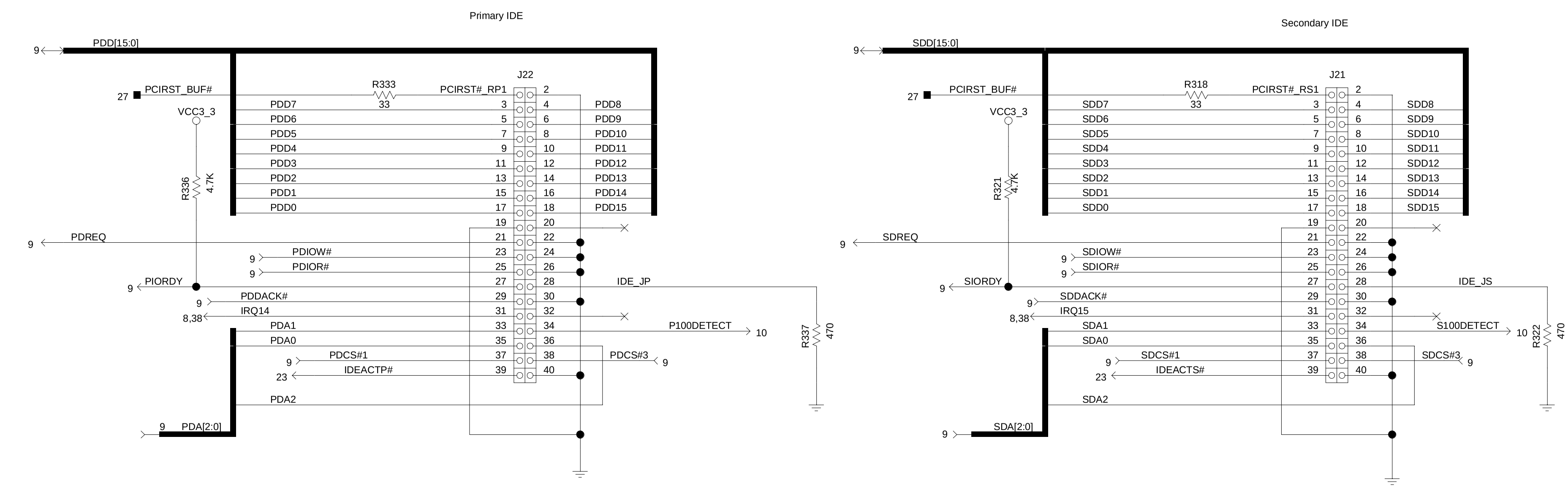
DRAWN BY: PCG AE
PROJECT: Camino2
LAST REVISED: 3-20-2000_10:15
SHEET: 25 OF 40

PCI Connectors 2 and 3

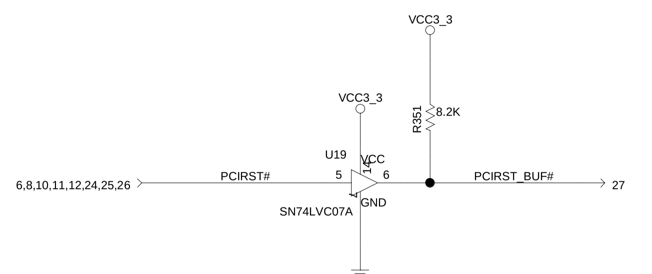


TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD PCI CONNECTORS 3 AND 4		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED: 3-20-2000_10:15	PROJECT: Camino2 SHEET: 26 OF 40

IDE Connectors

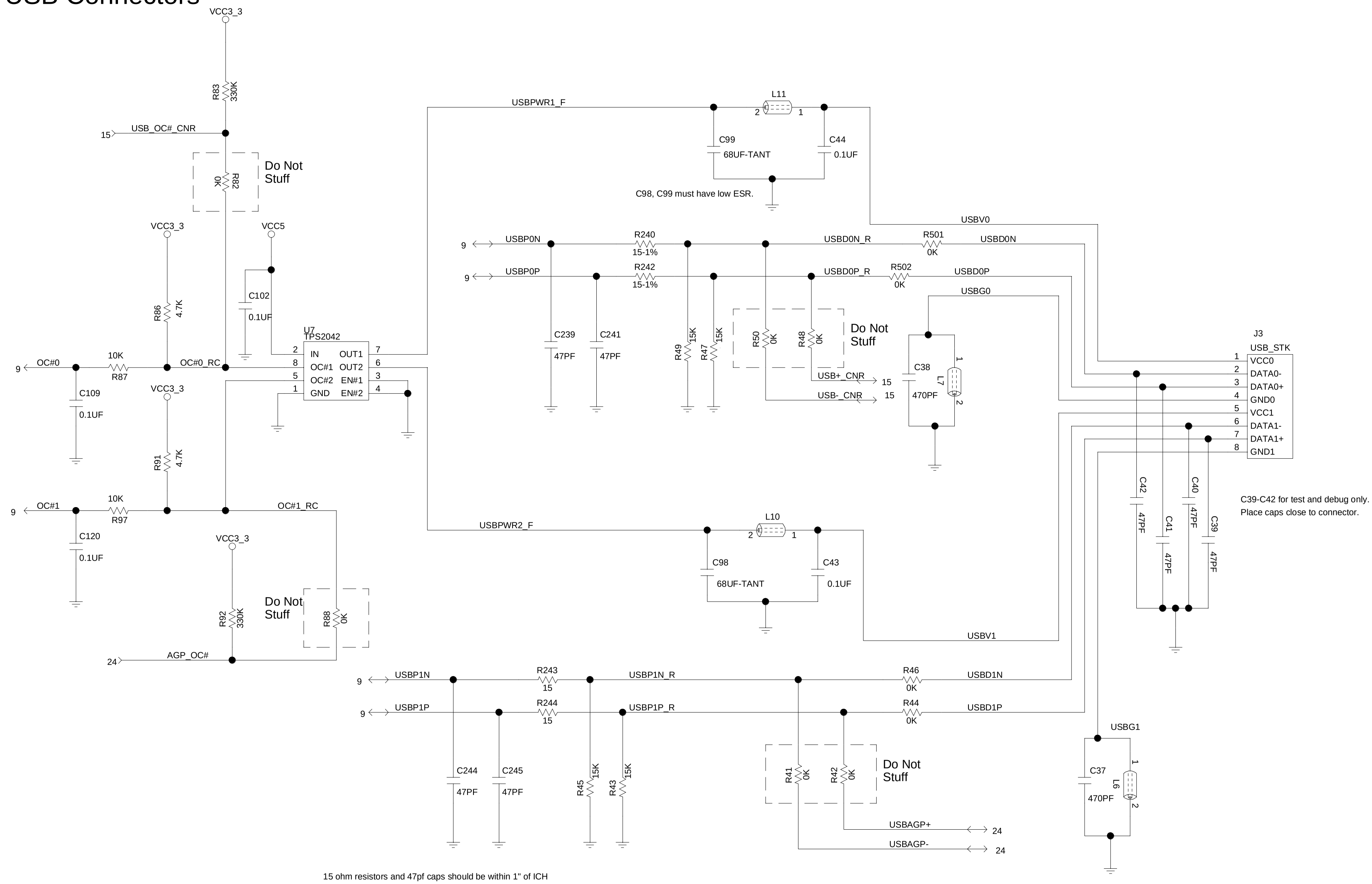


For drive side detection, stuff C329,C318.
For host side detection, no stuff C329,C318.
P100DETECT and S100DETECT can be connected to a GPI for BIOS cable detection.



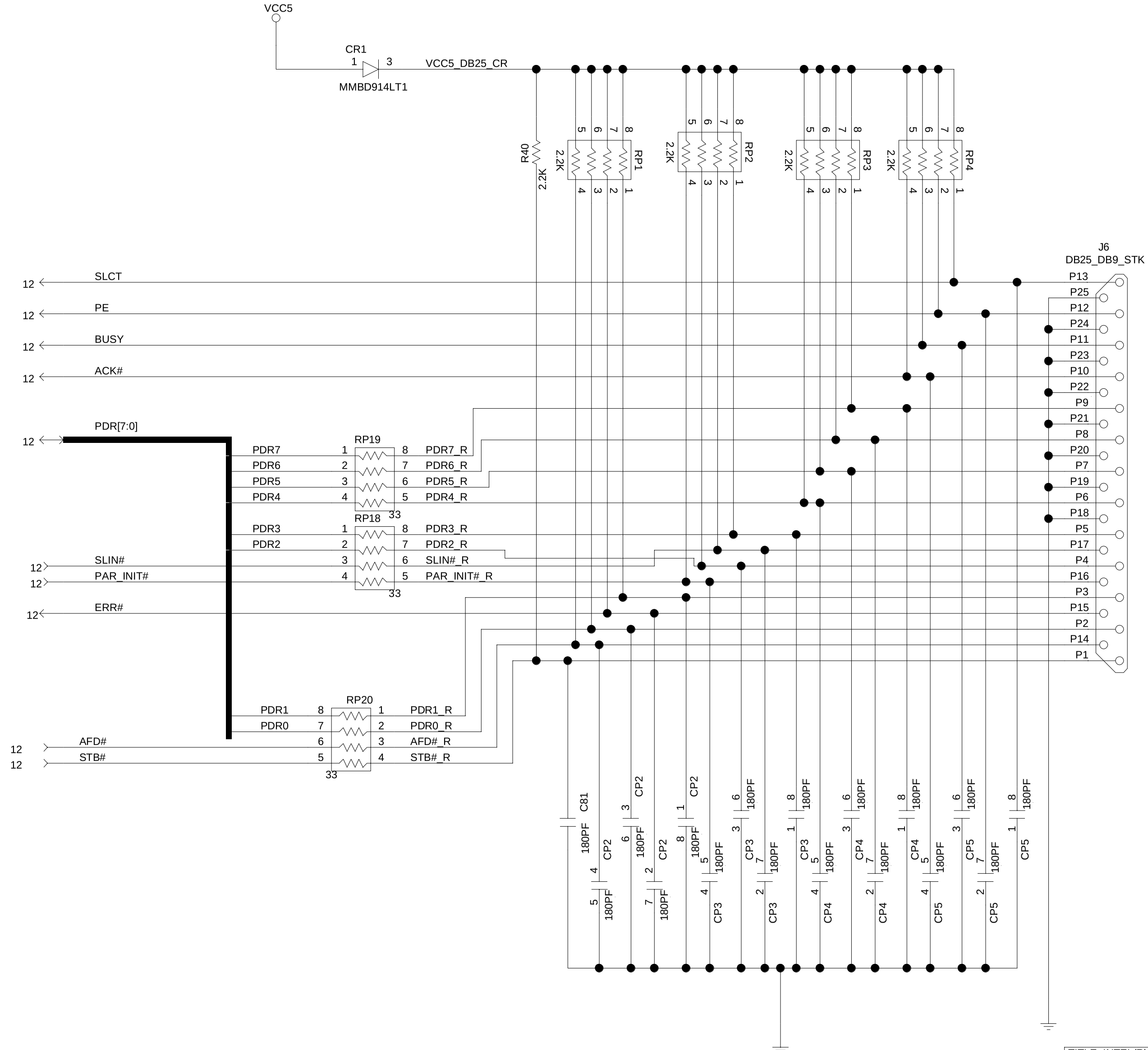
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD IDE CONNECTORS		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 27 OF 40

USB Connectors



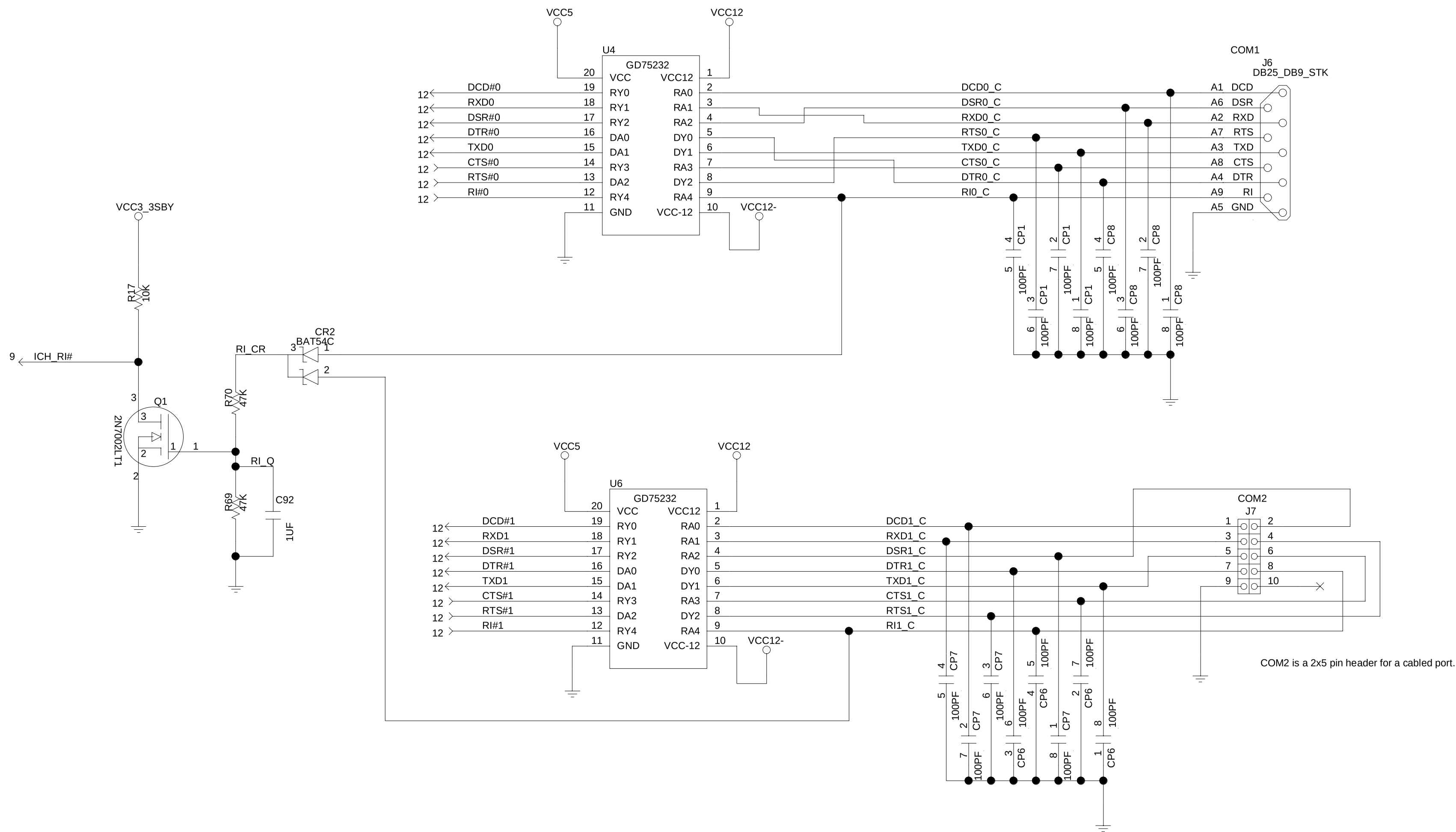
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD USB CONNECTORS			REV: 0.5
intel®	PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
		LAST REVISED: 3-20-2000_10:15	SHEET: 28 OF 40

Parallel Port



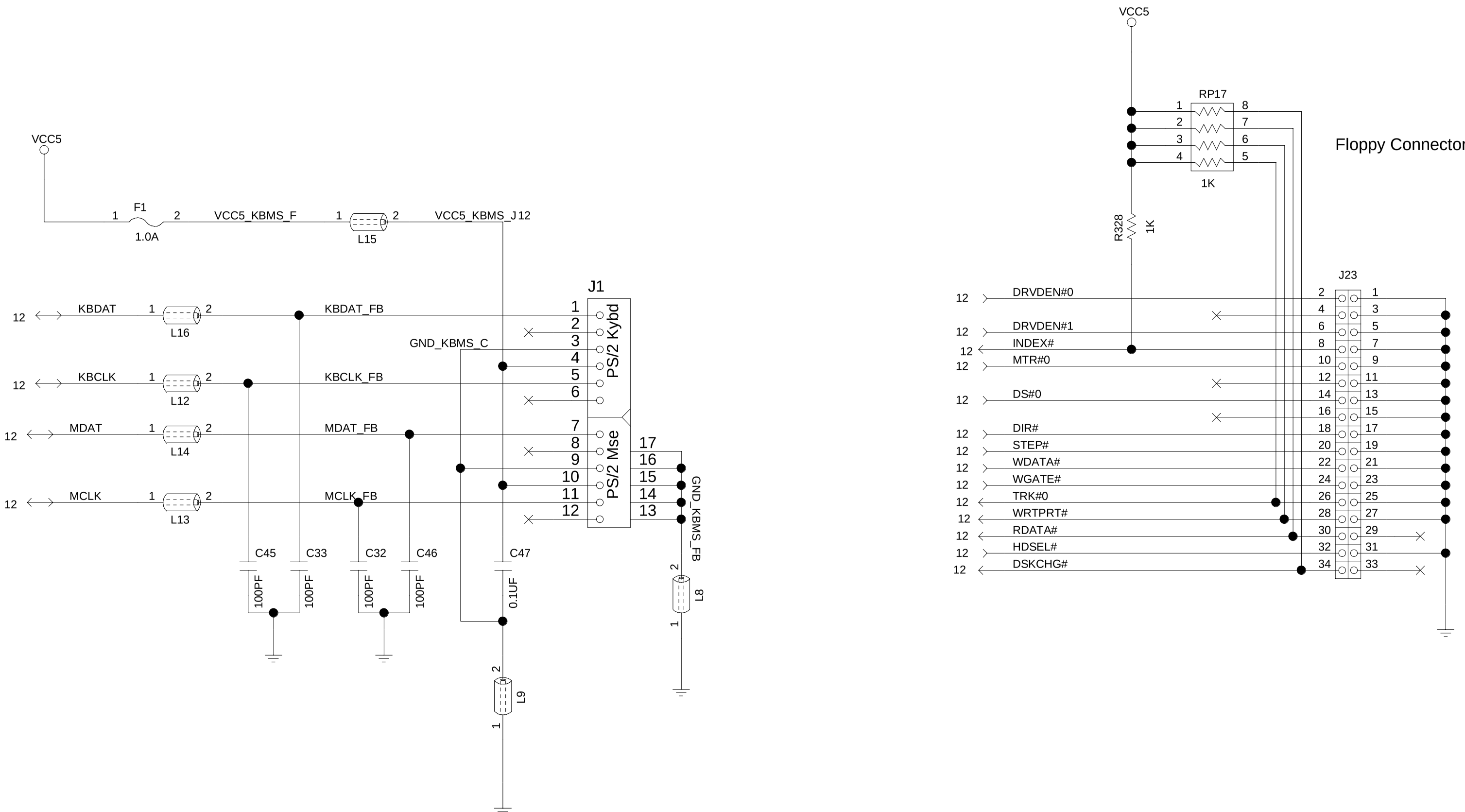
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD PARALLEL PORT		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 29 OF 40

Serial Ports



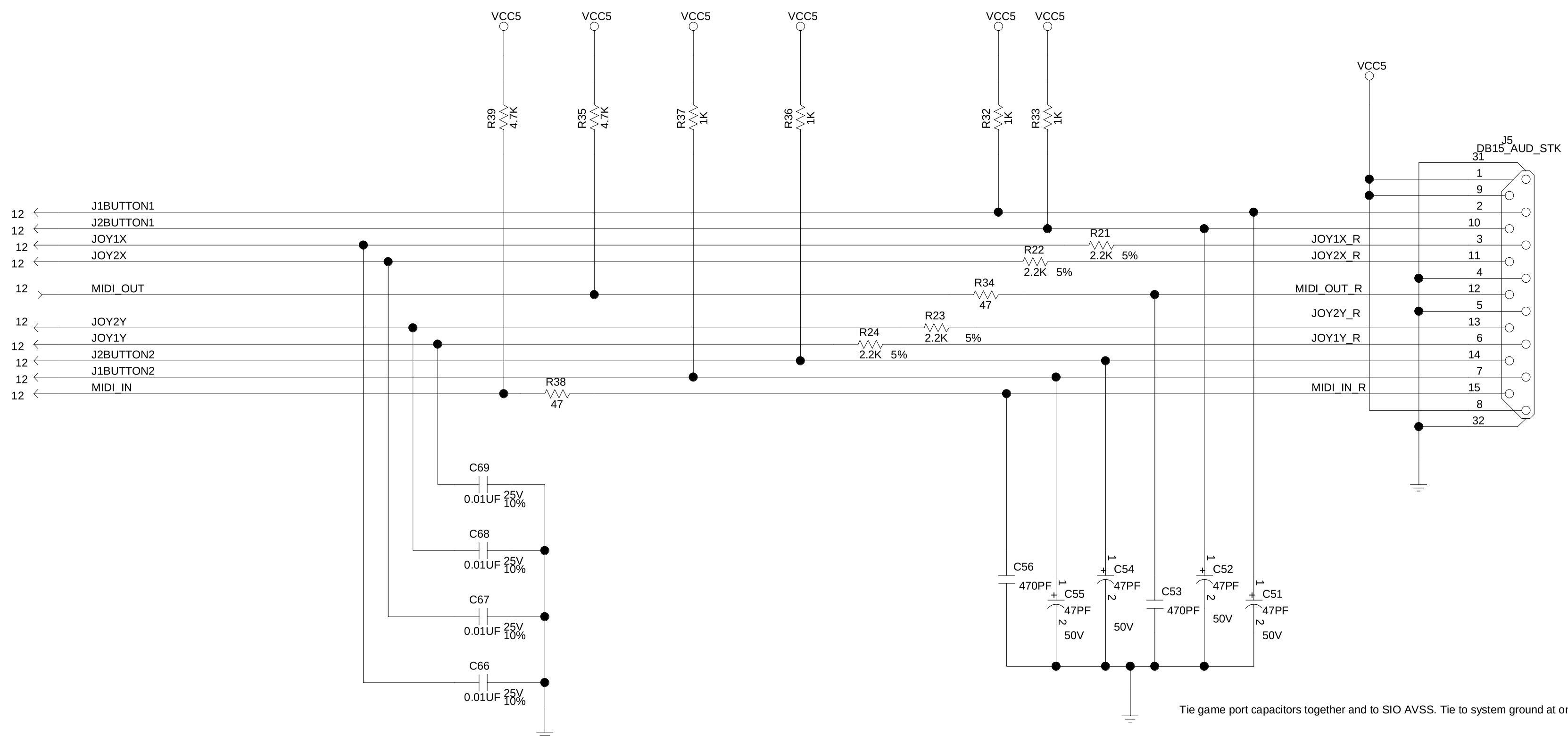
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD SERIAL PORTS			REV: 0.5
intel®	PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
		LAST REVISED: 3-20-2000_10:15	SHEET: 30 OF 40

Keyboard/Mouse/Floppy



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD KEYBOARD/MOUSE/FLOPPY			REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2	
	LAST REVISED: 3-20-2000_10:15	SHEET: 31 OF 40	

Game Port

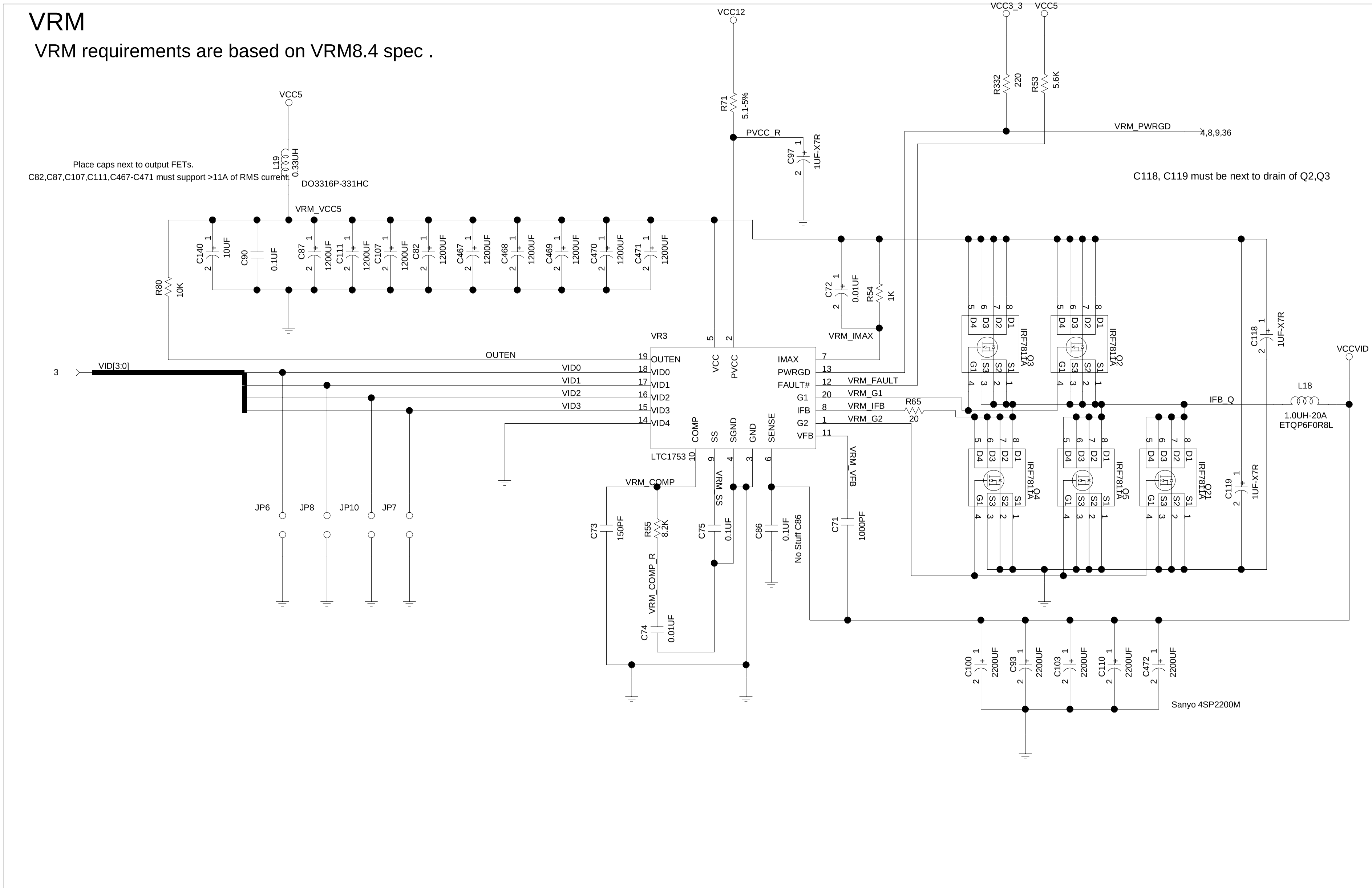


Tie game port capacitors together and to SIO AVSS. Tie to system ground at only a single point.

TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD GAME PORT		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED:	PROJECT: Camino2 SHEET: 32 OF 40

VRM

VRM requirements are based on VRM8.4 spec .



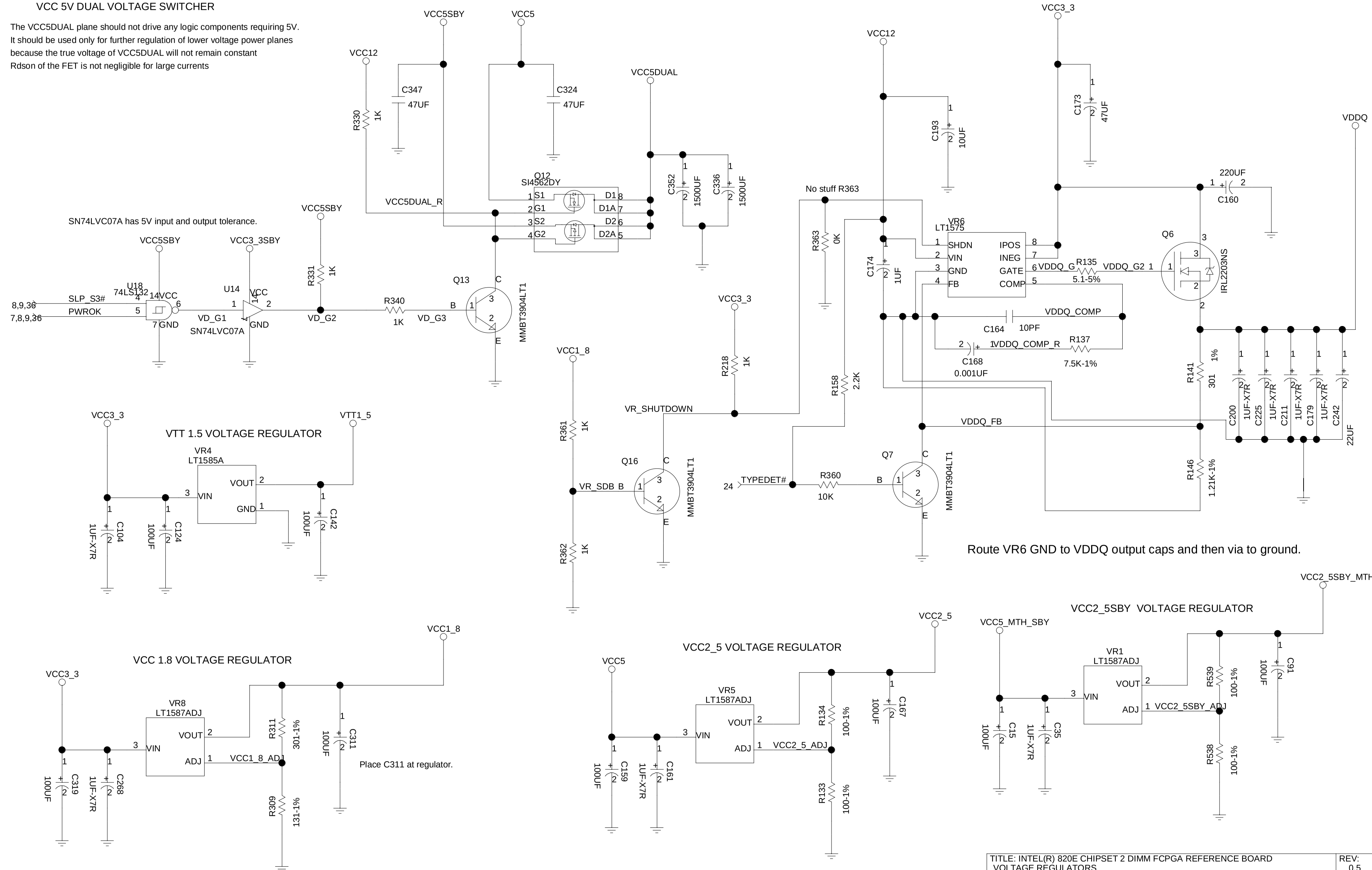
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD VRM 8.4		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 33 OF 40

Voltage Regulators

VCC 5V DUAL VOLTAGE SWITCHER

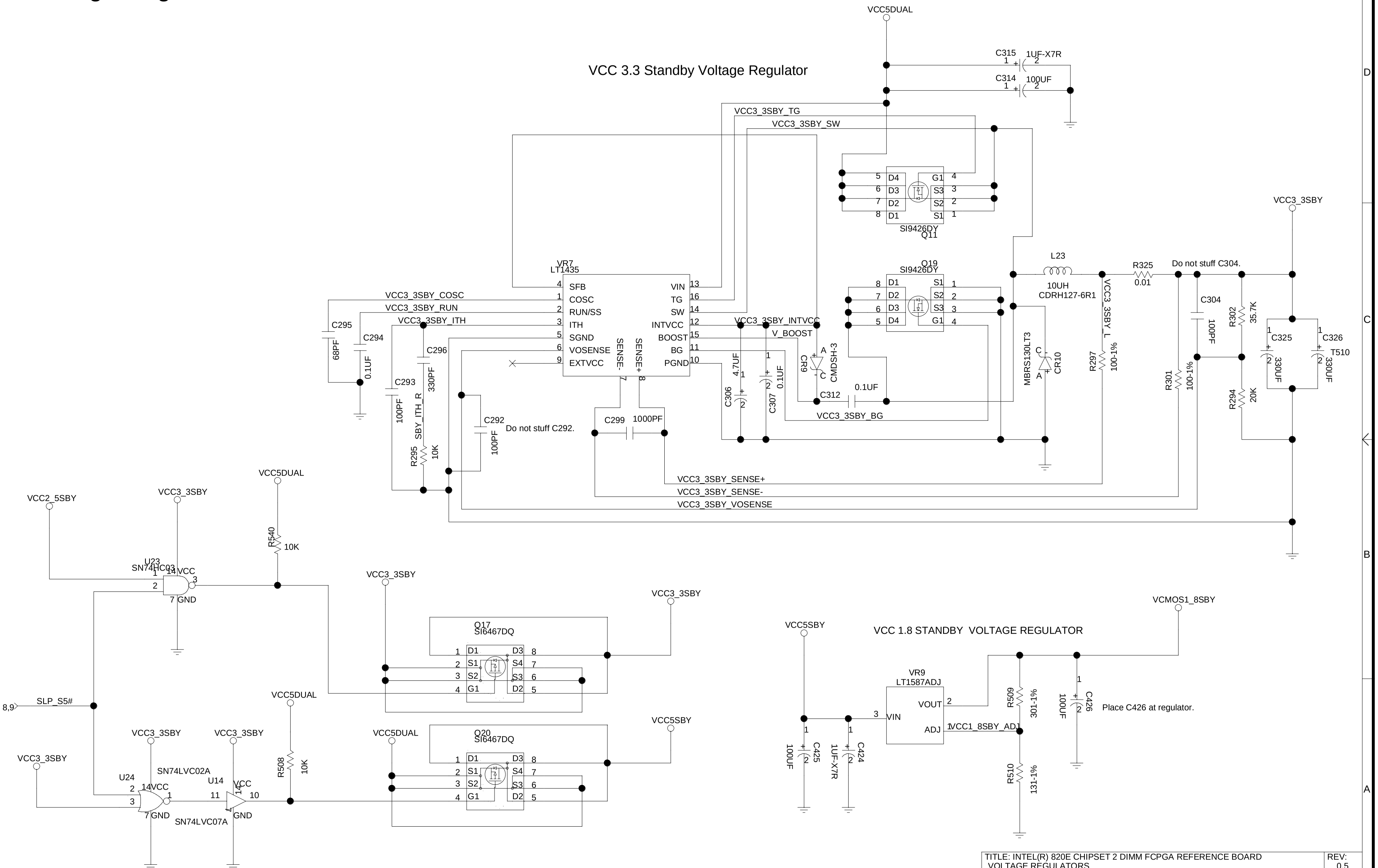
The VCC5DUAL plane should not drive any logic components requiring 5V.
It should be used only for further regulation of lower voltage power planes
because the true voltage of VCC5DUAL will not remain constant
Rdson of the FET is not negligible for large currents

SN74LVC07A has 5V input and output tolerance.



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD VOLTAGE REGULATORS		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 34 OF 40

Voltage Regulators



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
VOLTAGE REGULATORS

REV: 0.5

intel® PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

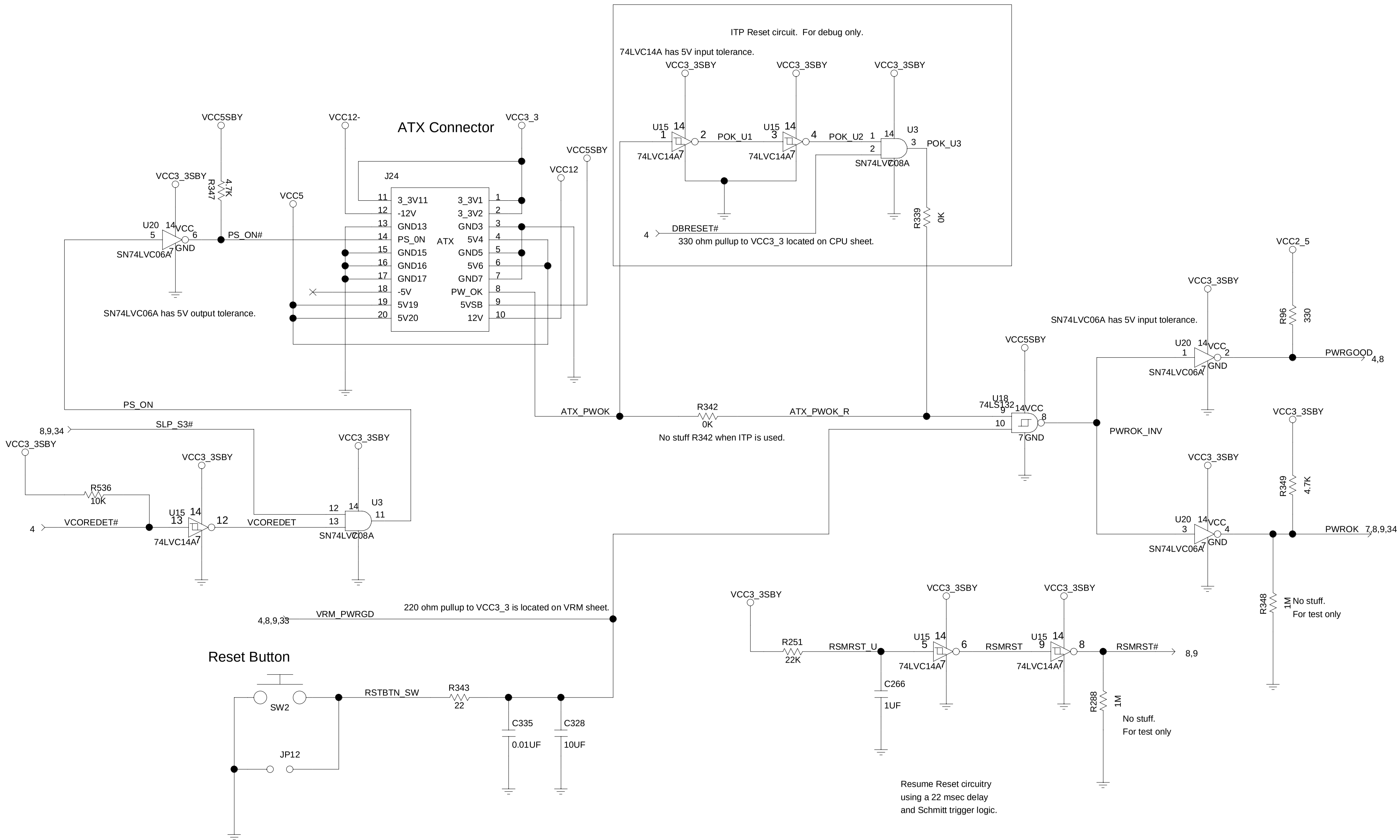
DRAWN BY: PCG AE

PROJECT: Camino2

LAST REVISED: 3-20-2000_10:15

SHEET: 35 OF 40

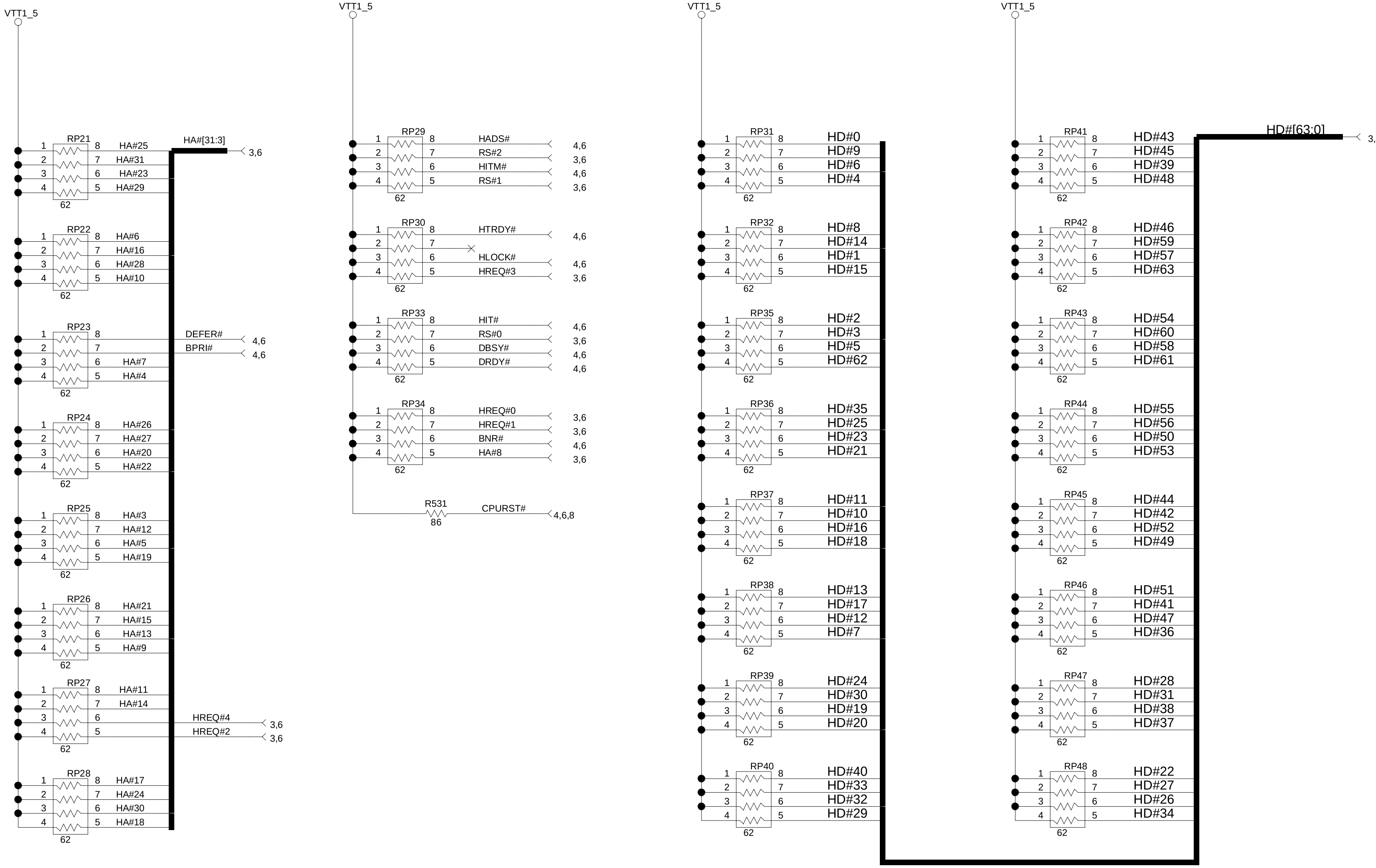
Power Connector



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
POWER CONNECTOR

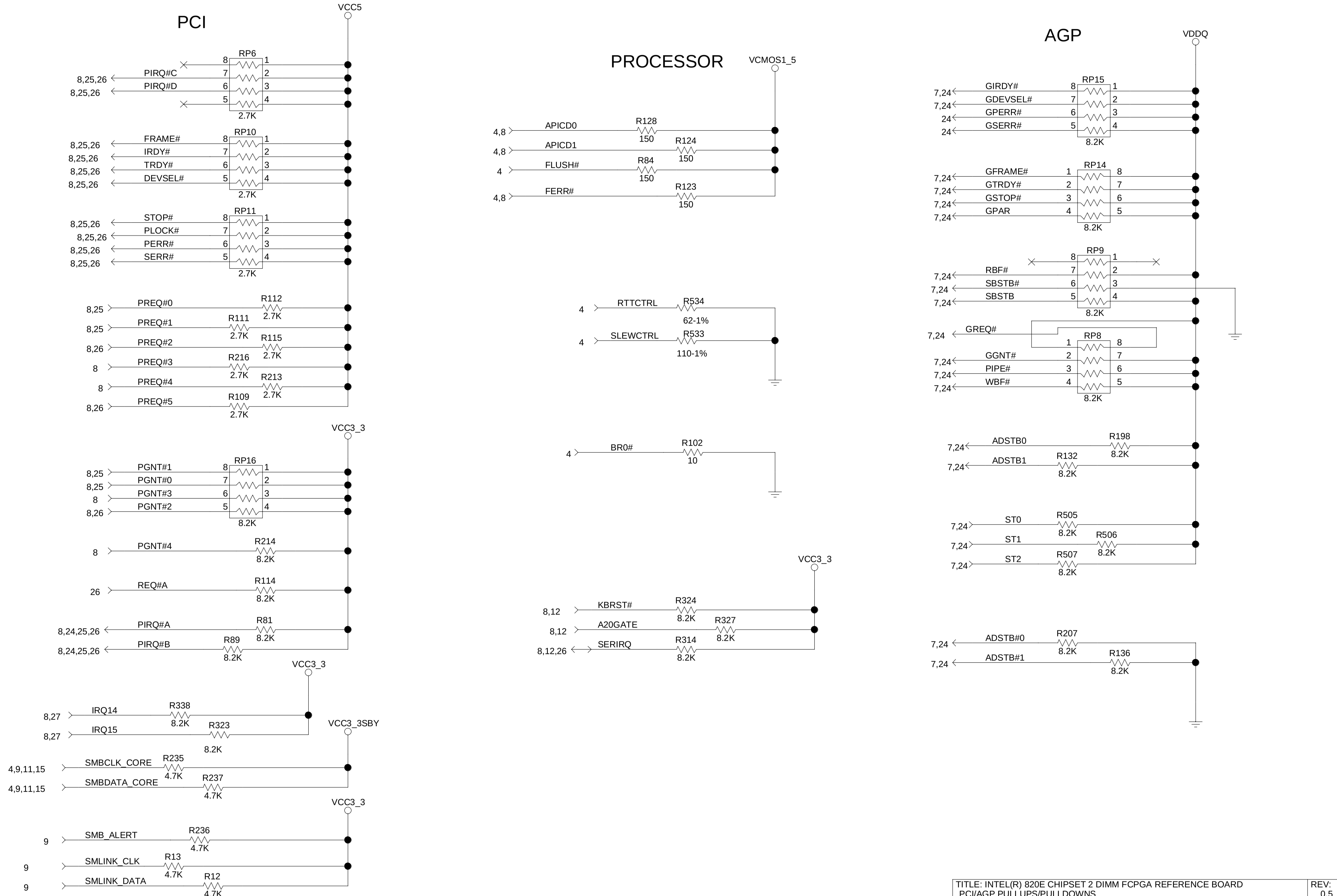
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 36 OF 40
		REV: 0.5

AGTL Termination



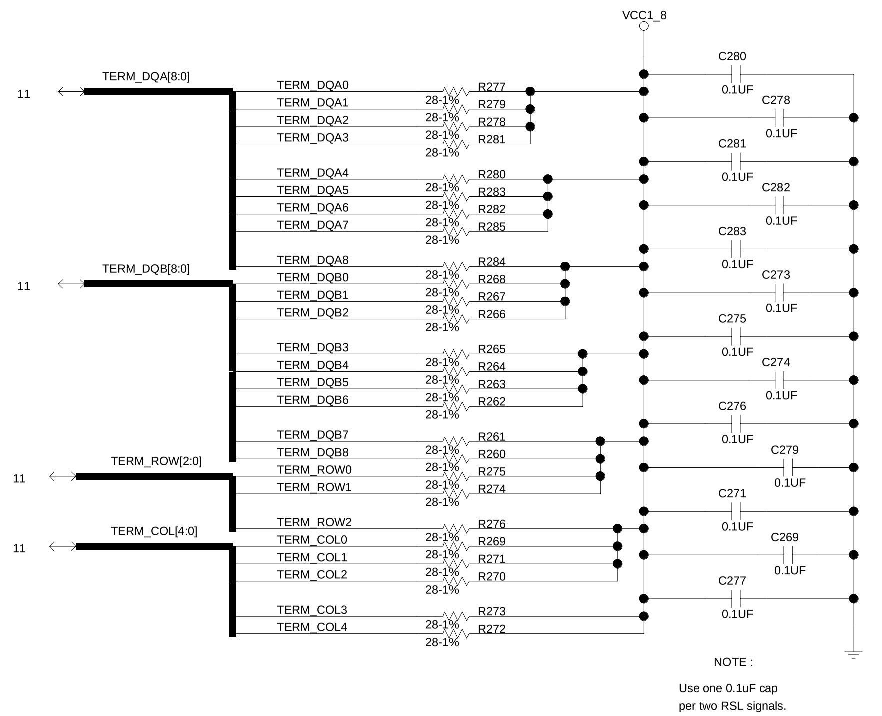
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD AGTL TERMINATION			REV: 0.5
intel®	PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
		LAST REVISED: 3-20-2000_10:15	SHEET: 37 OF 40

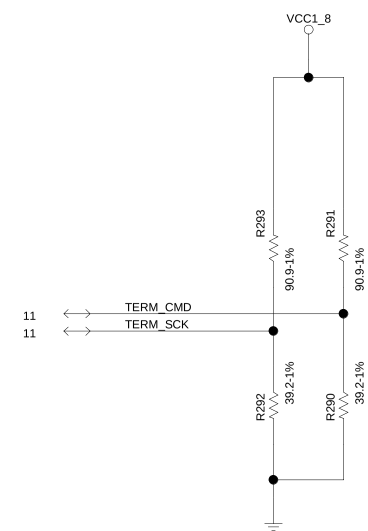
PCI/AGP Pullups/Pulldowns



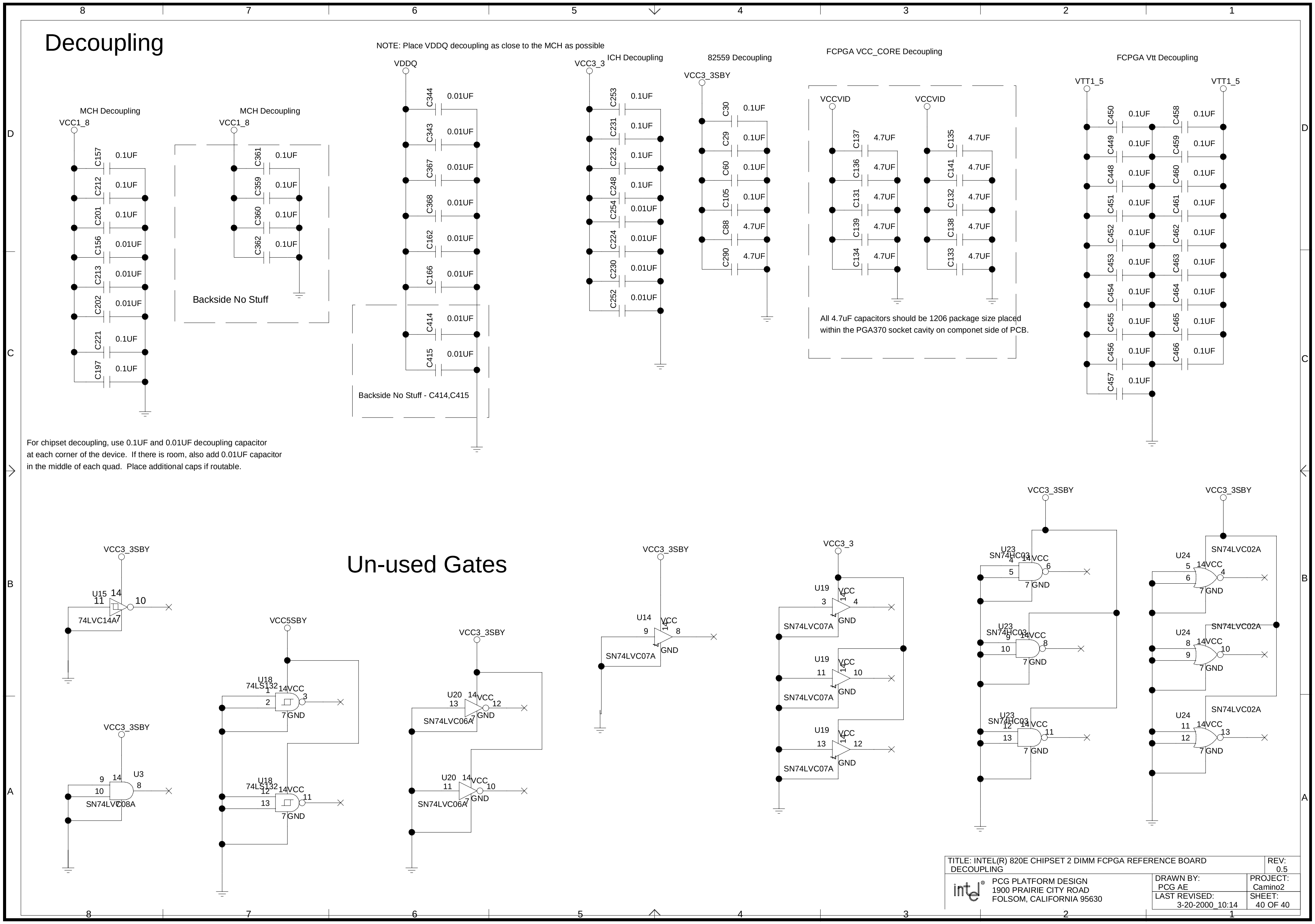
TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD PCI/AGP PULLUPS/PULLDOWNS		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 38 OF 40

Rambus* Termination





TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD RAMBUS TERMINATION		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:15	SHEET: 39 OF 40

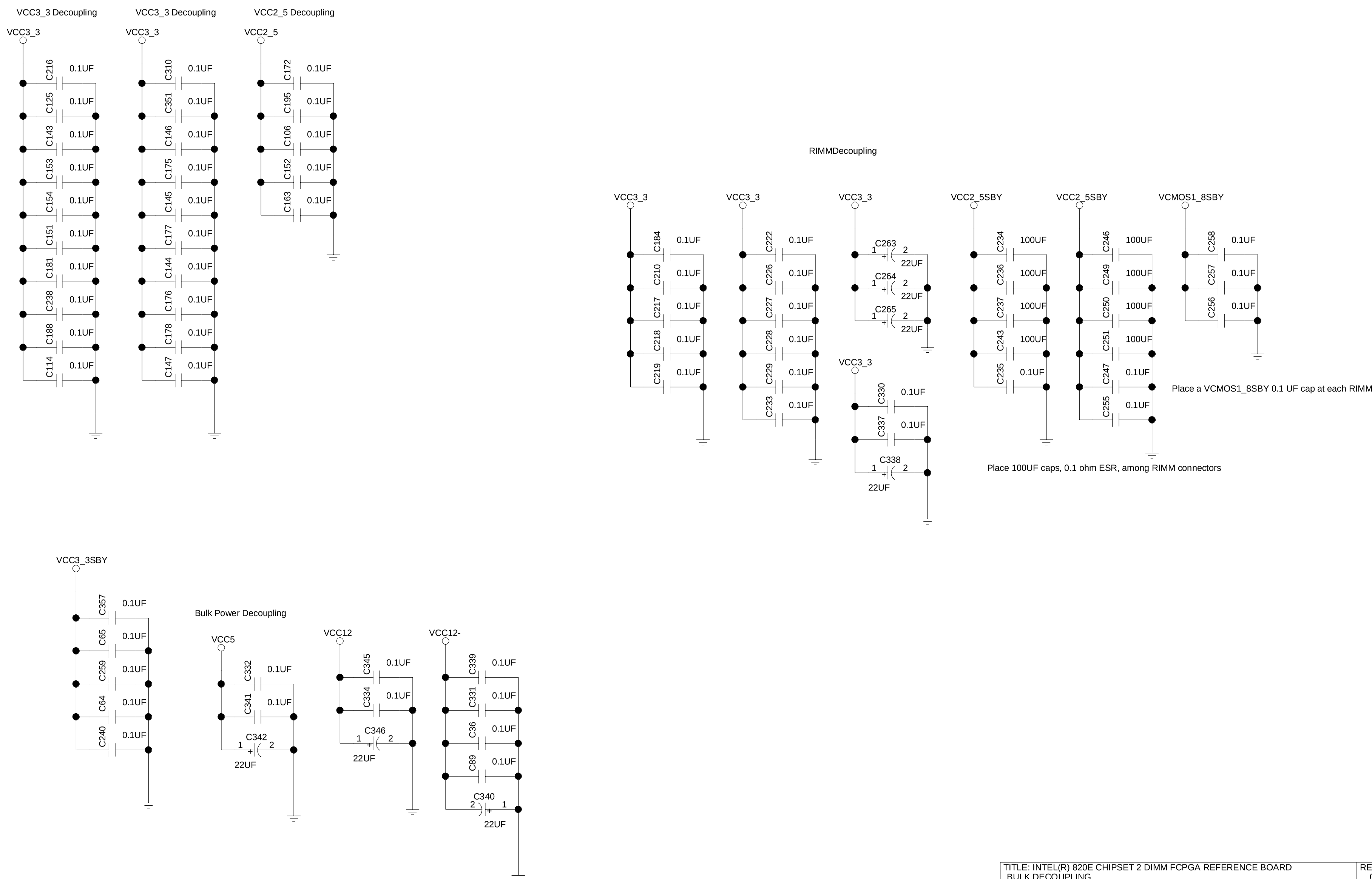


TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD
DECOUPLING

intel® PCG PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630

REV: 0.5	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED: 3-20-2000_10:14	SHEET: 40 OF 40

Decoupling

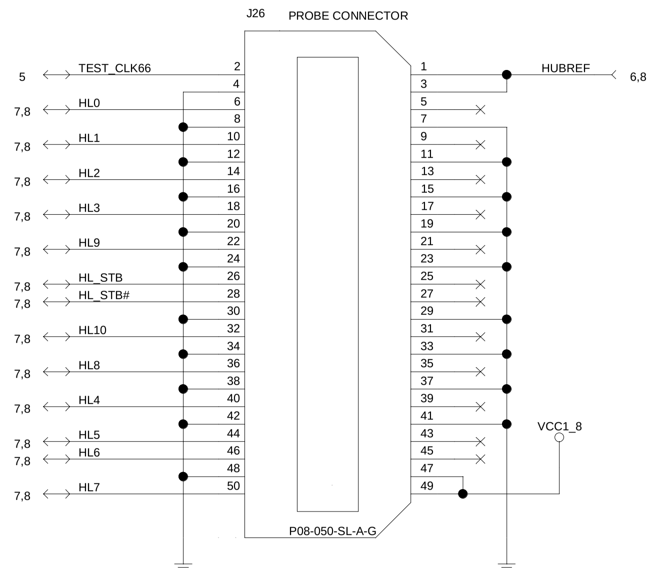


TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD BULK DECOUPLING		REV: 0.5
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED: 3-20-2000_10:14	PROJECT: Camino2 SHEET: 41 OF 40

Revision History

TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD REVISION HISTORY			REV: 0.5
intel®	PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
		LAST REVISED: 3-20-2000_10:14	SHEET: 42 OF 40

Hub Interface Connector
For debug only.



TITLE: INTEL(R) 820E CHIPSET 2 DIMM FCPGA REFERENCE BOARD		REV: 0.5
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: Camino2
	LAST REVISED:	SHEET: 43 OF 40