



LAN91C100FD REV. D

FEAST Fast Ethernet Controller with Full Duplex Capability

PRODUCT FEATURES

Data Brief

- Dual Speed CSMA/CD Engine (10 Mbps and 100 Mbps)
- Compliant with IEEE 802.3 100BASE-T Specification
- Supports 100BASE-TX, 100BASE-T4, and 10BASE-T Physical Interfaces
- 32 Bit Wide Data Path (into Packet Buffer Memory)
- Support for 32 and 16 Bit Buses
- Support for 32, 16 and 8 Bit CPU Accesses
- Synchronous, Asynchronous and Burst DMA Interface Mode Options
- 128 Kbyte External Memory
- Built-In Transparent Arbitration for Slave Sequential Access Architecture
- Flat MMU Architecture with Symmetric Transmit and Receive Structures and Queues
- MII (Media Independent Interface) Compliant MAC-PHY Interface Running at Nibble Rate
- MII Management Serial Interface
- Seven Wire Interface to 10 Mbps ENDEC
- EEPROM-Based Setup
- Full Duplex Capability

ORDER NUMBER(S):

LAN91C100-FD 208-PIN QFP PACKAGE

LAN91C100-FD-SS FOR 208-PIN QFP LEAD-FREE ROHS COMPLIANT PACKAGE

LAN91C100-FD FOR 208-PIN TQFP PACKAGE

LAN91C100-FD-ST FOR 208-PIN TQFP LEAD-FREE ROHS COMPLIANT PACKAGE



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General Description

The LAN91C100FD is designed to facilitate the implementation of first generation Fast Ethernet adapters and connectivity products. For this first generation of products, flexibility dominates over integration. The LAN91C100FD is a digital device that implements the MAC portion of the CSMA/CD protocol at 10 and 100 Mbps, and couples it with a lean and fast data and control path system architecture to ensure the CPU to packet RAM data movement does not cause a bottleneck at 100 Mbps.

Total memory size is 128 Kbytes, equivalent to a total chip storage (transmit plus receive) of 64 outstanding packets. The LAN91C100FD is software compatible with the LAN9000 family of products and can use existing LAN9000 drivers (ODI, IPX, and NDIS) in 16 and 32 bit Intel X86 based environments.

Memory management is handled using a unique MMU (Memory Management Unit) architecture and a 32-bit wide data path. This I/O mapped architecture can sustain back-to-back frame transmission and reception for superior data throughput and optimal performance. It also dynamically allocates buffer memory in an efficient buffer utilization scheme, reducing software tasks and relieving the host CPU from performing these housekeeping functions. The total memory size is 128 Kbytes (external), equivalent to a total chip storage (transmit and receive) of 64 outstanding packets.

FEAST provides a flexible slave interface for easy connectivity with industry-standard buses. The Bus Interface Unit (BIU) can handle synchronous as well as asynchronous buses, with different signals being used for each one. FEAST's bus interface supports synchronous buses like the VESA local bus, as well as burst mode DMA for EISA environments. Asynchronous bus support for ISA is supported even though ISA cannot sustain 100 Mbps traffic. Fast Ethernet could be adopted for ISA-based nodes on the basis of the aggregate traffic benefits.

Two different interfaces are supported on the network side. The first is a conventional seven wire ENDEC interface that connects to the LAN83C694 for 10BASE-T and coax 10 Mbps Ethernet networks. The second interface follows the MII (Media Independent Interface) specification draft standard, consisting of 4 bit wide data transfers at the nibble rate. This interface is applicable to 10 Mbps or 100 Mbps networks. Three of the LAN91C100FD's pins are used to interface to the two-line MII serial management protocol. Four I/O ports (one input and three output pins) are provided for LAN83C694 configuration.

The LAN91C100FD is based on the LAN91C100 FEAST, functional revision G modified to add full duplex capability. Also added is a software-controlled option to allow collisions to discard receive packets. Previously, the LAN91C100 supported a "Diagnostic Full Duplex" mode. Under this mode the transmit packet is looped internally and received by the MAC. This mode was enabled using the FDUPLEX bit in the TCR. In order to avoid confusion, the new, broader full duplex function of the LAN91C100FD is designated as Switched Full Duplex, and the TCR bit enabling it is designated as SWFDUP. When the LAN91C100FD is configured for SWFDUP, its transmit and receive paths will operate independently and some CSMA/CD functions will be disabled. When the controller is not configured for SWFDUP it will follow the CSMA/CD protocol.

Block Diagram

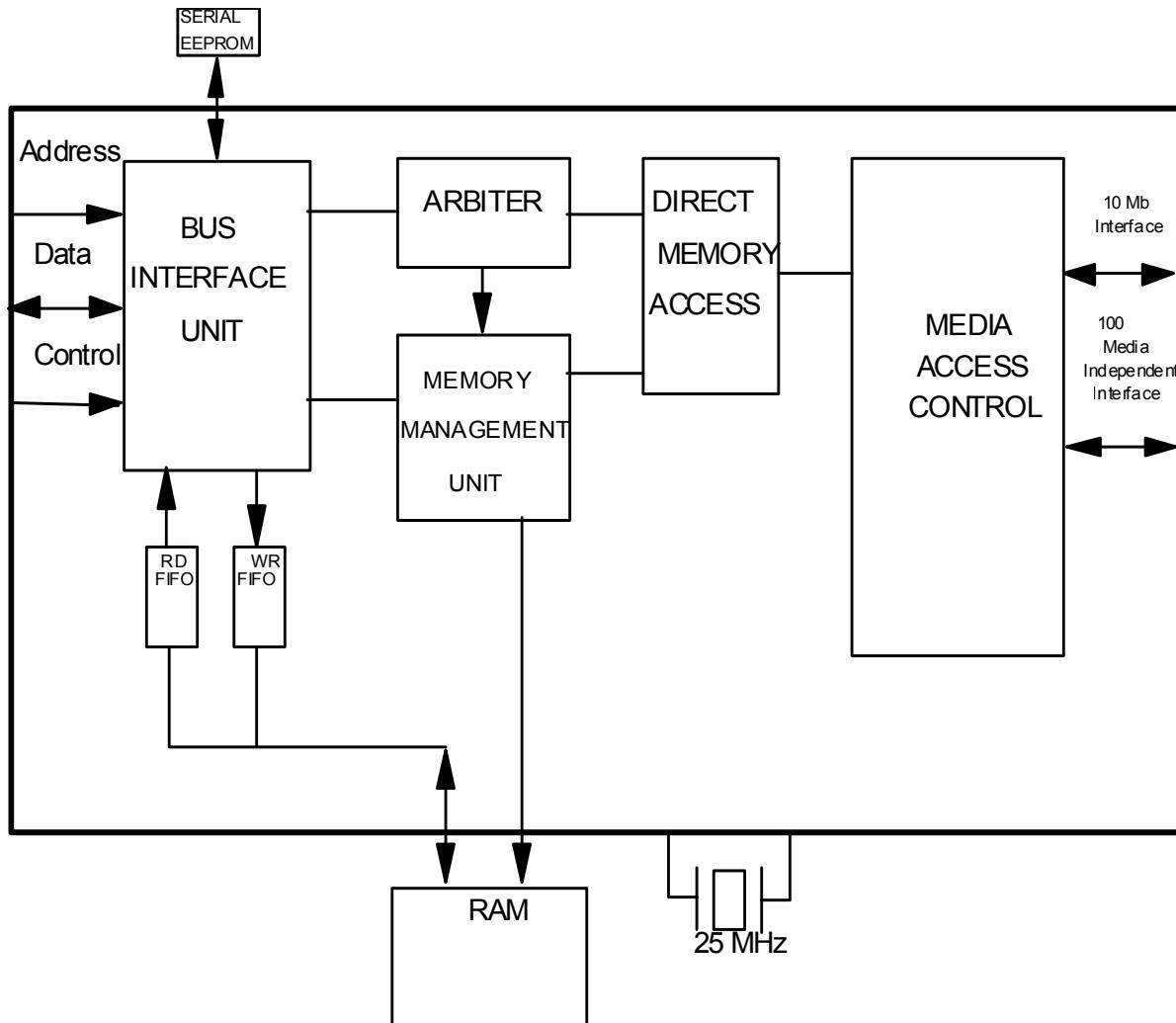


Figure 1 LAN91C100FD Block Diagram

Package Outlines

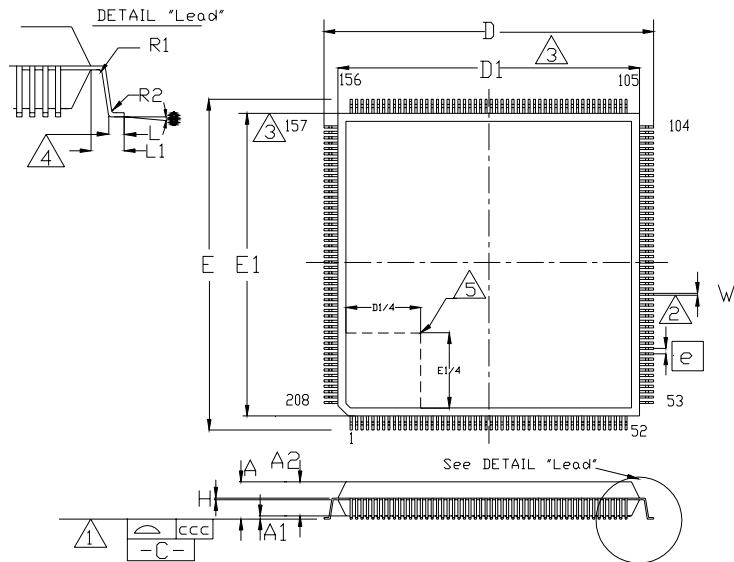


Figure 2 208 Pin QFP Package Outline

Table 1 208 Pin QFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	4.07	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	3.17	~	3.67	Body Thickness
D	30.35	~	30.85	X Span
D1	27.90	~	28.10	X Body Size
E	30.35	~	30.85	Y Span
E1	27.90	~	28.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.30	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.25	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

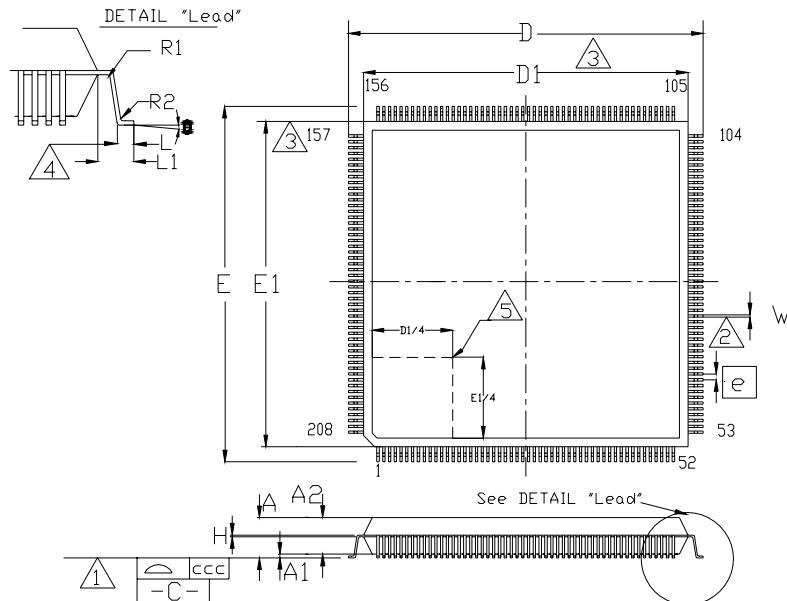


Figure 3 208 Pin TQFP Package Outline

Table 2 208 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARK
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	29.80	~	30.20	X Span
D1	27.90	~	28.10	X Body Size
E	29.80	~	30.20	Y Span
E1	27.90	~	28.10	Y body Size
H	0.09	~	0.23	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
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