AR-B1462
INDUSTRIAL GRADE
486DX/DX2/DX4 CPU CARD
User's Guide

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0.PREFACE

0.1 COPYRIGHT NOTICE AND DISCLAIMER

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0.2 WELCOME TO THE AR-B1462 CPU BOARD

This guide introduces the Acrosser AR-B1462 CPU board.

Use the information describes this card's functions, features, and how to start, set up and operate your AR-B1462. You also could find general system information here.

0.3 BEFORE YOU USE THIS GUIDE

If you have not already installed this AR-B1462, refer to the Chapter 3, "Setting Up the System" in this guide. Check the packing list, make sure the accessories in the package.

The AR-B1462 diskette provides the newest information about the card**. Please refer to the README.DOC file of the enclosed utility diskette**. It contains the modification and hardware & software information, and adding the description or modification of product function after manual published.

0.4 RETURNING YOUR BOARD FOR SERVICE

If your board requires servicing, contact the dealer from whom you purchased the product for service information. If you need to ship your board to us for service, be sure it is packed in a protective carton. We recommend that you keep the original shipping container for this purpose.

You can help assure efficient servicing of your product by following these guidelines:

1. Include your name, address, telephone and facsimile number where you may be reached during the day.
2. A description of the system configuration and/or software at the time is malfunction.
3. A brief description is in the symptoms.

0.5 TECHNICAL SUPPORT AND USER COMMENTS

User's comments are always welcome as they assist us in improving the usefulness of our products and the understanding of our publications. They form a very important part of the input used for product enhancement and revision.

We may use and distribute any of the information you supply in any way we believe appropriate without incurring any obligation. You may, of course, continue to use the information you supply.

If you have suggestions for improving particular sections or if you find any errors, please indicate the manual title and book number.

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0.6 ORGANIZATION

This information for users covers the following topics (see the Table of Contents for a detailed listing):

- Chapter 1, "Overview", provides an overview of the system features and packing list.
- Chapter 2, "System Controller" describes the major structure.
- Chapter 3, "Setting Up the System", describes how to adjust the jumper, and the connectors setting.
- Chapter 4, "CRT/LCD Flat Panel Display", describes the configuration and installation procedure using the LCD and CRT display.
- Chapter 5, "Installation", describes setup procedures including information on the utility diskette.
- Chapter 6, "Solid State Disk", describes the various type SSDs' installation steps.
- Chapter 7, "BIOS Console", providing the BIOS options setting.
- Chapter 8, Specifications & SSD Types Supported
- Chapter 9, Placement & Dimensions
- Chapter 10, Programming RS-485 & Index

0.7 STATIC ELECTRICITY PRECAUTIONS

Before removing the board from its anti-static bag, read this section about static electricity precautions.
Static electricity is a constant danger to computer systems. The charge that can build up in your body may be more than sufficient to damage integrated circuits on any PC board. It is, therefore, important to observe basic precautions whenever you use or handle computer components. Although areas with humid climates are much less prone to static build-up, it is always best to safeguard against accidents may result in expensive repairs. The following measures should generally be sufficient to protect your equipment from static discharge:

- Touch a grounded metal object to discharge the static electricity in your body (or ideally, wear a grounded wrist strap).
- When unpacking and handling the board or other system component, place all materials on an antic static surface.
- Be careful not to touch the components on the board, especially the "golden finger" connectors on the bottom of every board.

1. OVERVIEW

This chapter provides an overview of your system features and capabilities. The following topics are covered:

- Introduction
- Packing List
- Features

1.1 INTRODUCTION

The AR-B1462 is a disk size industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. The total on-board memory for the AR-B1462 can be configured from 1MB to 128MB by using all 72-pin type DRAM SIMM devices.

The 8 layers PCB CPU card is equipped with a IDE HDD interface, a floppy disk drive adapter, 1 parallel port, 4 serial ports and a watchdog timer. Its dimensions are as compact as 146mmX203mm. It highly condensed features make it an ideal cost/performance solution for high-end commercial and industrial applications where CPU speeding and mean time between failure is critical.

The AR-B1462 provides 2 bus interfaces, ISA bus and PC/104 compatible expansion bus. Based on the PC/104 expansion bus, you could easy install thousands of PC/104 module from hundreds venders around the world. You could also directly connect the power supply to the AR-B1462 on-board power connector in standalone applications.

A watchdog timer has a software programmable time-out interval, is also provided on this CPU card. It ensures that the system does not hang-up if a program can not execute normally.

A super I/O chip (SMC37C669) is embedded in the AR-B1462 card. It combines functions of a floppy disk drive adapter, a hard disk drive (IDE) adapter, four serial (with 16C550 UART) adapters and 1 parallel adapter. The I/O port configurations can be done by set the BIOS setup program.

As an UART, the chip supports serial to parallel conversion on data characters received from a peripheral device or a MODEM, and parallel to serial conversion on data character received from the CPU. The UART includes a programmable baud rate generator, complete MODEM control capability and a processor interrupt system. As a parallel port, the SMC37C669 provides the user with a fully bi-directional parallel centronics-type printer interface.

The special device is the AR-B1462 provides one audio connector, the sound system is built-in 16bit PnP sound blaster with DOS and Windows drivers. In the same time the AR-B1462 provides network connectors that are 10M bps NE2000 compatible. We designed the connectors for easily setup.

The super VGA controller supports CRT color monitor, STN, Dual-Scan, TFT, monochrome and colored panels. It can be connected to create a compact video solution for the industrial environment. And provides the touch screen header on the serial port 4 for multiple function.

Note: Just the AR-B1462A supported the audio function and supported 2MB on-board VRAM. The AR-B1462 only supported 1MB on-board VRAM.

1.2 PACKING LIST

The accessories are included with the system. Before you begin installing your AR-B1462 board, take a moment to make sure that the following items have been included inside the AR-B1462 package.

- The quick setup manual
- 1 AR-B1462 CPU card
- 1 Hard disk drive interface cable
- 1 Floppy disk drive interface cable
- 1 Parallel port interface cable
- 1 AUI cable
- 1 PS/2 mouse cable
- 1 Keyboard adapter
- 1 RJ-45 network cable
- 1 20-pin RS-485/RS-422 adapter cable
- 1 10-pin to DB-15 VGA
- 4 phone-jack to DB-9 adapter
- 4 Software utility diskettes

If use the AR-B1462A CPU card, the card added the audio function the accessories also added as follows.

- 1 AR-B9425 card
- 1 audio adapter cable

1.3 FEATURES

The system provides a number of special features that enhance its reliability, ensure its availability, and improve its expansion capabilities, as well as its hardware structure.

- All-In-One designed 486DX/DX2/DX4 CPU card.
- Supports 25 to 133 MHz 3.3V/3.45V/5V CPU with voltage regulator.
- Supports ISA bus and PC/104 bus.
- Supports 512KB cache on board.
- Supports two 72-pin DRAM SIMMs up to 128MB DRAM on board.
- Supports D.O.C. up to 72MB.
- Legal AMI BIOS.
- IDE hard disk drive interface.
- Floppy disk drive interface.
- Bi-direction parallel interface.
- 4 serial ports with 16C550 UART.
- Programmable watchdog timer.
- Build-in 16bit PnP sound blaster with DOS and Windows drivers
- Supports 10M bps NE2000 compatible chips.
- On-board built-in buzzer.
- 8 layers PCB.

2. SYSTEM CONTROLLER

This chapter describes the major structure of the AR-B1462 CPU board. The following topics are covered:

- DMA Controller
- Keyboard Controller
- Interrupt Controller
- Real-Time Clock and Non-Volatile RAM
- Timer
- Serial Port
- Parallel Port

2.1 DMA CONTROLLER

The equivalent of two 8237A DMA controllers are implemented in the AR-B1462 board. Each controller is a four-channel DMA device that will generate the memory addresses and control signals necessary to transfer information directly between a peripheral device and memory. This allows high speeding information transfer with less CPU intervention. The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 channel 0 provides the cascade interconnection between the two DMA devices, thereby maintaining IBM PC/AT compatibility.

Following is the system information of DMA channels:

DMA Controller 1	DMA Controller 2
Channel 0: Spare	Channel 4: Cascade for controller 1
Channel 1: IBM SDLC	Channel 5: Spare
Channel 2: Diskette adapter	Channel 6: Spare
Channel 3: Spare	Channel 7: Spare

Table 2-1 DMA Channel Controller

2.2 KEYBOARD CONTROLLER

The 8042 processor is programmed to support the keyboard serial interface. The keyboard controller receives serial data from the keyboard, checks its parity, translates scan codes, and presents it to the system as a byte data in its output buffer. The controller can interrupt the system when data is placed in its output buffer, or wait for the system to poll its status register to determine when data is available.

Data can be written to the keyboard by writing data to the output buffer of the keyboard controller.

Each byte of data is sent to the keyboard controller in series with an odd parity bit automatically inserted. The keyboard controller is required to acknowledge all data transmissions. Therefore, another byte of data will not be sent to keyboard controller until acknowledgment is received for the previous byte sent. The “output buffer full” interruption may be used for both send and receive routines.

2.3 INTERRUPT CONTROLLER

The equivalent of two 8259 Programmable Interrupt Controllers (PIC) are included on the AR-B1462 board. They accept requests from peripherals, resolve priorities on pending interrupts in service, issue interrupt requests to the CPU, and provide vectors which are used as acceptance indices by the CPU to determine which interrupt service routine to execute.

Following is the system information of interrupt levels:

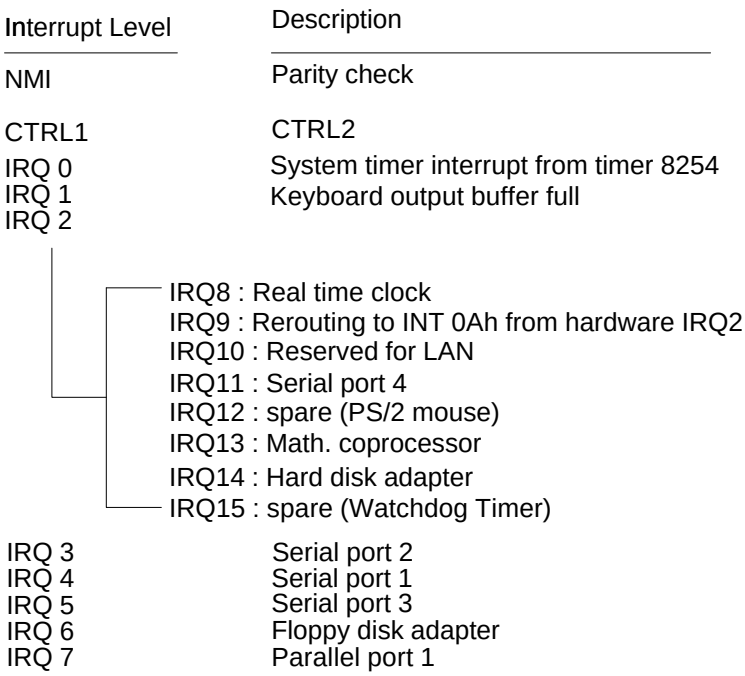


Figure 2-1 Interrupt Controller

2.3.1 I/O Port Address Map

Hex Range	Device
000-01F	DMA controller 1
020-021	Interrupt controller 1
022-023	System -- ALI M1489/M1487 Video – C & T F65550 (PCI bus) I/O – Two SMC FDC37C669 (ISA bus) Audio – ESS ES1869S
040-04F	Timer 1
050-05F	Timer 2
060-06F	8042 keyboard/controller
070-071	Real-time clock (RTC), non-maskable interrupt (NMI)
080-09F	DMA page registers
0A0-0A1	Interrupt controller 2
0C0-0DF	DMA controller 2
0F0	Clear Math Co-processor
0F1	Reset Math Co-processor
0F8-0FF	Math Co-processor
170-178	Fixed disk 1
1F0-1F8	Fixed disk 0
201	Game port
208-20A	EMS register 0
218-21A	EMS register 1
278-27F	Parallel printer port 2 (LPT 2)
2E8-2EF	Serial port 4 (COM 4)
2F8-2FF	Serial port 2 (COM 2)
300-31F	Prototype card/streaming type adapter
320-33F	LAN adapter
378-37F	Parallel printer port 1 (LPT 1)
380-38F	SDLC, bisynchronous
3A0-3AF	Bisynchronous
3B0-3BF	Monochrome display and printer port 3 (LPT 3)
3C0-3CF	EGA/VGA adapter
3D0-3DF	Color/graphics monitor adapter
3E8-3EF	Serial port 3 (COM 3)
3F0-3F7	Diskette controller
3F8-3FF	Serial port 1 (COM 1)

Table 2-2 I/O Port Address Map

2.3.2 I/O Channel Pin Assignment (Bus1)

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
A1	-IOCHCK	Input	B1	GND	Ground
A2	SD7	Input/Output	B2	RSTDRV	Output
A3	SD6	Input/Output	B3	+5V	Power
A4	SD5	Input/Output	B4	IRQ9	Input
A5	SD4	Input/Output	B5	-5V	Power
A6	SD3	Input/Output	B6	DRQ2	Input
A7	SD2	Input/Output	B7	-12V	Power
A8	SD1	Input/Output	B8	-ZWS	Input
A9	SD0	Input/Output	B9	+12V	Power
A10	-IOCHRDY	Input	B10	GND	Ground
A11	AEN	Output	B11	-SMEMW	Output
A12	SA19	Input/Output	B12	-SMEMR	Output
A13	SA18	Input/Output	B13	-IOW	Input/Output

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
A14	SA17	Input/Output	B14	-IOR	Input/Output
A15	SA16	Input/Output	B15	-DACK3	Output
A16	SA15	Input/Output	B16	DRQ3	Input
A17	SA14	Input/Output	B17	-DACK1	Output
A18	SA13	Input/Output	B18	DRQ1	Input
A19	SA12	Input/Output	B19	-REFRESH	Input/Output
A20	SA11	Input/Output	B20	BUSCLK	Output
A21	SA10	Input/Output	B21	IRQ7	Input
A22	SA9	Input/Output	B22	IRQ6	Input
A23	SA8	Input/Output	B23	IRQ5	Input
A24	SA7	Input/Output	B24	IRQ4	Input
A25	SA6	Input/Output	B25	IRQ3	Input
A26	SA5	Input/Output	B26	-DACK2	Output
A27	SA4	Input/Output	B27	TC	Output
A28	SA3	Input/Output	B28	BALE	Output
A29	SA2	Input/Output	B29	+5V	Power
A30	SA1	Input/Output	B30	OSC	Output
A31	SA0	Input/Output	B31	GND	Ground

Table 2-3 I/O Channel Pin Assignments

I/O Pin	Signal Name	Input/Output	I/O Pin	Signal Name	Input/Output
C1	-SBHE	Input/Output	D1	-MEMCS16	Input
C2	LA23	Input/Output	D2	-IOCS16	Input
C3	LA22	Input/Output	D3	IRQ10	Input
C4	LA21	Input/Output	D4	IRQ11	Input
C5	LA20	Input/Output	D5	IRQ12	Input
C6	LA19	Input/Output	D6	IRQ15	Input
C7	LA18	Input/Output	D7	IRQ14	Input
C8	LA17	Input/Output	D8	-DACK0	Output
C9	-MRD16	Input/Output	D9	DRQ0	Input
C10	-MWR16	Input/Output	D10	-DACK5	Output
C11	SD8	Input/Output	D11	DRQ5	Input
C12	SD9	Input/Output	D12	-DACK6	Output
C13	SD10	Input/Output	D13	DRQ6	Input
C14	SD11	Input/Output	D14	-DACK7	Output
C15	SD12	Input/Output	D15	DRQ7	Input
C16	SD13	Input/Output	D16	+5V	Power
C17	SD14	Input/Output	D17	-MASTER	Input
C18	SD15	Input/Output	D18	GND	Ground

Table 2-4 I/O Channel Pin Assignments

2.4 REAL-TIME CLOCK AND NON-VOLATILE RAM

The AR-B1462 contains a real-time clock compartment that maintains the date and time in addition to storing configuration information about the computer system. It contains 14 bytes of clock and control registers and 114 bytes of general purpose RAM. Because of the use of CMOS technology, it consumes very little power and can be maintained for long period of time using an internal Lithium battery. The contents of each byte in the CMOS RAM are listed as follows:

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic status byte
0F	Shutdown status byte
10	Diskette drive type byte, drive A and B
11	Fixed disk type byte, drive C
12	Fixed disk type byte, drive D
13	Reserved
14	Equipment byte
15	Low base memory byte
16	High base memory byte
17	Low expansion memory byte
18	High expansion memory byte
19-2D	Reserved
2E-2F	2-byte CMOS checksum
30	Low actual expansion memory byte
31	High actual expansion memory byte
32	Date century byte
33	Information flags (set during power on)
34-7F	Reserved for system BIOS

Table 2-5 Real-Time Clock & Non-Volatile RAM

2.5 TIMER

The AR-B1462 provides three programmable timers, each with a timing frequency of 1.19 MHz.

Timer 0 The output of this timer is tied to interrupt request 0. (IRQ 0)

Timer 1 This timer is used to trigger memory refresh cycles.

Timer 2 This timer provides the speaker tone.
Application programs can load different counts into this timer to generate various sound frequencies.

2.6 SERIAL PORT

The ACEs (Asynchronous Communication Elements ACE1 to ACE4) are used to convert parallel data to a serial format on the transmit side and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The ACEs are capable of handling divisors of 1 to 65535, and produce a 16x clock for driving the internal transmitter logic.

Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE a completed MODEM control capability, and a processor interrupt system that may be software tailored to the computing time required handle the communications link.

The following table is summary of each ACE accessible register

DLAB	Port Address	Register
0	base + 0	Receiver buffer (read)
		Transmitter holding register (write)
0	base + 1	Interrupt enable
X	base + 2	Interrupt identification (read only)
X	base + 3	Line control
X	base + 4	MODEM control
X	base + 5	Line status
X	base + 6	MODEM status
X	base + 7	Scratched register
1	base + 0	Divisor latch (least significant byte)
1	base + 1	Divisor latch (most significant byte)

Table 2-6 ACE Accessible Registers

(1) Receiver Buffer Register (RBR)

Bit 0-7: Received data byte (Read Only)

(2) Transmitter Holding Register (THR)

Bit 0-7: Transmitter holding data byte (Write Only)

(3) Interrupt Enable Register (IER)

Bit 0: Enable Received Data Available Interrupt (ERBFI)
Bit 1: Enable Transmitter Holding Empty Interrupt (ETBEI)
Bit 2: Enable Receiver Line Status Interrupt (ELSI)
Bit 3: Enable MODEM Status Interrupt (EDSSI)
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(4) Interrupt Identification Register (IIR)

Bit 0: "0" if Interrupt Pending
Bit 1: Interrupt ID Bit 0
Bit 2: Interrupt ID Bit 1
Bit 3: Must be 0
Bit 4: Must be 0
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(5) Line Control Register (LCR)

Bit 0: Word Length Select Bit 0 (WLS0)
Bit 1: Word Length Select Bit 1 (WLS1)

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: Number of Stop Bit (STB)
Bit 3: Parity Enable (PEN)
Bit 4: Even Parity Select (EPS)
Bit 5: Stick Parity
Bit 6: Set Break
Bit 7: Divisor Latch Access Bit (DLAB)

(6) MODEM Control Register (MCR)

Bit 0: Data Terminal Ready (DTR)
Bit 1: Request to Send (RTS)
Bit 2: Out 1 (OUT 1)
Bit 3: Out 2 (OUT 2)
Bit 4: Loop
Bit 5: Must be 0
Bit 6: Must be 0
Bit 7: Must be 0

(7) Line Status Register (LSR)

Bit 0: Data Ready (DR)
Bit 1: Overrun Error (OR)
Bit 2: Parity Error (PE)
Bit 3: Framing Error (FE)
Bit 4: Break Interrupt (BI)
Bit 5: Transmitter Holding Register Empty (THRE)
Bit 6: Transmitter Shift Register Empty (TSRE)
Bit 7: Must be 0

(8) MODEM Status Register (MSR)

Bit 0: Delta Clear to Send (DCTS)
Bit 1: Delta Data Set Ready (DDSR)
Bit 2: Training Edge Ring Indicator (TERI)
Bit 3: Delta Receive Line Signal Detect (DSLSD)
Bit 4: Clear to Send (CTS)
Bit 5: Data Set Ready (DSR)
Bit 6: Ring Indicator (RI)
Bit 7: Received Line Signal Detect (RSLD)

(9) Divisor Latch (LS, MS)

	LS	MS
Bit 0:	Bit 0	Bit 8
Bit 1:	Bit 1	Bit 9
Bit 2:	Bit 2	Bit 10
Bit 3:	Bit 3	Bit 11
Bit 4:	Bit 4	Bit 12
Bit 5:	Bit 5	Bit 13
Bit 6:	Bit 6	Bit 14
Bit 7:	Bit 7	Bit 15

Desired Baud Rate	Divisor Used to Generate 16x Clock
300	384
600	192
1200	96
1800	64
2400	48
3600	32
4800	24
9600	12
14400	8
19200	6
28800	4
38400	3
57600	2
115200	1

Table 2-7 Serial Port Divisor Latch

2.7 PARALLEL PORT

(1) Register Address

Port Address	Read/Write	Register
base + 0	Write	Output data
base + 0	Read	Input data
base + 1	Read	Printer status buffer
base + 2	Write	Printer control latch

Table 2-8 Registers' Address

(2) Printer Interface Logic

The parallel portion of the SMC37C669 makes the attachment of various devices that accept eight bits of parallel data at standard TTL level.

(3) Data Swapper

The system microprocessor can read the contents of the printer's Data Latch through the Data Swapper by reading the Data Swapper address.

(4) Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the Printer Status Buffer. The bit definitions are described as follows:

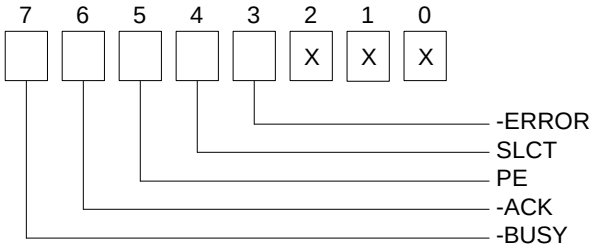


Figure 2-2 Printer Status Buffer

NOTE: X presents not used.

Bit 7: This signal may become active during data entry, when the printer is off-line during printing, or when the print head is changing position or in an error state. When Bit 7 is active, the printer is busy and can not accept data.

Bit 6: This bit represents the current state of the printer's ACK signal. A0 means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before receiving a BUSY message stops.

Bit 5: A1 means the printer has detected the end of the paper.

Bit 4: A1 means the printer is selected.

Bit 3: A0 means the printer has encountered an error condition.

(5) Printer Control Latch & Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the address of printer control swapper. Bit definitions are as follows:

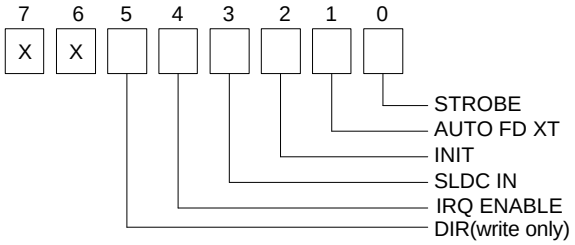


Figure 2-3 Bit' s Definition

NOTE: X presents not used.

Bit 5: Direction control bit. When logic 1, the output buffers in the parallel port are disabled allowing data driven from external sources to be read; when logic 0, they work as a printer port. This bit is write only.

Bit 4: A1 in this position allows an interrupt to occur when ACK changes from low state to high state.

Bit 3: A1 in this bit position selects the printer.

Bit 2: A0 starts the printer (50 microseconds pulse, minimum).

Bit 1: A1 causes the printer to line-feed after a line is printed.

Bit 0: A0.5 microsecond minimum highly active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

3. SETTING UP THE SYSTEM

This section describes pin assignments for system' s external connectors and the jumpers setting.

- Overview
- System Setting
- Ethernet Controller

3.1 OVERVIEW

The AR-B1462 is a half size industrial grade CPU card that has been designed to withstand continuous operation in harsh environments. This section provides hardware's jumpers setting, the connectors' locations, and the pin assignment.

Note: Just the AR-B1462A supported the audio function and supported 2MB on-board VRAM. The AR-B1462 only supported 1MB on-board VRAM.

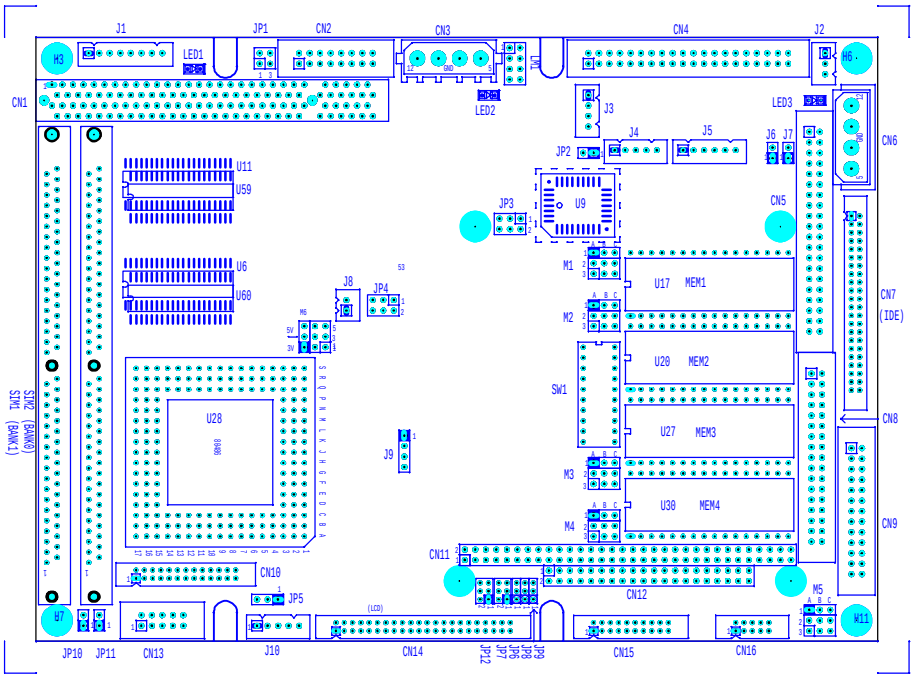


Figure 3-1 AR-B1462 Jumpers & Connectors Placement

3.2 SYSTEM SETTING

Jumper pins allow you to set specific system parameters. Set them by changing the pin location of jumper blocks. (A jumper block is a small plastic-encased conductor [shorting plug] that slips over the pins.) To change a jumper setting, remove the jumper from its current location with your fingers or small needle-nosed pliers. Place the jumper over the two pins designated for the desired setting. Press the jumper evenly onto the pins. Be careful not to bend the pins.

We will show the locations of the AR-B1462 jumper pins, and the factory-default setting.

CAUTION: Do not touch any electronic component unless you are safely grounded. Wear a grounded wrist strap or touch an exposed metal part of the system unit chassis. The static discharges from your fingers can permanently damage electronic components.

3.2.1 FDD Port Connector (CN8)

The AR-B1462 provides a 34-pin header type connector for supporting up to two floppy disk drives.

To enable or disable the floppy disk controller, please use the BIOS Setup program.

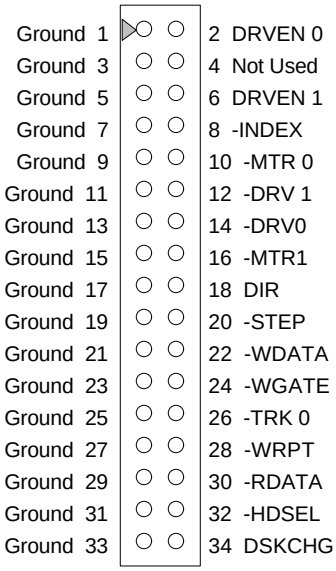


Figure 3-2 CN8: FDD Port connector

3.2.2 Hard Disk (IDE) Connector

(1) 40-Pin Hard Disk (IDE) Connector (CN5)

A 40-pin header type connector (CN5) is provided to interface with up to two embedded hard disk drives (IDE AT bus). This interface, through a 40-pin cable, allows the user to connect up to two drives in a "daisy chain" fashion. To enable or disable the hard disk controller, please use the BIOS Setup program. The following table illustrates the pin assignments of the hard disk drive's 40-pin connector.

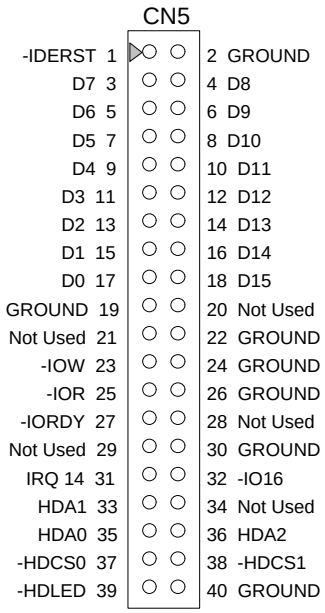


Figure 3-3 CN5: Hard Disk (IDE) Connector

Caution: When the CN5 is used to connect the hard disk drive, if you find it can not make partition, please change the hard disk cable to below 35cm in length.

(2) 44-Pin Hard Disk (IDE) Connector (CN7)

AR-B1462 also provides IDE interface 44-pin connector to connect with the hard disk device.

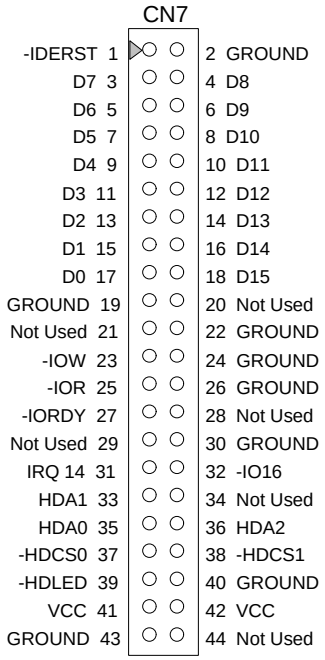


Figure 3-4 CN7: Hard Disk (IDE) Connector

3.2.3 Parallel Port Connector (CN9)

To use the parallel port, an adapter cable has to be connected to the CN9 (26-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1462 package. The connector for the parallel port is a 25 pin D-type female connector.

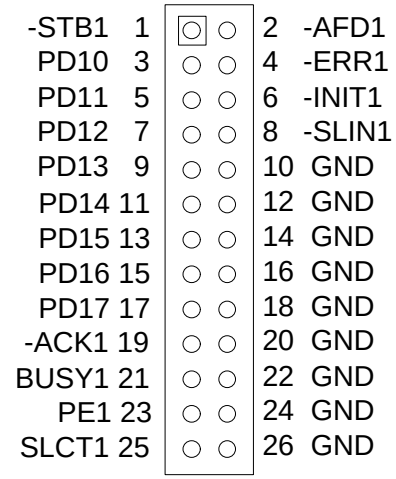


Figure 3-5 CN9: Parallel Port Connector

CN9	DB-25	Signal	CN9	DB-25	Signal
1	1	-Strobe	2	14	-Auto Form Feed
3	2	Data 0	4	15	-Error
5	3	Data 1	6	16	-Initialize
7	4	Data 2	8	17	-Printer Select In
9	5	Data 3	10	18	Ground
11	6	Data 4	12	19	Ground
13	7	Data 5	14	20	Ground
15	8	Data 6	16	21	Ground
17	9	Data 7	18	22	Ground
19	10	-Acknowledge	20	23	Ground
21	11	Busy	22	24	Ground
23	12	Paper	24	25	Ground
25	13	Printer Select	26	--	No Used

Table 3-1 Parallel Port Pin Assignment

3.2.4 PC/104 Connector

(1) 64 Pin PC/104 Connector Bus A & B (CN11)

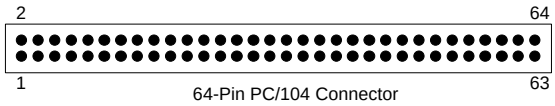


Figure 3-6 CN11: 64 Pin PC/104 Connector Bus A & B

CN11

		1	2		
-IOCHCK ---	A1	●	●	B1	--- GND
SD7 ---	A2	●	●	B2	--- RSTDRV
SD6 ---	A3	●	●	B3	--- +5 VDC
SD5 ---	A4	●	●	B4	--- IRQ9
SD4 ---	A5	●	●	B5	--- -5 VDC
SD3 ---	A6	●	●	B6	--- DRQ2
SD2 ---	A7	●	●	B7	--- -12 VDC
SD1 ---	A8	●	●	B8	--- -ZWS
SD0 ---	A9	●	●	B9	--- +12 VDC
-IOCHRDY---	A10	●	●	B10	--- GND
AEN ---	A11	●	●	B11	--- -SMEMW
SA19 ---	A12	●	●	B12	--- -SMEMR
SA18 ---	A13	●	●	B13	--- -IOW
SA17 ---	A14	●	●	B14	--- -IOR
SA16 ---	A15	●	●	B15	--- -DACK3
SA15 ---	A16	●	●	B16	--- DRQ3
SA14 ---	A17	●	●	B17	--- -DACK1
SA13 ---	A18	●	●	B18	--- DRQ1
SA12 ---	A19	●	●	B19	--- -REFRESH
SA11 ---	A20	●	●	B20	--- BUSCLK
SA10 ---	A21	●	●	B21	--- IRQ7
SA9 ---	A22	●	●	B22	--- IRQ6
SA8 ---	A23	●	●	B23	--- IRQ5
SA7 ---	A24	●	●	B24	--- IRQ4
SA6 ---	A25	●	●	B25	--- IRQ3
SA5 ---	A26	●	●	B26	--- -DACK2
SA4 ---	A27	●	●	B27	--- TC
SA3 ---	A28	●	●	B28	--- BALE
SA2 ---	A29	●	●	B29	--- +5 VDC
SA1 ---	A30	●	●	B30	--- OSC
SA0 ---	A31	●	●	B31	--- GND
GND ---	A32	●	●	B32	--- GND

Figure 3-7 CN11: 64-Pin PC/104 Connector Bus A & B

(2) 40 Pin PC/104 Connector Bus C & D (CN12)

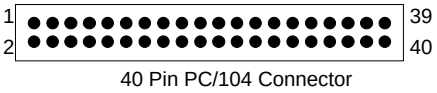


Figure 3-8 CN12: 40 Pin PC/104 Connector Bus C & D

CN12

		1	2		
GND ---	C1	●	●	D1	--- GND
-SBHE ---	C2	●	●	D2	--- -MEM16
LA23 ---	C3	●	●	D3	--- -IOCS16
LA22 ---	C4	●	●	D4	--- IRQ10
LA21 ---	C5	●	●	D5	--- IRQ11
LA20 ---	C6	●	●	D6	--- IRQ12
LA19 ---	C7	●	●	D7	--- IRQ15
LA18 ---	C8	●	●	D8	--- IRQ14
LA17 ---	C9	●	●	D9	--- -DACK0
-MRD16 ---	C10	●	●	D10	--- DRQ0
-MWR16 ---	C11	●	●	D11	--- -DACK5
SD8 ---	C12	●	●	D12	--- DRQ5
SD9 ---	C13	●	●	D13	--- -DACK6
SD10 ---	C14	●	●	D14	--- DRQ6
SD11 ---	C15	●	●	D15	--- -DACK7
SD12 ---	C16	●	●	D16	--- DRQ7
SD13 ---	C17	●	●	D17	--- +5 VDC
SD14 ---	C18	●	●	D18	--- -MASTER
SD15 ---	C19	●	●	D19	--- GND
Not Used ---	C20	●	●	D20	--- GND

Figure 3-9 CN12: 40-Pin PC/104 Connector Bus C & D

(3) I/O Channel Signal Description

Name	Description
BUSCLK [Output]	The BUSCLK signal of the I/O channel is asynchronous to the CPU clock.
RSTDRV [Output]	This signal goes high during power-up, low line-voltage or hardware reset
SA0 - SA19 [Input / Output]	The System Address lines run from bit 0 to 19. They are latched onto the falling edge of "BALE"
LA17 - LA23 [Input/Output]	The Unlatched Address line run from bit 17 to 23
SD0 - SD15 [Input/Output]	System Data bit 0 to 15
BALE [Output]	The Buffered Address Latch Enable is used to latch SA0 - SA19 onto the falling edge. This signal is forced high during DMA cycles
-IOCHCK [Input]	The I/O Channel Check is an active low signal which indicates that a parity error exist on the I/O board
IOCHRDY [Input, Open collector]	This signal lengthens the I/O, or memory read/write cycle, and should be held low with a valid address
IRQ 3-7, 9-12, 14, 15 [Input]	The Interrupt Request signal indicates I/O service request attention. They are prioritized in the following sequence : (Highest) IRQ 9, 10, 11, 12, 13, 15, 3, 4, 5, 6, 7 (Lowest)
-IOR [Input/Output]	The I/O Read signal is an active low signal which instructs the I/O device to drive its data onto the data bus
-IOW [Input/Output]	The I/O write signal is an active low signal which instructs the I/O device to read data from the data bus
-SMEMR [Output]	The System Memory Read is low while any of the low 1 mega bytes of memory are being used
-MEMR [Input/Output]	The Memory Read signal is low while any memory location is being read
-SMEMW [Output]	The System Memory Write is low while any of the low 1 mega bytes of memory is being written
-MEMW [Input/Output]	The Memory Write signal is low while any memory location is being written
DRQ 0-3, 5-7 [Input]	DMA Request channels 0 to 3 are for 8-bit data transfers. DMA Request channels 5 to 7 are for 16-bit data transfers. DMA request should be held high until the corresponding DMA has been completed. DMA request priority is in the following sequence:(Highest) DRQ 0, 1, 2, 3, 5, 6, 7 (Lowest)
-DACK 0-3, 5-7 [Output]	The DMA Acknowledges 0 to 3, 5 to 7 are the corresponding acknowledge signals for DRQ 0 to 3 and 5 to 7
AEN [output]	The DMA Address Enable is high when the DMA controller is driving the address bus. It is low when the CPU is driving the address bus
-REFRESH [Input/Output]	This signal is used to indicate a memory refresh cycle and can be driven by the microprocessor on the I/O channel
TC [Output]	Terminal Count provides a pulse when the terminal count for any DMA channel is reached
SBHE [Input/Output]	The System Bus High Enable indicates the high byte SD8 - SD15 on the data bus

Name	Description
-MASTER [Input]	The MASTER is the signal from the I/O processor which gains control as the master and should be held low for a maximum of 15 microseconds or system memory may be lost due to the lack of refresh
-MEMCS16 [Input, Open collector]	The Memory Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data memory operation
-IOCS16 [Input, Open collector]	The I/O Chip Select 16 indicates that the present data transfer is a 1-wait state, 16-bit data I/O operation
OSC [Output]	The Oscillator is a 14.31818 MHz signal used for the color graphic card
-ZWS [Input, Open collector]	The Zero Wait State indicates to the microprocessor that the present bus cycle can be completed without inserting additional wait cycle

Table 3-2 I/O Channel Signal's Description

3.2.5 LED Header (LM1)

The AR-B1462 provides one module for various LEDs' headers.

Figure 3-10 LM1: LED Header

3.2.6 Serial Port

(1) RS-422/RS-485 Select

SW1-9 & SW1-10 selects COM B port, and adjusts the CN15 connector is RS-485 or RS-232C. M5 selects COM A port for using DB2 for RS-232C or connects External RS-485.

(A) COM-A RS-485/RS-422 Adapter Select (M5)

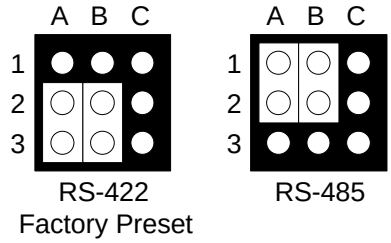


Figure 3-11 M5: COM-A RS-485/RS-422 Adapter Select

(B) Terminal Select (M5)

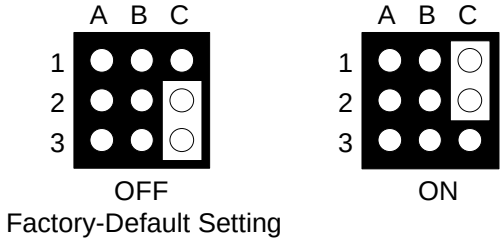
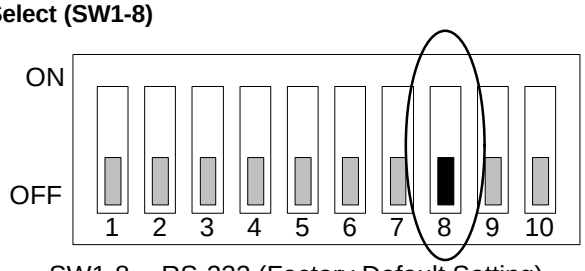
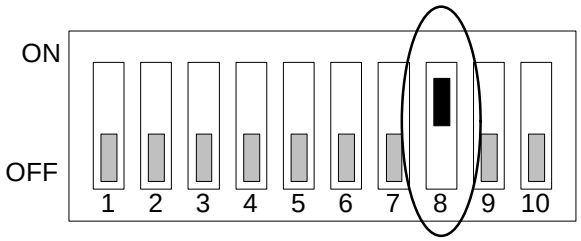


Figure 3-12 M5: Terminal Select

(C) COM-A RS-232/TTL Select (SW1-8)



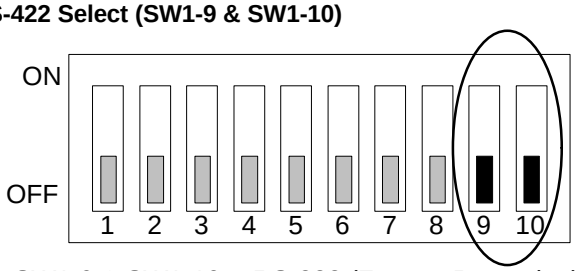
SW1-8 -- RS-232 (Factory Default Setting)



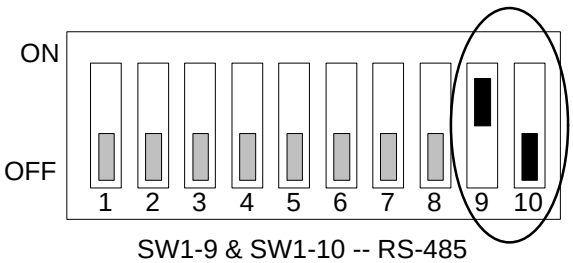
SW1-8 -- TTL

Figure 3-13 SW1-8: COM-A RS-232/TTL Select

(D) COM-B RS-232C/RS-422 Select (SW1-9 & SW1-10)



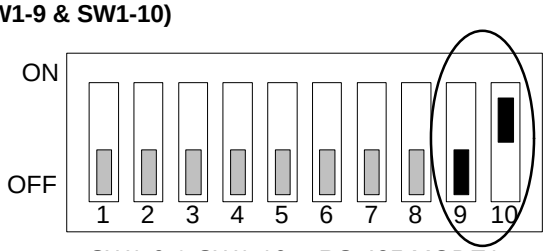
SW1-9 & SW1-10 -- RS-232 (Factory Presetting)



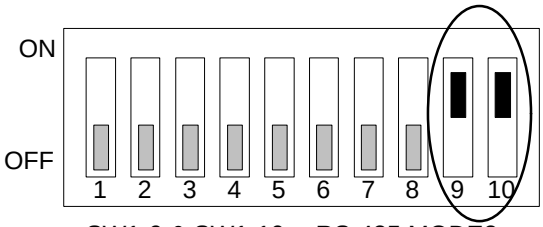
SW1-9 & SW1-10 -- RS-485

Figure 3-14 SW1-9 & SW1-10: COM-B RS-232/RS-422 Select

(E) RS-485 Mode Select (SW1-9 & SW1-10)



SW1-9 & SW1-10 -- RS-485 MODE1



SW1-9 & SW1-10 -- RS-485 MODE2

Figure 3-15 SW1-9 & SW1-10: RS-485 Mode Select

When RS-422 or RS-485 mode is selected, you also need to change M5 to select between RS-422 or RS-485 mode.

NOTE: 1. The recommended configuration for RS-485 interface is to set the transmitter to the controlled by DTR and set the transmitter. Receiver is disabled.

2. The receiver is always enabled, so you will receive data that you transmitted previously. It is not recommended to use this setting as RS-485 interface.

(2) RS-485/RS-422 Connector (CN15)

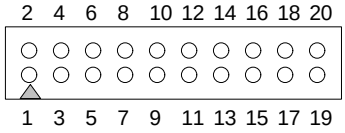


Figure 3-16 CN15: RS-485/RS-422 Connector

CN15	Signal	CN15	Signal
1	-DCDAT	2	-DSRAT
3	RXDAT	4	-RTSAT
5	TXDAT	6	-CTSAT
7	-DTRAT	8	-RIAT
9	GND	10	VCC
11	GND	12	CTS+
13	RTS+	14	CTS-
15	RTS-	16	RXD+
17	TXD+	18	RXD-
19	TXD-	20	GND

Table 3-3 RS-485/RS-422 Pin Assignment

(3) TTL Connector (CN16)

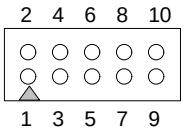


Figure 3-17 CN16: TTL Connector

CN16	Signal	CN16	Signal
1	TTLOP0	2	TTLIP0
3	TTLOP1	4	TTLIP1
5	TTLOP2	6	TTLIP2
7	TTLOP3	8	TTLIP3
9	GROUND	10	VCC

Table 3-4 TTL Pin Assignment

(4) RS-232 Connector (CN4)

There are four serial ports with EIA RS-232C interface on the AR-B1462. To configure these serial ports, use the BIOS Setup program, and adjust the jumpers on M5 and SW1.

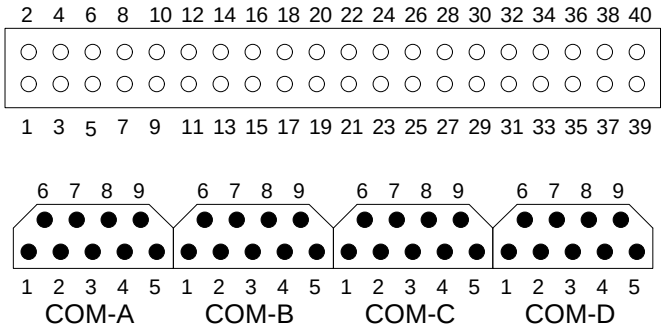


Figure 3-18 CN4: RS-232 Connector

CN4	DB-9	Signal	CN4	DB-9	Signal
1	A-1	-DCDA	2	A-6	-DSRA
3	A-2	RXDA	4	A-7	-RTSA
5	A-3	TXDA	6	A-8	-CTSA
7	A-4	-DTRA	8	A-9	-RIA
9	A-5	GNDA	10	--	GNDA
11	B-1	-DCDB	12	B-6	-DSRB
13	B-2	RXDB	14	B-7	-RTSB
15	B-3	TXDB	16	B-8	-CTSB
17	B-4	-DTRB	18	B-9	-RIB
19	B-5	GNDB	20	--	GNDB
21	C-1	-DCDC	22	C-6	-DSRC
23	C-2	RXDC	24	C-7	-RTSC
25	C-3	TXDC	26	C-8	-CTSC
27	C-4	-DTRC	28	C-9	-RIC
29	C-5	GNDC	30	--	GNDC
31	D-1	-DCDD	32	D-6	-DSRD
33	D-2	RXDD	34	D-7	-RTSD
35	D-3	TXDD	36	D-8	-CTSD
37	D-4	-DTRD	38	D-9	-RID
39	D-5	GNDD	40	--	GNDD

Table 3-5 RS-232 Connector Pin Assignment

3.2.7 Keyboard Connector

(1) Keyboard Lock Header (J7)

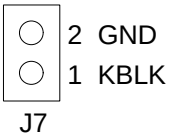


Figure 3-19 J7: Keyboard Lock Header

(2) Keyboard Connector (J4)

This keyboard connector is a PS/2 type keyboard connector. This connector is also for a standard IBM-compatible keyboard with the keyboard adapter cable. J4 provides the way of connecting a keyboard to the AR-B1462.

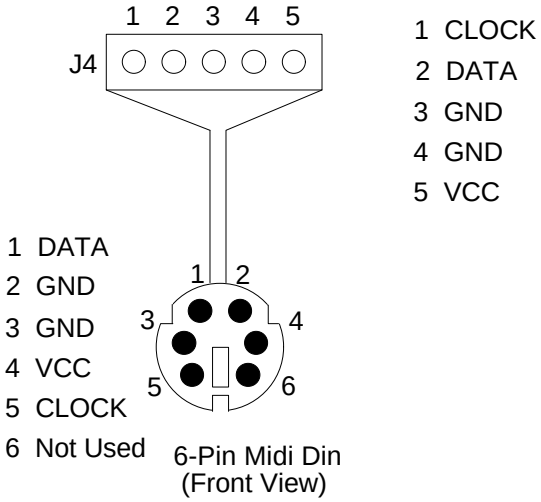


Figure 3-20 J4: Keyboard Connector

3.2.8 External Speaker Header (J9)

Besides the onboard buzzer, you can use an external speaker by connecting to the J9 header.

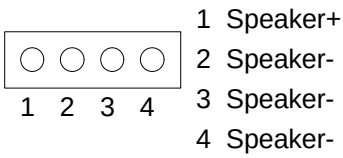


Figure 3-21 J9: Speaker Header

3.2.9 Power Connector

(1) 8-Pin Power Connector (J1)

J1 is an 8-pin power connector. You can directly connect the power supply to the onboard power connector for stand-alone applications.

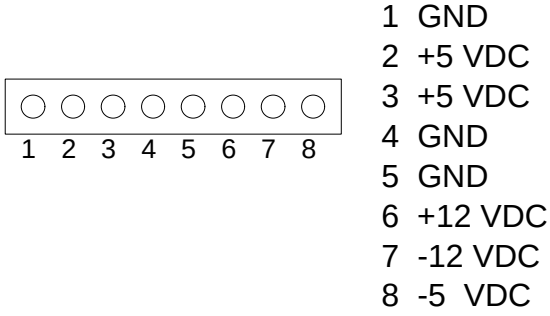


Figure 3-22 J1: 8-Pin Power Connector

(2) 4-Pin Power Connector (CN6)

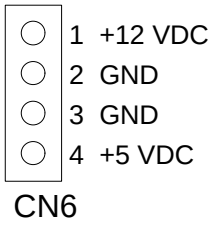


Figure 3-23 CN6: 4-Pin Power Connector

3.2.10 Reset Header (J6)

J6 is used to connect to an external reset switch. Shorting these two pins will reset the system.

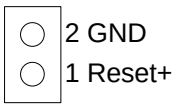


Figure 3-24 J6: Reset Header

3.2.11 PS/2 Mouse Connector

(1) PS/2 Mouse IRQ12 Setting (JP2)

The default of <Enabled> allows the system detecting a PS/2 mouse on boot. If detected, IRQ12 will be used for the PS/2 mouse. IRQ12 will be reserved for expansion cards and therefore the PS/2 mouse will not function.

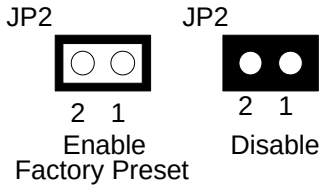


Figure 3-25 JP2: PS/2 Mouse IRQ12 Setting

CAUTION: After adjusting the JP2 correctly, the user must set the <PS/2 Mouse Support> option to Enabled in the BIOS <Advanced CMOS Setup> Menu. Then the PS/2 mouse can be used.

(2) PS/2 Mouse Connector (J5)

To use the PS/2 interface, an adapter cable has to be connected to the J5 (6-pin header type) connector. This adapter cable is mounted on a bracket and is included in your AR-B1462 package. The connector for the PS/2 mouse is a Mini-DIN 6-pin connector. Pin assignments for the PS/2 port connector are as follows:

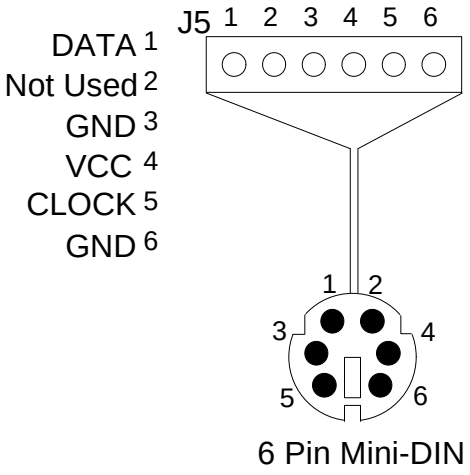


Figure 3-26 J5: PS/2 Mouse Connector

3.2.12 Battery Setting

(1) Battery Charger Select (JP9)

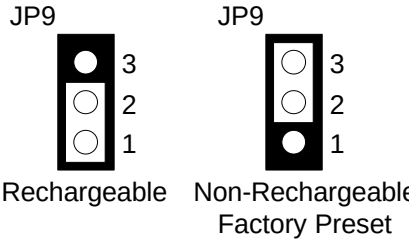


Figure 3-27 JP9: Battery Charger Select

(2) External Battery Connector (J8)

J8 allows users to connector an external 4.5 to 6 VDC battery to the AR-B1462, if the on-board battery is fully discharged. Only the SRAM disk will draw the battery current. If no SRAM chips will be used, no battery is needed. The battery charger on AR-B1462 does not source charge current to the external battery which connects to J8.

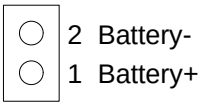


Figure 3-28 J8: External Battery Connector

3.2.13 26-Pin Audio Connector (CN10)

The AR-B1462 didn't support the audio function, only using the AR-B1462A just find this connector.

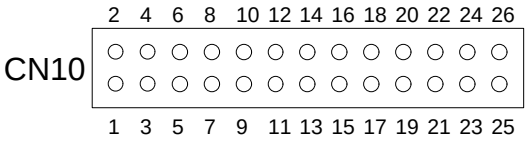


Figure 3-29 CN10: 26-Pin Audio Connector

CN10	Signal	CN10	Signal
1	AUXAL	2	LINEL
3	AUXAR	4	LINER
5	+12V	6	VJOYS
7	AUDIOL	8	MICPH
9	AUDIOR	10	PCSPKO
11	GND	12	GND
13	MIDIIN	14	MIDIOP
15	GND	16	GND
17	-JSWA	18	JTMA
19	-JSWB	20	JTMB
21	-JSWC	22	JTMC
23	-JSWD	24	JTMD
25	GND	26	GND

Table 3-6 Audio Connector Pin Assignment

3.2.14 CPU Setting

The AR-B1462 accepts many types of microprocessors such as Intel/AMD/Cyrix 486DX/DX2/DX4. All of these CPUs include an integer processing unit, floating-point processing unit, memory-management unit, and cache. They can give a two to ten-fold performance improvement in speed over the 386 processor, depending on the clock speeds used and specific application. Like the 386 processor, the 486 processor includes both segment-based and page-based memory protection schemes. The instruction of processing time is reduced by on-chip instruction pipelining. By performing fast, on-chip memory management and caching, the 486 processor relaxes requirements for memory response for a given level of system performance.

(1) CPU Logic Core Voltage Select (M6)

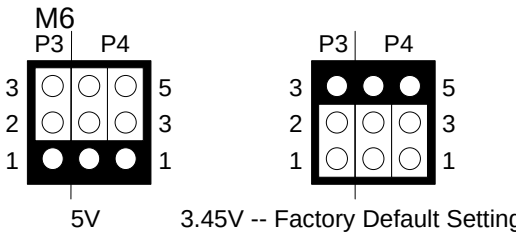


Figure 3-30 M6: CPU Logic Core Voltage

(2) AMD 3X/4X CPU Select (JP11)

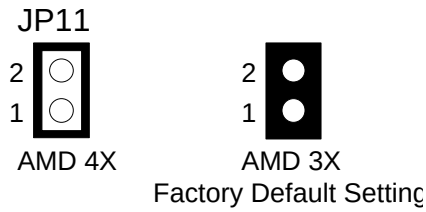


Figure 3-31 JP11: AMD 3X/4X CPU Select

(3) PCI Clock Select (JP4)

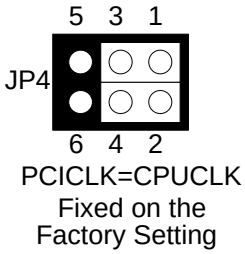


Figure 3-32 JP4: PCI Clock Select

(4) CPU Base Clock Select (JP3)

PIN1-2	PIN3-4	PIN5-6	Base Clock
Close	Close	Close	50MHz
Close	Close	Open	40MHz
Close	Open	Close	33.3MHz
Close	Open	Open	25MHz
Open	Close	Close	20MHz
Open	Close	Open	16MHz
Open	Open	Close	12MHz
Open	Open	Open	8MHz

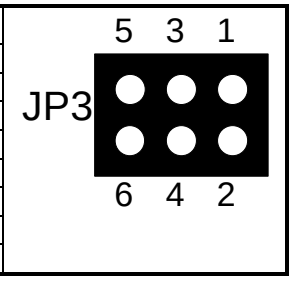


Table 3-7 JP3: CPU Base Clock Select

(5) CPU Cooling Fan Power Connector (CN3)

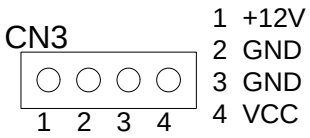


Figure 3-33 CN3: CPU Cooling Fan Power Connector

3.2.15 PCI Connector

(1) PCI Connector Power Select (JP1)

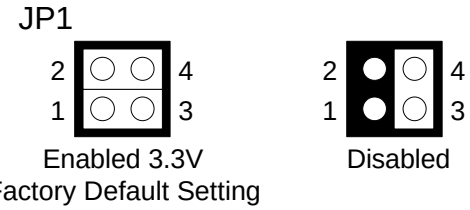


Figure 3-34 JP1: PCI Connector Power Select

(2) 120-Pin PCI Connector (CN1)

CN1

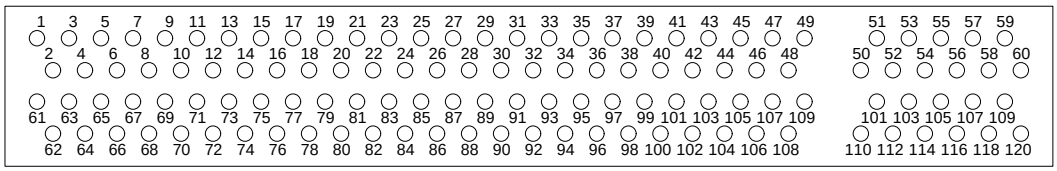


Figure 3-35 CN1: 120-Pin PCI Connector

CN1	Signal	CN1	Signal	CN1	Signal	CN1	Signal
1	-TRST	2	+12V	61	-12V	62	TCK
3	TMS	4	TDI	63	GND	64	TD0
5	+5V	6	-INTA	65	+5V	66	+5V
7	-INTC	8	+5V	67	-INTB	68	-INTD
9	NC	10	+5V	69	-PRST1	70	NC
11	NC	12	GND	71	-PRST2	72	GND
13	GND	14	NC	73	GND	74	NC
15	-RST	16	+5V	75	GND	76	CLK
17	-GNT	18	GND	77	GND	78	-REQ
19	NC	20	AD30	79	+5V	80	AD31
21	+3.3V	22	AD28	81	AD29	82	GND
23	AD26	24	GND	83	AD27	84	AD25
25	AD24	26	IDSEL	85	+3.3V	86	C/BE3
27	+3.3V	28	AD22	87	AD23	88	GND
29	AD20	30	GND	89	AD21	90	AD19
31	AD18	32	AD16	91	+3.3V	92	AD17
33	+3.3V	34	-FRAME	93	C/BE2	94	GND
35	GND	36	-TRDY	95	-IRDY	96	+3.3V
37	GND	38	-STOP	97	-DEVSL	98	GND
39	+3.3V	40	SDONE	99	-LOCK	100	-PERR
41	-SB0	42	GND	101	+3.3V	102	-SERR
43	PAR	44	AD15	103	+3.3V	104	C/BE1
45	+3.3V	46	AD13	105	AD14	106	GND
47	AD11	48	GND	107	AD12	108	AD10
49	AD9	50	C/BE0	109	GND	110	AD8
51	+3.3V	52	AD6	111	AD7	112	+3.3V
53	AD4	54	GND	113	AD5	114	AD3
55	AD2	56	AD0	115	GND	116	AD1
57	+5V	58	-REQ64	117	+5V	118	-ACK64
59	+5V	60	+5V	119	+5V	120	+5V

Table 3-8 Audio Connector Pin Assignment

3.2.16 Memory Setting

(1) DRAM Configuration

There are two 32-bit memory banks on the AR-B1462 board. It can be one-side or double-side SIMM (Single-Line Memory Modules) which is designed to accommodate 256KX36 bit to 16MX36-bit SIMMs. This provides the user with up to 128MB of main memory. The 32-bit SIMM (without parity bit) also can be used on AR-B1462 board. There are listing on-board memory configurations available. Please refer to the following table for details:

SIMM1	SIMM2	Total Memory
256KX32(X36)	None	1MB
256KX32(X36)	256KX32(X36)	2MB
512KX32(X36)	None	2MB
512KX32(X36)	512KX32(X36)	4MB
1MX32(X36)	None	4MB
1MX32(X36)	1MX32(X36)	8MB
2MX32(X36)	None	8MB
2MX32(X36)	2MX32(X36)	16MB
4MX32(X36)	None	16MB
4MX32(X36)	4MX32(X36)	32MB
8MX32(X36)	None	32MB
8MX32(X36)	8MX32(X36)	64MB
16MX32(X36)	None	64MB
16MX32(X36)	16MX32(X36)	128MB

Table 3-9 DRAMs' Configuration

(2) Cache RAM Select (JP10)

The AR-B1462 can be configured to provide a write-back or write-through cache scheme and support 512KB cache systems. A write-back cache system may provide better performance than a write-through cache system. The BIOS Setup program allows you to set the cache scheme either write-back or write-through, either the internal cache selection.

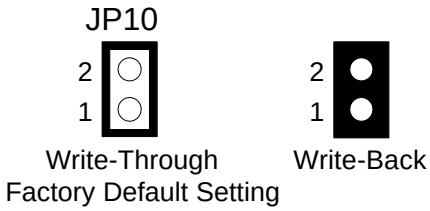


Figure 3-36 JP10: Write-Through/Write-Back CPU Select

3.3 ETHERNET CONTROLLER

The Ethernet controller of the AR-B1462 is a highly integrated design that provides all Media Access Control (MAC) and Encode-Decode (ENDEC) functions in accordance with the IEEE 802.3 standard. Network interfaces include 10BASE5 or 10BASE2 Ethernet via 10BASE-T via the Twisted-pair. The Ethernet controller can interface directly to the PC-AT ISA bus without any external device. The interface to PC-AT ISA bus is fully compatible with NE2000 Ethernet adapter cards, so all software programs designed for NE2000 can run on the Ethernet controller card without any modification.

Microsoft's Plug and Play and the jumperless software configuration function are both supported. The capability of the PnP and Non-PnP mode autoswitch function allows users to configure network card. No jumpers or switches are needed to set when using either the PC or PnP function. The integrated 8KX16 SRAM and 10BASE-T transceiver make Ethernet controller more cost-effective.

3.3.1 Network 4-Pin Connector (J3)

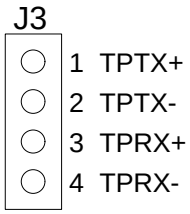


Figure 3-37 J3: Network Connector

3.3.2 AUI Connector (CN2)

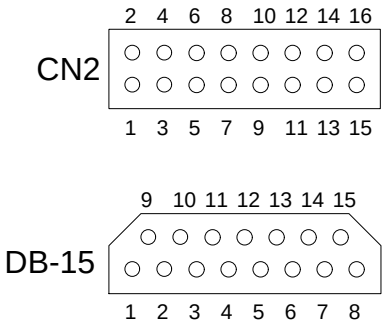


Figure 3-38 CN2: AUI Connector

CN2	DB-15	Signal	CN2	DB-15	Signal
1	1	GND	2	9	T5CD-
3	2	T5CD+	4	10	T5TX-
5	3	T5TX+	6	11	GND
7	4	GND	8	12	T5RX-
9	5	T5RS+	10	13	+12V
11	6	GND	12	14	GND
13	7	Not Used	14	15	Not Used
15	8	GND	16	--	Not Used

Table 3-10 AUI Connector Pin Assignment

4. CRT/LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure using LCD and CRT display.

- Connecting the CRT Monitor
- LCD Flat Panel Display
- Supported LCD Panel

4.1 CONNECTING THE CRT MONITOR

To connect a CRT monitor, an adapter cable has to be connected to the CN13 (10-pin header type) connector. This adapter cable is included in your AR-B1462 package.

4.1.1 CRT Connector (CN13)

The AR-B1462 support CRT color monitors. AR-B1462 used onboard VGA chipset and supported 1MB on-board VRAM, and the AR-B1462A supported 2MB on-board VRAM. For different VGA display modes, your monitor must possess certain characteristics to display the mode you want.

To connect to a CRT monitor, an adapter cable has to be connected to the CN13 connector. CN13 is used to connect with a VGA monitor when you are using the on-board VGA controller as a display adapter.

CN13 is a 10-pin connector that attaches to the CRT monitor via a HD-sub 15-pin adapter cable. Pin assignments for the CN13 & HDB15 connector is as follows:

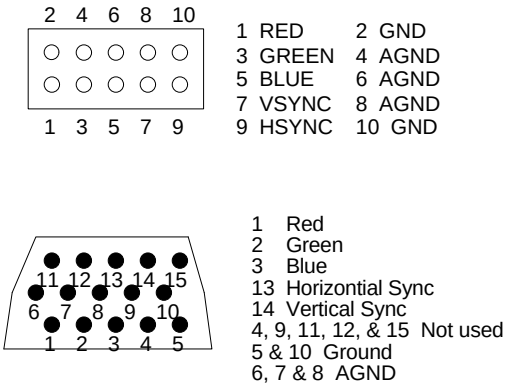


Figure 4-1 CN13: CRT Connector

CN13	DB-15	FUNCTION	CN13	DB-15	FUNCTION
1	1	Red	2	5	GND
3	2	Green	4	6	AGND
5	3	Blue	6	7	AGND
7	14	V-sync	8	8	AGND
9	13	H-sync	10	10	GND

Table 4-1 CRT Connector Assignment

4.2 LCD FLAT PANEL DISPLAY

This section describes the configuration and installation procedure for a LCD display. Skip this section if you are using a CRT monitor only.

Use the Flash memory Writer utility to download the new BIOS file into the ROM chip to configure the BIOS default settings for different types of LCD panels. Next, set your system properly and configure the AR-B1462 VGA module for the right type of LCD panel you are using.

The following shows the block diagram of the system when using the AR-B1462 with a LCD display.

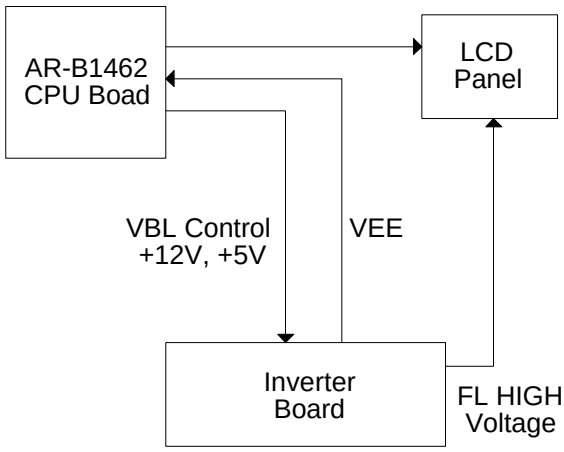


Figure 4-2 LCD Panel Block Diagram

The block diagram shows that the AR-B1462 still needs components to use with a LCD panel. The inverter board provides the control for the brightness and the contrast of the LCD panel. The inverter is also the components that supply the high voltage to drive the LCD panel. Each item will be explained further in the section.

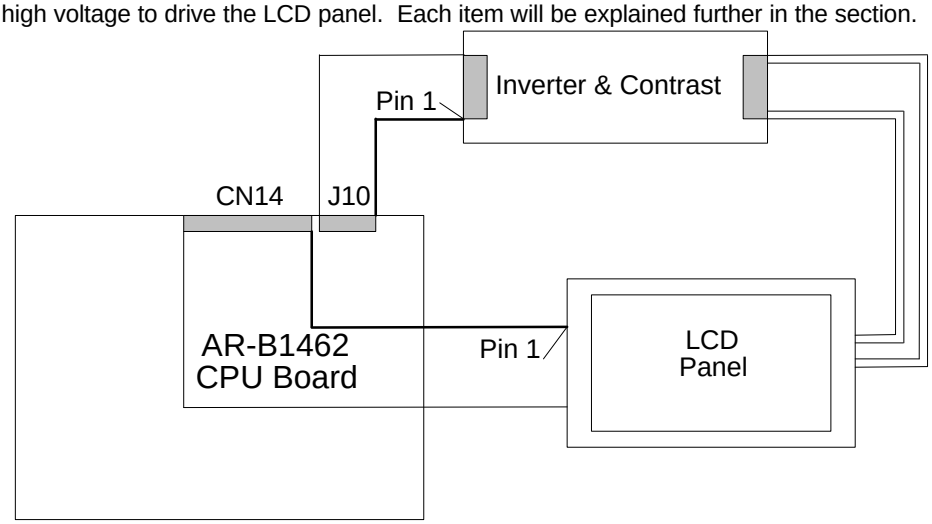


Figure 4-3 LCD Panel Cable Installation Diagram

NOTE: Be careful with the pin orientation when installing connectors and the cables. A wrong connection can easily destroy your LCD panel. Pin 1 of the cable connector is indicated with a sticker and pin1 of the ribbon cable is usually has a different color.

4.2.1 Inverter Board Description

The inverter board supplies high voltage signals to drive the LCD panel by converting the 12 volt signal from the AR-B1462 into a high voltage AC signal for LCD panel. It can be installed freely on the space provided over the VR board. If the VR board is installed on the bracket, you have to provide a place to install the inverter board into your system.

4.2.2 LCD Connector

(1) DE/E Signal from M or LP Select (JP6)

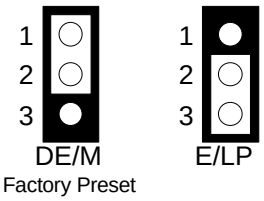


Figure 4-4 JP6: DE/E Signal from M or LP

(2) DENAVEE & DVEE Signal Select (JP5)

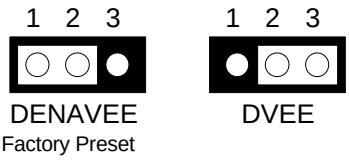


Figure 4-5 JP5: DENAVEE & DVEE Signal Select

(3) LCD Control Connector (J10)

J10 is a 5-pin connector that attaches to the Contrast and Backlight board, Its pin assignment is shown below:

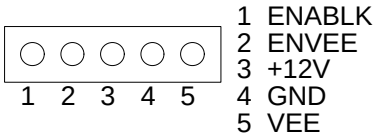


Figure 4-6 J10: LCD Control Connector

(4) Touch Screen Connector (J2)

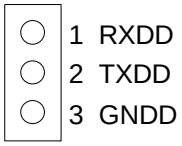
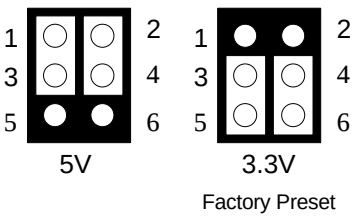


Figure 4-7 J2: Touch Screen Connector

(5) LCD Voltage Selector (JP12)

JP12 is used to select the LCD voltages to be 3.3V or 5V.



(6) LCD Panel Display Connector (CN14)

Attach a display panel connector to this 44-pin connector with pin assignments as shown below:

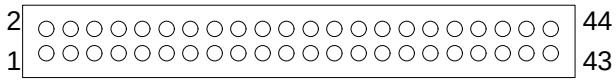


Figure 4-8 CN14: LCD Display Connector

Pin	Signal	Pin	Signal
1	GND	2	SHFCLK
3	GND	4	LP
5	FLM	6	GND
7	P0	8	P1
9	P2	10	P3
11	P4	12	P5
13	GND	14	P6
15	P7	16	P8
17	P9	18	P10
19	P11	20	GND
21	P12	22	P13
23	P14	24	P15
25	P16	26	P17
27	GND	28	P18
29	P19	30	P20
31	P21	32	P22
33	P23	34	GND
35	VCC	36	VCC
37	+12V	38	+12V
39	GND	40	GND
41	DE	42	ENABLK
43	GND	44	VEE

Table 4-2 LCD Display Assignment

4.3 SUPPORTED LCD PANEL

At present, this VGA card can provide a solution with an inverter board for the following list of standard LCD panels. Consult your Acrosser representative for new developments. When using other models of standard LCD panels in the market.

NO.	Manufacture	Model No.	Description
1	NEC	NL-6448AC30-10	TFT 9.4”
2	NEC	NL-6448AC32-10	TFT 10.2”
3	NEC	NL-6448AC33-10	TFT 10.4”
4	HITACHI	LMG5371	MONO 9.4” Dual Scan
5	HITACHI	LMG9200	DSTN 9.4”
6	HITACHI	LMG9400	DSTN 10.4”
7	ORION	OGM-640CN03C-S	DSTN 10.4”
8	SHARP	LQ10D321	TFT 10.4”

Table 4-3 LCD Panel Type List

CAUTION: 1. If you want to connect the LCD panel, you must update the AR-B1462’s BIOS, then you can setup the corrected BIOS. Please contact Acrosser for the latest BIOS update.

2. If user needs to update the BIOS version or connect other LCD, please contact the sales department. The detail supported LCDs are listed in the Acrosser Web site, user can download the suitable BIOS. The address is as follows:

http:\\www.acrosser.com

5. INSTALLATION

This chapter describes the procedure of the utility diskette installation. The following topics are covered:

- Overview
- Utility Diskette
- Watchdog Timer

5.1 OVERVIEW

This chapter provides information for you to set up a working system based on the AR-B1462 CPU board. Please read the details of the CPU board' s hardware descriptions before installation carefully, especially jumpers' setting, switch settings and cable connections.

Follow steps listed below for proper installation:

Step 1 : Read the CPU card' s hardware description in this manual.

Step 2 : Install any DRAM SIMM onto the CPU card. (or user can skip this step because that the AR-B1462 embedded on-board DRAM)

Step 3 : Set jumpers.

Step 4 : Make sure that the power supply connected to your passive CPU board backplane is turned off.

Step 5 : Plug the CPU card into a free AT-bus slot or PICMG slot on the backplane and secure it in place with a screw to the system chassis.

Step 6 : Connect all necessary cables. Make sure that the FDC, HDC, serial and parallel cables are connected to pin 1 of the related connector.

Step 7 : Connect the hard disk/floppy disk flat cables from the CPU card to the drives. Connect a power source to each drive.

Step 8 : Plug the keyboard into the keyboard connector.

Step 9 : Turn on the power.

Step 10: Configure your system with the BIOS Setup program then re-boot your system.

Step 11: If the CPU card does not work, turn off the power and read the hardware description carefully again.

Step 12: If the CPU card still does not perform properly, return the card to your dealer for immediate service.

5.2 UTILITY DISKETTE

AR-B1462 provides two VGA driver diskettes, support WIN31, WIN95, WINNT 4.0 & OS/2; and one audio driver diskette. If your operating system is the other operating system, please attach Acrosser that will provide the technical supporting for the VGA resolution.

There are two diskettes: disk#2 is for WIN31, WIN95 & WINNT4.0 VGA resolution, disk#3 is for WINNT3.5 and OS/2 VGA resolution. While user extracted the compressed files there is the README.* file in each sub-directories. Please refer to the file of README for any troubleshooting before install the driver. The disk#1 is for SSD and network utility driver. The AR-B1462A supports audio function, so the disk provides audio driver.

5.2.1 VGA Driver

(1) WIN 3.1 Driver

For the WIN31 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

Step 1: Make the new created directory to put the VGA drivers.
```
C:\>MD VGAW31
```

Step 2: Insert the Utility Disk #2 in the floppy disk drive, and then copy the compress file –VGAWIN31.ZIP, and the extract program –PKUNZIP.EXE, in the new created directory.
```
C:\>COPY A:\ VGAWIN31.ZIP C:\VGAW31
C:\>COPY A:\PKUNZIP.EXE C:\VGAW31
```

Step 3: Change directory to the new created directory, and extract the compress file.
```
C:\>CD VGAW31
C:\VGAW31>PKUNZIP -d VGAWIN31.ZIP
```

Step 4: In the DOS mode execute the SETUP.EXE file.
C:\VGAW31>SETUP

Step 5: The screen shows the chip type, and presses any key enter the main menu.
CHIPS 655XX - PCI Display Drivers
Preliminary Version 3.3.0

Step 6: There are some items for choice to setup. Please choose the <Windows Version 3.1> item, notice the function key defined. Press [ENTER] selected the <All Resolutions>, when this line appears [*] symbol, that means this item is selected. Press [End] starts to install.

Step 7: The screen will show the dialog box to demand user typing the WIN31's path. The default is C:\WINDOWS.

Step 8: Follow the setup steps' messages execute. As completed the setup procedure will generate the message as follow.

Installation is done!

Change to your Windows directory and type SETUP to run the Windows Setup program. Choose one of the new drivers marked by an *. Please refer to the User's Guide to complete the installation.

Step 9: Presses [Esc] return the main menu, and re-press [Esc] return to the DOS mode.

Step 10: And then re-name the OEM655XX.INF file as OEM65DGM.INF in the system directory of cwin31 directory. Acrosser recommends the method as:

C:\WINDOWS\SYSTEM>COPY OEM655XX.INF OEM65DGM.INF

Step 11: In the WIN31, you can find the <Chips CPL> icon located in the {CONTROL PANEL} group.

Step 12: Adjust the <Refresh Rate>, <Cursor Animation>, <Font size>, <Resolution>, and <Big Cursor>.

(2) WIN 95 Driver

For the WIN95 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

Step 1: Make the new created directory to put the VGA drivers.
C:\>MD VGAW95

Step 2: Insert the Utility Disk #2 in the floppy disk drive, and then copy the compress file –VGAWIN95.ZIP, and the extract program –PKUNZIP.EXE, in the new created directory.
C:\>COPY A:\VGAWIN95.ZIP C:\VGAW95
C:\>COPY A:\PKUNZIP.EXE C:\VGAW95

Step 3: Change directory to the new created directory, and extract the compress file.
C:\>CD VGAW95
C:\VGAW95>PKUNZIP -d VGAWIN95.ZIP

Step 4: Enter the WIN95 operation system, please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
C:\VGAW95

Step 5: And then you can find the <Chips and Tech 65550 PCI (new)> item, select it and click the <OK> button.

Step 6: Finally, user can find the <DISPLAY> icon adds the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size> ..and other functions. Please refer to the messages during installation.

(3) WINNT Driver

For the WINNT4.0 and WINNT3.5 operating system, user must in the DOS mode decompress the compress file. And then the following steps are for WINNT4.0, if you use WINNT3.5 for the disk#3 as to the steps:

Step 1: Make the new created directory to put the VGA drivers.
C:\>MD VGANT40

Step 2: Insert the Utility Disk #2 in the floppy disk drive, and then copy the compress file –WINNT40.ZIP, and the PKUNZIP.EXE program –, in the new created directory.
C:\>COPY A:\WINNT40.ZIP C:\VGANT40
C:\>COPY A:\PKUNZIP.EXE C:\VGANT40

Step 3: Change directory to the new created directory, and extract the compress file.
C:\>CD VGANT40
C:\VGANT40>PKUNZIP -d WINNT40.ZIP

Step 4: Enter the WINNT4.0 operation system, please choose the <SETTING> item of the <DISPLAY> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
C:\VGANT40

Step 5: And then you can find the <Chips and Tech 65550 PCI (new)> item, select it and click the <OK> button.

Step 6: Finally, user can find the <DISPLAY> icon adds the <Chips> item. You can select this item, and adjust the <Screen Resolution>, <Refresh Rate>, <Font Size> ..and other function. Please refer to the messages during installation.

(4) OS/2 Warp Driver

The following steps must be performed before you install the 65550 display's driver:

CAUTION:

1. OS/2 DOS Support must be installed.
2. If you previously installed SVGA support, you must do the following:
   a) Close all DOS Full Screen and WIN-OS2 sessions.
   b) Reset the system to VGA mode. VGA is the default video mode enabled when OS/2 is installed. To restore VGA mode, use Selective Install and select VGA for Primary Display. For more information on this procedure, see the section on Changing Display Adapter Support in the OS/2 Users Guide.

To install this driver, do the following steps:

Step 1: Open an OS/2 full screen or windowed session.

Step 2: Place the 65550 PCI Display Driver Diskette in drive A. (DISK #3)

Step 3: Because the diskette enclosed the compress file, to extract file had to as the steps.

Step 4: In the OS/2-DOS mode, make the VGA directory for decompress the driver.
C:\>MD VGAOS2
C:\>CD VGAOS2
C:\VGAOS2>COPY A:\VGAOS2.ZIP
C:\VGAOS2>PKUNZIP -d VGAOS2.ZIP

Step 5: At the OS/2 command prompt, type the following commands to copy the files to the OS/2 drive:
C:\VGAOS2> SETUP C:\VGAOS2 C: <ENTER>

Step 6: When the Setup Program is completed, you will need to perform a shutdown and then restart the system in order for changes to take effect.

Step 7: Please refer to the README.TXT file, there is detail description, user had to according to the installation step by step. When install completed, user can adjust the VGA resolution in the SYSTEM icon <SCREEN> item of the <SYSTEM SETUP>.

5.2.2 Audio Driver

(1) WIN 3.1 Driver

For the WIN31 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

Step 1: Make the new created directory to put the audio drivers.
C:\>MD AUW31

Step 2: Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file –WIN31DRV.ZIP, and the extract program –PKUNZIP.EXE, in the new created directory.
C:\>COPY A:\ AUDIO\WIN31DRV.ZIP C:\AUW31
C:\>COPY A:\PKUNZIP.EXE C:\AUW31

Step 3: Change directory to the new created directory, and extract the compress file.
C:\>CD AUW31
C:\AUW31>PKUNZIP -d WIN31DRV.ZIP

Step 4: In the FILE MANAGER ICON execute the SETUP.EXE file.

Step 5: The screen shows the chip type, and presses any key enter the main menu.

Step 6: There are some items for choice to setup. Please choose the <Driver Installation> item, notice the function key defined. And then the screen shows the hardware setting, press [OK] starts to install.

Step 7: Completed the installation, user will find two drivers: <ESS AudioDrive ES1869 4.17.08> and <ESS AudioDrive MPU-401 4.17.08>.

(2) WIN 95 Driver

For the WIN95 operating system, user must in the DOS mode decompress the compress file. And then as to the steps:

Step 1: Make the new created directory to put the audio drivers.
C:\>MD AUW95

Step 2: Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file —WIN95DRV.ZIP, and the extract program —PKUNZIP.EXE, in the new created directory.
C:\>COPY A:\AUDIO\WIN95DRV.ZIP C:\AUW95
C:\>COPY A:\PKUNZIP.EXE C:\AUW95

Step 3: Change directory to the new created directory, and extract the compress file.
C:\>CD AUW95
C:\AUW95>PKUNZIP -d WIN95DRV.ZIP

Step 4: In the WIN95 operation system, please choose the <ADDING NEW HARDWARE> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
C:\AUW95

Step 5: And then you can find the <ES1869 Plug and Play AudioDrive> item, select it and click the <OK> button.

Step 6: Finally, the installation is completed and user must reboot the system.

(3) WINNT Driver

For the WINNT4.0 and WINNT3.5 operating system, user must in the DOS mode decompress the compress file. And then the following steps are for WINNT4.0:

Step 1: Make the new created directory to put the audio drivers.
C:\>MD AUNT40

Step 2: Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file —NT40DRV.ZIP, and the PKUNZIP.EXE program —, in the new created directory.
C:\>COPY A:\AUNT40\NT40DRV.ZIP C:\AUNT40
C:\>COPY A:\PKUNZIP.EXE C:\AUNT40

Step 3: Change directory to the new created directory, and extract the compress file.
C:\>CD AUNT40
C:\AUNT40>PKUNZIP -d NT40DRV.ZIP

Step 4: In the WINNT4.0 operation system, please choose the <ADDING NEW HARDWARE> icon in the {CONTROL PANEL}. Please select the <From Disk Install> item, and type the factory source files' path.
C:\AUNT40

Step 5: And then you can find the <ES1869 Plug and Play AudioDrive> item, select it and click the <OK> button.

Step 6: Finally, the installation is completed and user must reboot the system.

(4) DOS Driver

Step 1: Make the new created directory to put the audio drivers.
```
C:\>MD AUDOS
```

Step 2: Insert the Utility Disk #1 in the floppy disk drive, and then copy the compress file –DOSDRV.ZIP, and the extract program –PKUNZIP.EXE, in the new created directory.
```
C:\>COPY A:\AUDIO\DOSDRV.ZIP C:\AUDOS
C:\>COPY A:\PKUNZIP.EXE C:\AUDOS
```

Step 3: Change directory to the new created directory, and extract the compress file.
```
C:\>CD AUDOS
C:\AUDOS>PKUNZIP -d DOSDRV.ZIP
```

Step 4: In the DOS mode execute the SETUP.EXE file.
```
C:\AUDOS>ESS
```

Step 5: The screen shows the hardware configuration items for setup the base address, IRQ, DMA ..etc. If these items setting all are correct. The setup will ask the directory to install the files. The default directory is C:\AUDIODRV, and then press the [ENTER] key the installation is completed.

5.2.3 Network & SSD Utility

The first diskette provides two functions for user application. The file list is as follow:

UM9008	ZIP
PKUNZIP	EXE
README	DOC

The third diskette also provides SSD functions drivers. The file list is as follow:

SSD	<DIR>	
	WD1462	EXE
	WP1462	EXE
	RFG	EXE
	RFGDEMO	PGF

(1) Network Utility

1. Use PKUNZIP.EXE program to decompress the file in the DOS mode, and use the command to decompress. The decompressing active is as follow:
   For Example
   ```
   C:\>MD NET
   C:\>CD NET
   C:\NET>COPY A:\PKUNZIP.EXE C:\NET
   C:\NET>COPY A:\UM9008.ZIP C:\NET
   C:\NET>PKUNZIP -D UM9008.ZIP
   ```

2. And then enter the operation system, as the installation steps process. Please refer to the decompressed file. There is the README file in every sub-directory, and has detail description for using the drivers.

(2) SSD Utility

To support the AR-B1462 solid state disk's operations, the following files have been provided on the enclosed diskette #3's directory <SSD>.

(A) WD1462.EXE

WD1462.EXE This program demonstrates how to enable and trigger the watchdog timer. It allows you to test the <TIMES-OUT & RESET> function when the watchdog timer is enabled.

(B) WP1462.EXE

WP1462.EXE This program demonstrates how to enable and disable software write protected function. It also shows the current protect mode of write or read only memory.

(C) RFG.EXE

RFG.EXE This program is used to generate ROM pattern files in a binary format. Each ROM pattern file has the same size as the FLASH or EPROM and can be easily programmed on to the FLASH with on-board programmer or on to EPROM with any EPROM programmer. If you have specified a DOS drive in the *.PGF file, RFG will generate bootable ROM pattern files for the EPROM or FLASH disk. The RFG supports the following DOS, MS-DOS, PC-DOS, DR-DOS, and X-DOS.

NOTE: If you want to use AR-B1462 with any DOS which is not supported by RFG, please send your requirement to Acrosser Technology Co., Ltd. or contract with your local sales representative.

The RFG.EXE provided in the utility diskette is a program that converts the files you list in the PGF and convert them into ROM pattern file. The RFG will determine how many EPROMs are needed and generate the same number of ROM pattern files. These ROM pattern files are named with the name assigned by the ROM_NAME in the PGF and the extension names are *.R01, *.R02 ….etc. To generate ROM pattern files.
The ROM File Generator main menu will be displayed on the screen. There are 7 options on the main menu. They serve the following functions:

Quit to DOS
Quits and exits to the DOS

OS Shell
Exits from the RFG temporarily to the DOS prompt. Type <EXIT> to return to the RFG main menu.

Load PFG File
If this option is used, the RFG will prompt you for the PGF file name. This option is useful if you have not previously entered a PGF name or you wish to use a different PGF file. The RFG will check and display the PGF filename, ROM pattern file name, EPROM capacity, DOS version and the number of ROM pattern files that will be generated.

Type Current PGF File
This option instructs the RFG to use the DOS type command to display the contents of the current PGF file.

Generate ROM File(s)
If there is no mistake in your *.PGF file, then this menu option will generate ROM pattern files. The number of ROM pattern file generated by the RFG will depend on the total capacity needed by your files. For instance, if 3 files are generated, then you will need to use 3 EPROMs (The size depends upon the number stated in your PGF). The ROM pattern files will have the same file names, but will have different extension names. For example:

TEST.R01, TEST.R02, TEST.R03 ..etc.

Display Error in PGF File
This option displays errors that were detected in your PGF.

Help to PGF File

This option gives information on how to write a PGF file and how to generate ROM pattern files. An example PGF is also included.

Move the reverse video bar to <Generate ROM File(s)> then press [ENTER]. The ROM pattern file is a binary file. The file size will be the same size as the EPROM that you assigned in the PGF. For example, if you are using 128KX8 EPROM memory chips, then the size of ROM patterns file will be 131072 bytes. For other chips the file size will be:

64KX8 EPROM----65536 bytes
256KX8 EPROM –262144 bytes
512KX8 EPROM---524288 bytes
1MX8 EPROM -----1048576 bytes

(D) RFGDEMO.PGF

RFGDEMO.PGF This file provides a sample PROGRAM GROUP FILE which illustrates how to create ROM pattern files correctly.

The PGF is an ASCII text file that can be created by using any text editor, word processor or DOS <COPY CON> command. The PGF lists what files will be copied and if DOS is going to be copied. This file can have any DOS filename, but the extension name must be *.PGF. For example, followings are valid filenames.

RFGDEMO.PGF
MYRFG.PGF
MSDOS.PGF
…

An examples of the *.PGF file is as follow.

```
ROM_NAME=TEST1      ; ROM pattern file name is TEST1
                    ;The output file names will be TEST1.R01,
                    ;TEST1.R02..etc.
DOS_DRIVE=C:        ; DOS system drive unit is drive C:
                    ;If user does not want to copy DOS
                    ;system files onto the ROM disk
                    ;write as DOS_DRIVE=NONE
ROM_SIZE=128        ;64 means 64KX8 (28F512) EPROM
                    ;size used
                    ;128 means 128KX8 (27C/28F/29F010)
                    ;EPROM size used
                    ;256 means 512KX8 (27C/28F/29F020)
                    ;EPROM size used
                    ;512 means 512KX8 (27C/29F040)
                    ;EPROM size used
                    ;1024 means 1MX8 (27C080) EPROM
                    ;size used
```

The following two files are options which depend on whether the ROM disk is to be bootable or not.

CONFIG.SYS
AUTOEXEC.BAT

```
;Below are user's files
A:\USER1.COM  ; File USER1.COM on root of drive A:
USER2.EXE     ; File USER2.EXE on current directory & drive
C:\TTT\USER3.TXT ; File USER3.TXT on sub-directory TTT of drive C:
```

5.3 WATCHDOG TIMER

This section describes how to use the Watchdog Timer, disabled, enabled, and trigger.
The AR-B1462 is equipped with a programmable time-out period watchdog timer. User can use the program to enable the watchdog timer. Once you have enabled the watchdog timer, the program should trigger it every time before it times out. If your program fails to trigger or disable this timer before it times out because of system hang-up, it will generate a reset signal to reset the system. The time-out period can be programmed to be 3 to 42 seconds.

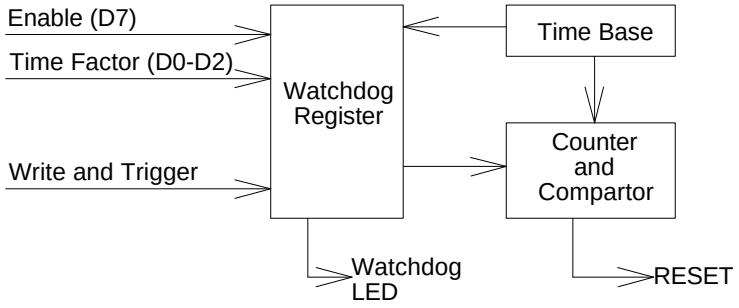


Figure 5-1 Watchdog Block Diagram

5.3.1 Watchdog Timer Setting

The watchdog timer is a circuit that may be used from your program software to detect crashes or hang-ups. Whenever the watchdog timer is enabled, the LED will blink to indicate that the timer is counting. The watchdog timer is automatically disabled after reset.
Once you have enabled the watchdog timer, your program must trigger the watchdog timer every time before it times-out. After you trigger the watchdog timer, it will be set to zero and start to count again. If your program fails to trigger the watchdog timer before time-out, it will generate a reset pulse to reset the system or trigger the IRQ15 signal to tell your program that the watchdog is times out.
The factor of the watchdog timer time-out constant is approximately 6 seconds. The period for the watchdog timer time-out period is between 1 to 7 timer factors.
If you want to reset your system when watchdog times out, the following table listed the relation of timer factors between time-out period.

Time Factor	Time-Out Period (Seconds)
80H	3
81H	6
82H	12
83H	18
84H	24
85H	30
86H	36
87H	42

Table 5-1 Time-Out Setting

If you want to generate IRQ15 signal to warn your program when watchdog times out, the following table listed the relation of timer factors between time-out period. And if you use the IRQ15 signal to warn your program when watchdog timer out, please enter the BIOS Setup the <Peripheral Setup> menu, the <OnBoard PCI IDE> and <IDE Prefetch> these two items must set to ***Primary***.

Time Factor	Time-Out Period (Seconds)
0C0H	3
0C1H	6
0C2H	12
0C3H	18
0C4H	24
0C5H	30
0C6H	36
0C7H	42

Table 5-2 Time-Out Setting

NOTE: 1. If you program the watchdog to generate IRQ15 signal when it times out, you should initial IRQ15 interrupt vector and enable the second interrupt controller (8259 PIC) in order to enable CPU to process this interrupt. An interrupt service routine is required too.

2. Before you initial the interrupt vector of IRQ15 and enable the PIC, please enable the watchdog timer previously, otherwise the watchdog timer will generate an interrupt at the time watchdog timer is enabled.

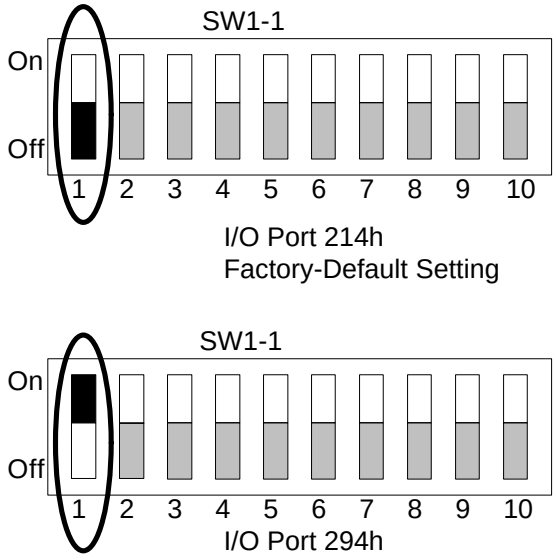


Figure 5-1 SW1-1: Watchdog I/O Port Address Select

5.3.2 Watchdog Timer Enabled

To enable the watchdog timer, you have to output a byte of timer factor to the watchdog register whose address is 214H or Base Port. The following is a BASICA program which demonstrates how to enable the watchdog timer and set the time-out period at 24 seconds.

```
1000        REM Points to command register
1010              WD_REG% = 214H
1020        REM Timer factor = 84H (or 0C4H)
1030              TIMER_FACTOR% = %H84
1040        REM Output factor to watchdog register
1050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

5.3.3 Watchdog Timer Trigger

After you enable the watchdog timer, your program must write the same factor as enabling to the watchdog register at least once every time-out period to its previous setting. You can change the time-out period by writing another timer factor to the watchdog register at any time, and you must trigger the watchdog before the new time-out period in next trigger. Below is a BASICA program which demonstrates how to trigger the watchdog timer:

```
2000        REM Points to command register
2010              WD_REG% = 214H
2020        REM Timer factor = 84H (or 0C4H)
2030              TIMER_FACTOR% = &H84
2040        REM Output factor to watchdog register
2050              OUT WD_REG%, TIMER_FACTOR%
      .,etc.
```

5.3.4 Watchdog Timer Disabled

To disable the watchdog timer, simply write a 00H to the watchdog register.

```
3000        REM Points to command register
3010              WD_REG% = BASE_PORT%
3020        REM Timer factor = 0
3030              TIMER_FACTOR% = 0
3040        REM Output factor to watchdog register
3050              OUT WD_REG%, TIMER_FACTOR%
      ., etc.
```

6.SOLID STATE DISK

The section describes the various type SSDs' installation steps as follows. This chapter describes the procedure of the installation. The following topics are covered:

- Overview
- Switch Setting
- Jumper Setting
- ROM Disk Installation
- DiskOnChip Installation

6.1 OVERVIEW

The AR-B1462 provides three 32-pin JEDEC DIP sockets which may be populated with up to 4MB of EPROM or 2MB of FLASH or 2MB of SRAM disk. It is ideal for diskless systems, high reliability and/or high speed access applications, controller for industrial or line test instruments, and etc.

If small page (less or equal 512 bytes per page) 5V FLASHs were used, you could format FLASH disk and copy files onto FLASH disk just like using a normal floppy disk. You can use all of the related DOS command (such as COPY, DEL ..etc.) to update files on the 5V FLASH disk.

The write protect function allows you to prevent your data on small page 5V FLASH or SRAM disk from accidental deletion or overwrite.

Data retention of SRAM is ensured by an on-board Lithium battery or an external battery pack that could be connected to the AR-B1462.

6.2 SWITCH SETTING

We will show the locations of the AR-B1462 switch, and the factory-default setting.

CAUTION: The switch setting needs to adjust with the jumpers setting, make sure the jumper settings and the switch setting are correct.

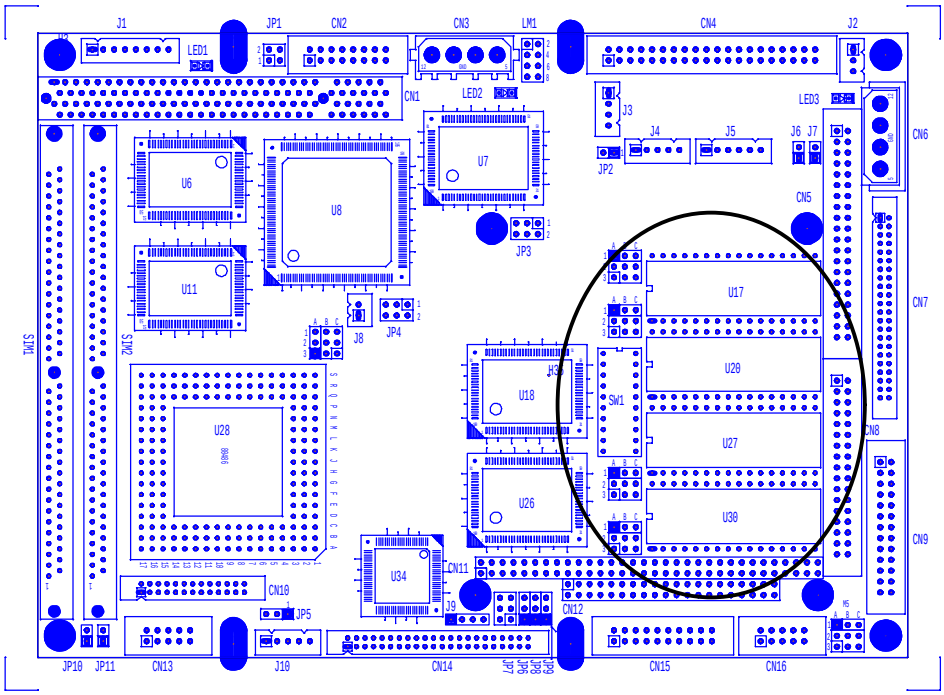


Figure 6-1 Switch & SSD Type Jumper Location

6.2.1 Overview

There is 1 DIP Switch located on the AR-B1462. It performs the following functions:

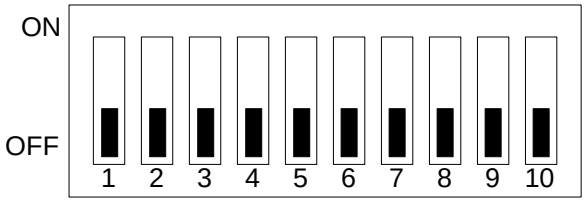


Figure 6-2 SW1: Switch Select

SW1-1	Set the base I/O port address
SW1-2	Set the starting memory address
SW1-3	Reserved
SW1-4 & SW1-5	Set the drive number of solid state disk
SW1-6 & SW1-7	Set the used ROM memory chips
SW1-8, SW1-9 & SW1-10	Mode select of serial port 1/2

6.2.2 I/O Port Address Select (SW1-1)

SW1-1 is provided to select one of the four base port addresses for the watchdog timer and the solid state disk. The AR-B1462 occupies 6 I/O port addresses. Followings state selections of base port address.

SW1-1	Base Port	Solid State Disk	Watchdog
OFF (*)	210h	210h-213h	214h-215h
ON	290h	290h-293h	294h-295h

Table 6-1 I/O Port Address Select

6.2.3 SSD Firmware Address Select (SW1-2)

The AR-B1462's SSD firmware occupies 32KB of memory. SW1-2 is used to select the memory base address. You must select an appropriate address so that the AR-B1462 will not conflict with memory installed on other add-on memory cards. Additionally, be sure not to use shadow RAM area or EMM driver's page frame in this area.

SW1-2	SSD BIOS Address	Bank Memory Address
OFF (*)	D000:0 (16KB)	CC00:0 (16KB)
ON	D000:0 (16KB)	D400:0 (16KB)

Table 6-2 SSD Firmware Address Select

If you are not going to use the solid state disk (SSD), you can use BIOS setup program to disable the SSD BIOS. The AR-B1462 will not occupy any memory address if the SSD BIOS is disabled.

If you are going to install the EMM386.EXE driver, please use the [X] option to prevent EMM386.EXE from using the particular range of segment address as an EMS page which is used by AR-B1462. For example, write a statement in the CONFIG.SYS file as follow: (If the memory configuration of AR-B1462 is CC00:0)

DEVICE=C:\DOS\EMM386.EXE X=CC00-CFFF

6.2.4 SSD Drive Number (SW1-4 & SW1-5)

The AR-B1462 SSD can simulate one or two disk drives. You can assign the drive letter of the AR-B1462 by configuring SW1-4 & SW1-5.

You can make the computer to boot from SSD by copying DOS into the SSD. If your SSD does not have DOS, the computer will boot from your hard disk or floppy disk. In this condition, the SSD BIOS of AR-B1462 will set the drive letter of the SSD to the desired drive letter automatically.

The AR-B1462 would simulate a single disk drive when only (FLASH) EPROM or SRAM (starting from MEM1 socket) is installed. The drive numbers with respect to the switch setting when the AR-B1462 simulates single disk drives.

SW1-4	SW1-5	Occupies floppy disk number (SSD)
OFF (*)	OFF	0 or 1 (Note 1)
ON	OFF	0 or 2 (Note 2)
OFF	ON	0
ON	ON	0

Table 6-3 SSD Drive Number

NOTE: 1. If there is no DOS on this SSD, the disk number will 1 (B:). If any DOS is found by the AR-B1462 SSD BIOS, the disk number will be 0 (A:) But, you can change the disk number from 0 to 1 by pressing the <ESC> key during system bootup.

2. If there is no DOS on this SSD, the disk number will be 2 (C: or D: or ..). If any DOS is found by the AR-B1462 SSD BIOS, the disk number will be 0 (A:). But, you can change the disk number from 0 to 2 by pressing the <ESC> key during system bootup.

(2) Simulate 2 Disk Drive

When (FLASH) EPROM and SRAM are both used on the AR-B1462, or you only have installed SRAM that does not start from MEM1 socket, the AR-B1462 will simulate two disk drives. The drive numbers respect to those switch settings when AR-B1462 simulates two disk drives.

SW1-4	SW1-5	Occupies floppy disk number	
		FLASH (EPROM)	SRAM
OFF	OFF	0 or 1 (Note 1)	2
ON	OFF	0 or 2 (Note 2)	3
OFF	ON	0	1
ON	ON	0	2

Table 6-4 SSD Drive Number for Simulate 2 Disk Drive

NOTE: 1. If there is no DOS on this SSD, the disk number will be 1 (B:). If any DOS is found by the AR-B1462 SSD BIOS, the disk letter will be 0 (A:). But, you can change the disk number from 0 to 1 by pressing the <ESC> key during system bootup.

2. If there is no DOS on this SSD, the disk number will be 2 (C: or D: or ...). If any DOS is found by the AR-B1462 SSD BIOS, the disk number will be 0 (A:). But, you can change the disk number from 0 to 2 by pressing the <ESC> key during system bootup.

(2) Disk Drive Name Arrangement

If any logical hard disk drives exist in your system, there will also be a different disk number depending on which version DOS you are using.

The solid state disk drive number with there respective DOS drive designation are listed in table as follows. The solid state disk drive number is changeable as the DOS version. The following table expresses the variety.

Condition	Floppy disk No.				Logical hard disk			
	0	1	2	3	1	2	3	4
No Logical hard disk	A:	B:	C:	D:	--	--	--	--
1 Logical hard disk	A:	B:	C:	D:	E:	--	--	--
2 Logical hard disk	A:	B:	C:	D:	E:	F:	--	--
3 Logical hard disk	A:	B:	C:	D:	E:	F:	G:	--
4 Logical hard disk	A:	B:	C:	D:	E:	F:	G:	H:

Table 6-5 SSD Drive Number for DOS Version before 5.0

Condition	Floppy disk No.				Logical hard disk			
	0	1	2	3	1	2	3	4
No Logical hard disk	A:	B:	C:	D:	--	--	--	--
1 Logical hard disk	A:	B:	D:	E:	C:	--	--	--
2 Logical hard disk	A:	B:	E:	F:	C:	D:	--	--
3 Logical hard disk	A:	B:	F:	G:	C:	D:	E:	--
4 Logical hard disk	A:	B:	G:	H:	C:	D:	E:	F:

Table 6-6 SSD Drive Number for DOS Version 5.0 and Newer

6.2.5 ROM Type Select (SW1-6 & SW1-7)

SW1-6 & SW1-7 are used to select the memory type of ROM disk section.

SW1-6	SW1-7	EPROM Type
OFF	OFF	UV EPROM (27Cxxx)
ON	OFF	5V FLASH 29Fxxx (*Note)
OFF	ON	5V FLASH (29Cxxx & 28Eexxx)
ON	ON	12V FLASH (28Fxxx)

Table 6-7 ROM Type Select

NOTE: It is also used to perform the hardware write protection of small page 5V FLASH (29Cxxx or 28Eexxx) disk.

6.2.6 Serial Port 1 Mode Select (SW1-8)

SW1-8 is used to select the interface mode of serial port 1.

SW1-8	Serial Port 1
OFF	RS-232C (*)
ON	TTL

Table 6-8 Serial Port 1 Mode Select

6.2.7 Serial Port 2 Mode Select (SW1-9 & SW1-10)

SW1-9 & SW1-10 are used to select the interface mode of serial port2.

SW1-9	SW1-10	Serial port 2
OFF	OFF	RS-232C (*)
ON	OFF	RS-422
OFF	ON	RS-485 mode1 (Note 1)
ON	ON	RS-485 mode2 (Note 2)

Table 6-9 Serial Port 2 Mode Select

When RS-422 or RS-485 mode is selected, you also need to change M5 to select between RS-422 or RS-485 mode.

NOTE: 1. The recommended configuration for RS-485 interface is to set the transmitter to be controlled by DTR and set the receiver to the inverse state of the transmitter. Receiver is disabled.

2. The receiver is always enabled, so you will receive data that you transmitted previously. It is not recommended to use this setting as RS-485 interface.

6.3 JUMPER SETTING

Before installing the memory into memory sockets MEM1 through MEM4, you have to configure the memory type which will be used (ROM/RAM) on the AR-B1462. Each socket is equipped with a jumper to select the memory type.

You can configure the AR-B1462 as a (FLASH) EPROM disk (ROM only), a SRAM disk (SRAM only) or a combination of (FLASH) EPROM and SRAM disk.

It is not necessary to insert memory chips into all of the sockets. The number of SRAM chips required depends on your RAM disk capacity. The number of EPROM chips required depends on the total size of files that you plan to copy onto the ROM disk and whether or not it will be bootable.

Insert the first memory chip into MEM1 if you are going to configure it as a ROM or SRAM disk. If you use a combination of ROM and RAM, then insert the (FLASH) EPROM chip starting with the MEM1, and insert the SRAM chips starting from the first socket which is configured as SRAM.

- M1:is used to configure the memory type of MEM1
- M2:is used to configure the memory type of MEM2
- M3:is used to configure the memory type of MEM3
- M4:is used to configure the memory type of MEM4

CAUTION: When the power is turned off, please note the following precautions.

1. If your data has been stored in the SRAM disk, do not change the jumper position or data will be lost.

2. Make sure jumpers are set properly. If you mistakenly set the jumpers for SRAM and you have EPROM or FLASH installed, the EPROM or FLASH will drain the battery's power.

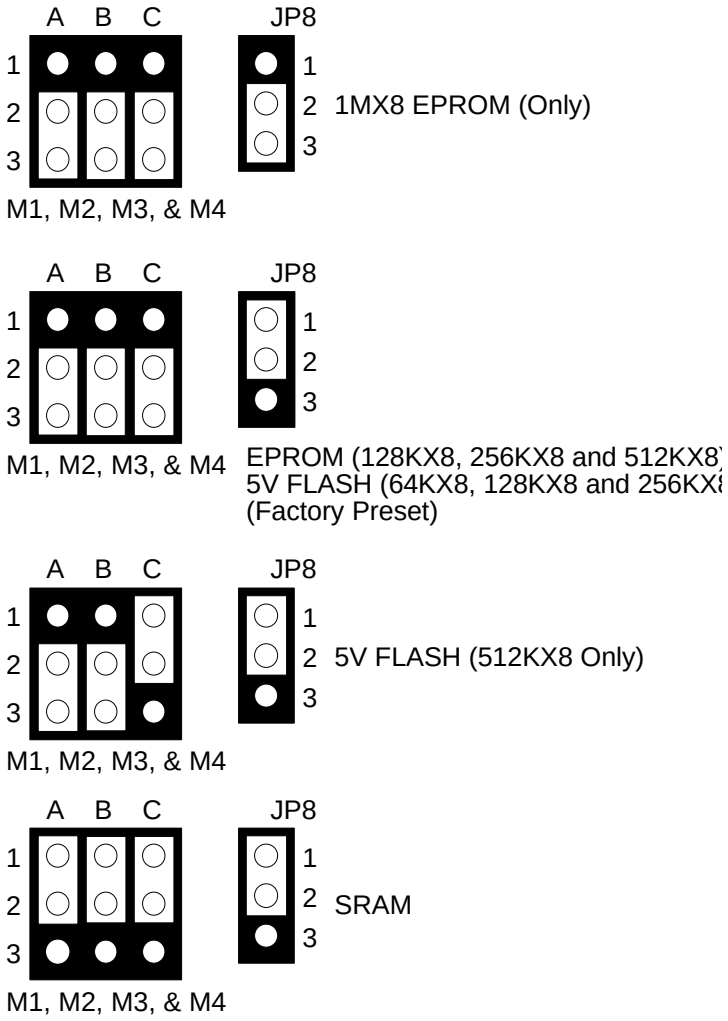


Figure 6-3 M1~M4 & JP8: Memory Type Setting

6.4 ROM DISK INSTALLATION

The section describes the various type SSDs' installation steps as follows. The jumper and switch adjust as SSD's different type to set.

6.4.1 UV EPROM (27Cxxx)

(2) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and EPROM type on SW1.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

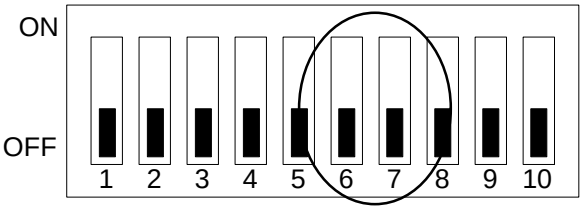
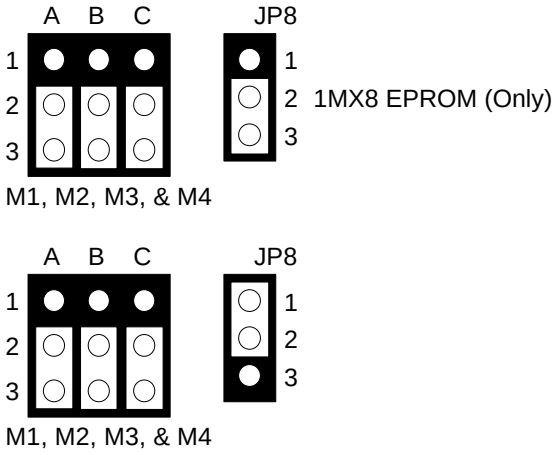


Figure 6-4 UV EPROM (27CXXX) Switch Setting



EPROM (128KX8, 256KX8 and 512KX8)

Figure 6-5 UV EPROM Jumper Setting

(2) Software Programming

Use the UV EPROM, please refer to the follow steps:

Step 1: Turn on the power and boot DOS from hard disk drive or floppy disk drive.

Step 2: Making a Program Group File (*.PGF file)

Step 3: Using the RFG.EXE to generate ROM pattern files, and counting the ROM numbers as the pattern files.

Step 4: In the DOS prompt type the command as follows.

```
C:\>RFG [file name of PGF]
```

Step 5: In the RFG.EXE main menu, choose the <Load PGF File> item, that is user editing *.PGF file.

Step 6: Choose the <Generate ROM File(s)>, the tools program will generate the ROM files, for programming the EPROMs.

Step 7: Program the EPROMs

Using the instruments of the EPROM writer to load and write the ROM pattern files into the EPROM chips. Make sure that the EPROMs are verified by the program without any error.

Step 8: Install EPROM chips

Be sure to place the programmed EPROMs (R01, R02 ….) into socket starting from MEM1 and ensure that the chips are installed in the sockets in the proper orientation.

6.4.2 Large Page 5V FLASH Disk

If you are using large page 5V FLASH as ROM disk, it is the same procedure as step 1 to step 4 of using the UV EPROM.

(2) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and large page 5V FLASH type on SW1.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

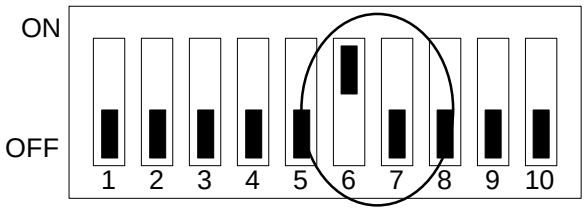
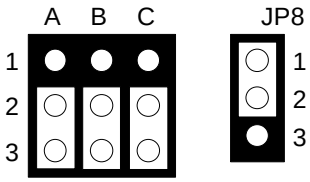
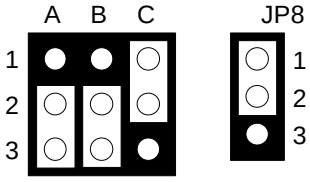


Figure 6-6 5V Large FLASH (29FXXX) Switch Setting



M1, M2, M3, & M4

5V FLASH (64KX8, 128KX8 and 256KX8)
(Factory Preset)



5V FLASH (512KX8 Only)

M1, M2, M3, & M4

Figure 6-7 Large Page 5V FLASH Jumper Setting

(2) Software Programming

And then, you should create a PGF and generate ROM pattern files by using the RFG.EXE.

Step 1: Making a Program Group File (*.PGF file)

Step 2: Generate ROM pattern files

Step 3: Turn off your system, and then install FLASH EPROMs into the sockets.

NOTE: Place the appropriate number of FLASH EPROM chips (the numbers depends on the ROM pattern files generated by RFG.EXE) into the socket starting from MEM1 and ensure that the chips are installed in the sockets in the proper orientation. Line up and insert the AR-B1462 board into any free slot of your computer.

Step 4: Turn on your system, and Program FLASH EPROMs.

NOTE: The FLASH EPROM program is built-in the AR-B1462 board. The FLASH EPROMs can be programmed on the AR-B1462. Before programming the FLASH EPROMs, please insert at least the same number of FLASH EPROMs, please insert at least the same number of FLASH EPROMs, please insert at least the same number of FLASH chips as the ROM pattern files generated.

Step 5: The PGM1462.EXE file is a program that loads and writes the ROM pattern files onto the (FLASH) memory chips. To program the FLASH EPROM.

Step 6: In the DOS prompt type the command as follows.

```
C:\>PGM1462 [ROM pattern file name]
```

Step 7: In the main menu, choose the <Load ROM File> item, that is the ROM_NAME=[file name] in the *.PGF file.

Step 8: Choose the <Program Memory> item, this item program will program the EPROMs.

NOTE: Move the reverse video bar to the <Program memory> option then press <ENTER>.

Step 9: Reboot the system

NOTE: Reboot your computer by making a software or hardware reset.

6.4.3 Small Page 5V FLASH ROM Disk

(1) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number and EPROM type on SW1.

Step 3: Insert programmed EPROM(s) or FLASH(s) chips into sockets starting at MEM1.

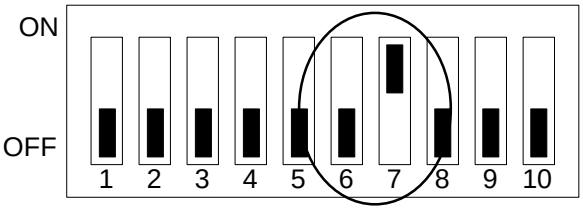
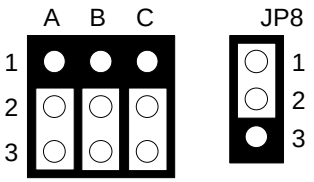


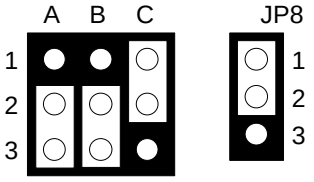
Figure 6-8 5V FLASH (29CXXX & 28EEXXX) Switch Setting



M1, M2, M3, & M4

(Factory Preset)

5V FLASH (64KX8, 128KX8 and 256KX8)



M1, M2, M3, & M4

5V FLASH (512KX8 Only)

Figure 6-9 5V FLASH (29CXXX & 28EEXXX) Jumper Setting

(2) Using Tool Program

If small page 5V FLASH EPROMs are used, it is the same procedure as step 1 to step 4 of using the UV EPROM:

Step 1: Making a Program Group File (*.PGF file)

Step 2: Generating ROM pattern files

Step 3: Installing FLASH EPROMs

Step 4: Programming FLASH EPROMs

Step 5: Reboot system

(3) Typing DOS Command

You can use another way to format and copy files to the 5V FLASH EPROM. This method provides the convenience of using a RAM disk. You can use the DOS <FORMAT> and <COPY> command to format and copy files. Follow the following steps to format and copy files to the FLASH disk. it is the same procedure as step 1 to step 4 of using the UV EPROM.

Step 1: Turn on your computer, when the screen shows the SSD BIOS menu, please hit the [F1] key during the system boot-up, this enables you to enter the FLASH setup program. If the program does not show up, check the switch setting of SW1.

Step 2: Use <Page-Up>, <Page-Down>, <Right>, and <Left> arrow keys to select the correct FLASH memory type and how many memory chips are going to be used.

Step 3: Press the [F4] key to save the current settings.

Step 4: After the DOS is loaded, use the DOS [FORMAT] command to format the FLASH disk.

To format the disk and copy DOS system files to the disk.

```
C:\>FORMAT [ROM disk letter] /S /U
```

To format the disk without copying DOS system files.

```
C:\>FORMAT [ROM disk letter] /U
```

Step 5: Copy your program or files to the FLASH disk by using DOS [COPY] command.

CAUTION: It is not recommended that the user formatted the disk and copy files to the FLASH disk very often. Since the FLASH EPROM's write cycle life time is about 10,000 or 100,000 times, writing data to the FLASH too often will reduce the life time of the FLASH EPROM chips, especially the FLASH EPROM chip in the MEM1 socket.

6.4.4 RAM Disk

(1) Switch and Jumper Setting

Step 1: Use jumper block to set the memory type as ROM (FLASH).

Step 2: Select the proper I/O base port, firmware address, disk drive number on SW1.

Step 3: Insert programmed SRAM chips into sockets starting at MEM1.

NOTE: If you use the SRAM, please skip the SW1-6 & SW1-7 setting.

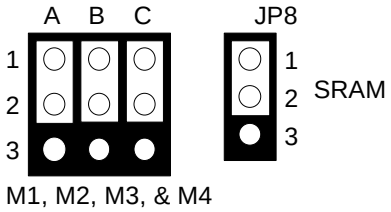


Figure 6-10 SRAM Jumper Setting

(2) Software Programming

It is very easy to use the RAM disk. The RAM disk operates just like a normal floppy disk. A newly installed RAM disk needs to be formatted before files can be copied to it. Use the DOS command [FORMAT] to format the RAM disk.

Step 1: Use jumper block to select the memory type as SRAM refer.

Step 2: Select the proper I/O base port, firmware address and disk drive number on SW1.

Step 3: Insert SRAM chips into sockets starting from MEM1

Step 4: Turn on power and boot DOS from hard disk drive or floppy disk drive.

Step 5: Use the DOS command [FORMAT] to format the RAM disk. If you are installing SRAM for the first time.
To format the RAM disk and copy DOS system files onto the RAM disk.

```
C:\>FORMAT [RAM disk letter] /S /U
```

To format the RAM disk without copying DOS system files into the RAM disk.

```
C:\>FORMAT [RAM disk letter] /U
```

Step 6: Use the DOS command [COPY] to copy files onto the RAM disk. For example, if you want to copy file <EDIT.EXE> to the RAM disk from drive C: and the RAM disk is assigned as drive A:.

```
COPY C:EDIT.EXE A:
```

NOTE: In addition, you can use any other DOS command to operate the RAM disk.

6.4.5 Combination of ROM and RAM Disk

The AR-B1462 can be configured as a combination of one ROM disk and one RAM disk. Each disk occupies a drive unit.

Step 1: Use jumper block to select the proper ROM/RAM configuration you are going to use.

Step 2: Insert the first programmed EPROM into the socket mem1, the second into the socket MEM2, etc.

Step 3: Insert the SRAM chips starting from the first socket assigned as SRAM.

Step 4: Select the proper I/O base port, firmware address and disk drive number on SW1.

Step 5: Turn on power and boot DOS from hard disk drive or floppy disk drive.

Step 6: Use the DOS command [FORMAT] to format the RAM disk.

```
C:\>FORMAT [RAM disk letter] /U
```

Step 7: If 5V FLASH (small page) is being used for the first time.
And then use the DOS command [FORMAT] to format the FLASH disk.

Step 8: If large page 5V FLASH is being installed for the first time, please use the FLASH programming utility RFG.EXE to program ROM pattern files.

NOTE: Users can only boot DOS from the ROM disk drive if the AR-B1462 is configured as a ROM and a RAM disk. You don't need to copy DOS onto the RAM disk.

6.5 DISKONCHIP INSTALLATION

The DiskOnChip is a new generation of high performance single-chip Flash Disk. It provides a Flash Disk in a standard 32-pin DIP package.
This unique data storage solution offers a better, faster, and more cost-effective Flash Disk for Single Board embedded systems. The DiskOnChip provides a Flash Disk that does not require any bus, slot or connector. Simply insert the DiskOnChip into 32-pin socket MEM4 position on the CPU board. It is the optimal solution for single board computers, it is a small, fully functional, easy to integrate, plug-and-play Flash Disk with a very low power consumption.
The DiskOnChip is fully tested and formatted before the product is shipped.

(1) DiskOnChip Hardware Installation

Step 1: Make sure the target platform is powered OFF

Step 2: Use JP7 to select the correct D.O.C. socket.

Step 3: Plug the DiskOnChip device into the MEM4 socket. Verify the direction is correct (pin 1 of the DiskOnChip is aligned with pin 1 of the MEM4 socket)

Step 4: Line up and insert the AR-B1462 card into any free slot of your computer.

Step 5: Power up the system

Step 6: During power up you may observe the messages displayed by the DiskOnChip when its drivers are automatically loaded into system's memory

Step 7: At this stage the DiskOnChip can be accessed as any disk in the system

Step 8: If the DiskOnChip is the only disk in the system, it will appear as the first disk (drive C: in DOS)

Step 9: If there are more disks besides the DiskOnChip, it will appear by default as the last drive, unless it was programmed as first drive.

Step 10: If you want the DiskOnChip to be bootable, copy the operating system files into the DiskOnChip by using the standard DOS command.

(2) DiskOnChip Memory Address Setting (JP7)

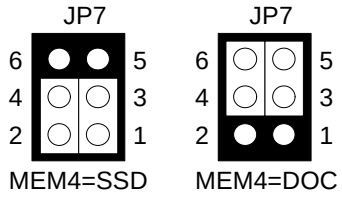


Figure 6-11 JP7: DiskOnChip Memory Address Setting

(3) Configuring the DiskOnChip as a Bootable Disk

The DiskOnChip fully supports the BOOT capability. In order for the DiskOnChip to be bootable, it should be DOS formatted as bootable, like any floppy or hard disk that required to be booted.

SYS D: Change the disk into bootable (assuming the DiskOnChip is disk D)

7. BIOS CONSOLE

This chapter describes the AR-B1462 BIOS menu displays and explains how to perform common tasks needed to get up and running, and presents detailed explanations of the elements found in each of the BIOS menus. The following topics are covered:

- BIOS Setup Overview
- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Password Setting
- Load Default Setting
- BIOS Exit
- BIOS Update

7.1 BIOS SETUP OVERVIEW

BIOS is a program used to initialize and set up the I/O system of the computer, which includes the ISA bus and connected devices such as the video display, diskette drive, and the keyboard.

The BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The BIOS Default Values ensure that the system will function at its normal capability. In the worst situation the user may have corrupted the original settings set by the manufacturer.

After the computer turned on, the BIOS will perform a diagnostics of the system and display the size of the memory that is being tested. Press the [Del] key to enter the BIOS Setup program, and then the main menu will show on the screen.

The BIOS Setup main menu includes some options. Use the [Up/Down] arrow key to highlight the option that you wish to modify, and then press the [Enter] key to assure the option and configure the functions.

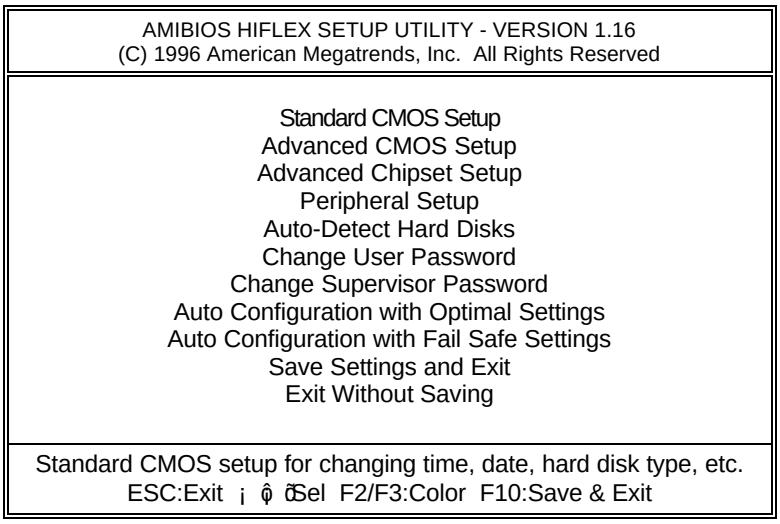


Figure 7-1 BIOS: Setup Main Menu

CAUTION: 1. AR-B1462 BIOS the factory-default setting is used to the <Auto Configuration with Optimal Settings> Acrosser recommends using the BIOS default setting, unless you are very familiar with the setting function, or you can contact the technical support engineer.

2. If the BIOS loss setting, the CMOS will detect the <Auto Configuration with Fail Safe Settings> to boot the operation system, this option will reduce the performance of the system. Acrosser recommends choosing the <Auto Configuration with Optimal Setting> in the main menu. The option is best-case values that should optimize system performance.
3. The BIOS settings are described in detail in this section.

7.2 STANDARD CMOS SETUP

The <Standard CMOS Setup> option allows you to record some basic system hardware configuration and set the system clock and error handling. If the CPU board is already installed in a working system, you will not need to select this option anymore.

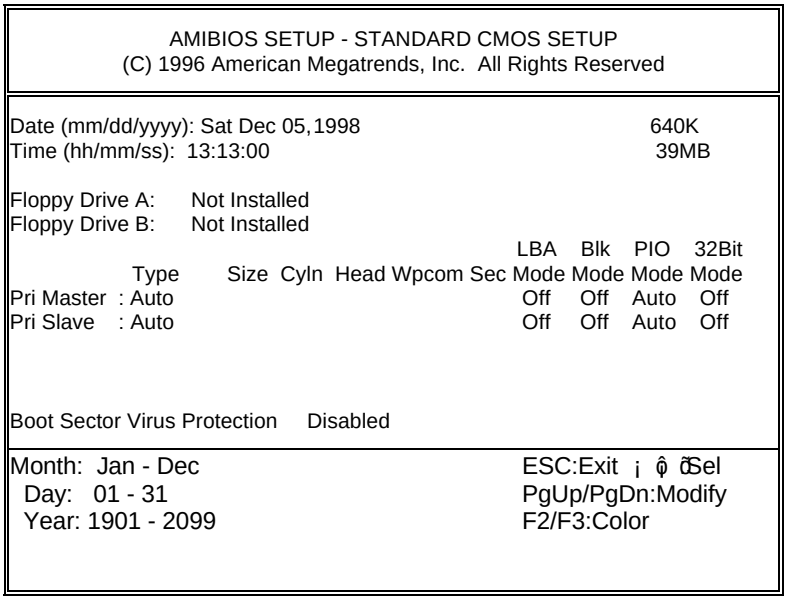


Figure 7-2 BIOS: Standard CMOS Setup

Date & Time Setup

Highlight the <Date> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the month, day and year format.

Highlight the <Time> field and then press the [Page Up] /[Page Down] or [+]/[-] keys to set the current date. Follow the hour, minute and second format.

The user can bypass the date and time prompts by creating an AUTOEXEC.BAT file. For information on how to create this file, please refer to the MS-DOS manual.

Floppy Setup

The <Standard CMOS Setup> option records the types of floppy disk drives installed in the system.

To enter the configuration value for a particular drive, highlight its corresponding field and then select the drive type using the left-or right-arrow key.

Hard Disk Setup

The BIOS supports various types for user settings, The BIOS supports <Pri Master> and <Pri Slave> so the user can install up to two hard disks. For the master and slave jumpers, please refer to the hard disk's installation descriptions and the hard disk jumper settings.

You can select <AUTO> under the <TYPE> and <MODE> fields. This will enable auto detection of your IDE drives during bootup. This will allow you to change your hard drives (with the power off) and then power on without having to reconfigure your hard drive type. If you use older hard disk drives which do not support this feature, then you must configure the hard disk drive in the standard method as described above by the <USER> option.

Boot Sector Virus Protection

This option protects the boot sector and partition table of your hard disk against accidental modifications. Any attempt to write to them will cause the system to halt and display a warning message. If this occurs, you can either allow the operation to continue or use a bootable virus-free floppy disk to reboot and investigate your system. The default setting is ***<Disabled>***. This setting is recommended because it conflicts with new operating systems. Installation of new operating system requires that you disable this to prevent write errors.

7.3 ADVANCED CMOS SETUP

The <Advanced CMOS SETUP> option consists of configuration entries that allow you to improve your system performance, or let you set up some system features according to your preference. Some entries here are required by the CPU board$ design to
remained in their default settings.

AMIBIOS SETUP - ADVANCED CMOS SETUP
(C) 1996 American Megatrends, Inc. All Rights Reserved

BootUp Sequence	C:,A:,CDROM	Available Options :
BootUp Num-Lock	On	C:, A:. CDROM
Floppy Drive Swap	Disabled	A:, C:, CDROM
Floppy Drive Seek	Disabled	CDROM, A:, C:
Mouse Support	Enabled	
Typematic Rate	Fast	
System Keyboard	Present	
Primary Display	VGA/EGA	
Password Check	Setup	
Wait For 'F1' If Error	Enabled	
Hit 'DEL' Message Display	Enabled	
Internal Cache	WriteBack	
External Cache	WriteThru	
System BIOS Cacheable	Enabled	
Hard disk Delay	3 Sec	
C000, 16k Shadow	Enabled	
C400, 16k Shadow	Enabled	
C800, 16k Shadow	Disabled	
CC00, 16k Shadow	Disabled	
D000, 16k Shadow	Disabled	
D400, 16k Shadow	Disabled	ESC:Exit ¡ ô õSel
D800, 16k Shadow	Disabled	PgUp/PgDn:Modify
DC00, 16k Shadow	Disabled	F2/F3:Color

Figure 7-3 BIOS: Advanced CMOS Setup

BootUp Sequence

The option determines where the system looks first for an operating system.

BootUp Num-Lock

This item is used to activate the Num-Lock function upon system boot. If the setting is on, after a boot, the Num-Lock light is lit, and user can use the number key.

Floppy Drive Swap

The option reverses the drive letter assignments of your floppy disk drives in the Swap A, B setting, otherwise leave on the default setting of ***Disabled*** (No Swap). This works separately from the BIOS Features floppy disk swap feature. It is functionally the same as physically interchanging the connectors of the floppy disk drives. When the setting is <***Enabled>***, the BIOS will be swapped floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A under DOS.

Floppy Drive Seek

If the <Floppy Drive Seek> item is setting ***Enabled***, the BIOS will seek the floppy <A> drive one time upon bootup.

Mouse Support

The setting of ***Enabled*** allows the system to detect a PS/2 mouse on bootup. If detected, IRQ12 will be used for the PS/2 mouse. IRQ 12 will be reserved for expansion cards if a PS/2 mouse is not detected. ***Disabled*** will reserve IRQ12 for expansion cards and therefore the PS/2 mouse will not function.

Typematic Rate

This item specifies the speed at which a keyboard keystroke is repeated.

System Keyboard

This function specifies that a keyboard is attached to the computer.

Primary Display

The option is used to set the type of video display card installed in the system.

Password Check

This option enables password checking every time the computer is powered on or every time the BIOS Setup is executed. If ***Always*** is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if the BIOS executed.

Wait for 'F1' If Error

AMIBIOS POST error messages are followed by:

```
Press <F1> to continue
```

If this option is set to ***Disabled***, the AMIBIOS does not wait for you to press the <F1> key after an error message.

Hit 'DEL' Message Display

Set this option to ***Disabled*** to prevent the message as follows:

```
Hit 'DEL' if you want to run setup
```

It will prevent the message from appearing on the first BIOS screen when the computer boots.

Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 7-1 Internal Cache Setting

External Cache

This option specifies the caching algorithm used for L2 secondary (external) cache memory. The settings are:

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack	Use the write-back caching algorithm.
WriteThru	Use the write-through caching algorithm.

Table 7-2 External Cache Setting

System BIOS Cacheable

When this option is set to ***Enabled***, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are ***Enabled*** or ***Disabled***. The Optimal default setting is ***Enabled***. The Fail-Safe default setting is ***Disabled***.

Shadow

These options control the location of the contents of the 32KB of ROM beginning at the specified memory location. If no adapter ROM is using the named ROM area, this area is made available to the local bus. The settings are:

SETTING	DESCRIPTION
Disabled	The video ROM is not copied to RAM. The contents of the video ROM cannot be read from or written to cache memory.
Enabled	The contents of C000h - C7FFFh are written to the same address in system memory (RAM) for faster execution.
Cached	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adapter ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.

Table 7-3 Shadow Setting

7.4 ADVANCED CHIPSET SETUP

This option controls the configuration of the board's chipset. Control keys for this screen are the same as for the previous screen.

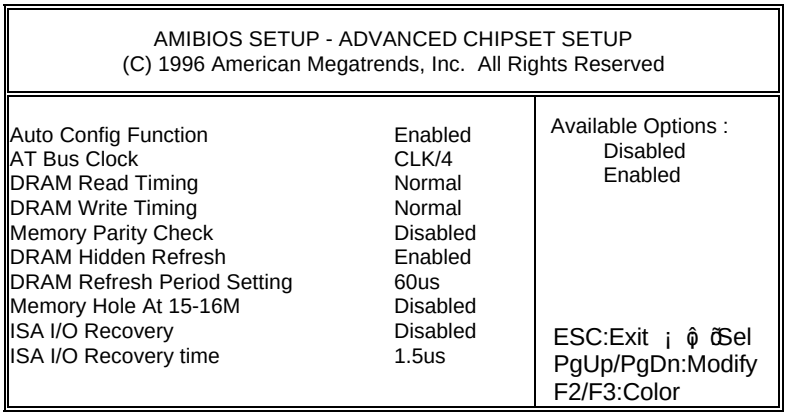


Figure 7-4 BIOS: Advanced Chipset Setup

Automatic Configuration

If selecting a certain setting for one BIOS Setup option determines the settings for one or more other BIOS Setup options, the BIOS automatically assigns the dependent settings and does not permit the end user to modify these settings unless the setting for the parent option is changed. Invalid options are grayed and cannot be selected.

AT Bus Clock

This option sets the polling clock speed of ISA Bus (PC/104).

NOTE: 1. PCLK means the CPU inputs clock.
2. Acrosser recommends user setting at the range of 8MHz to 10MHz.

Memory Parity Check

This option ***Enables*** or ***Disables*** parity is error checking for all system RAM. This option must be ***Disabled*** if the used DRAM SIMMs are 32-bit but not 36-bit devices.

Memory Hole at 15-16 M

This option specifies the range 15MB to 16MB in memory that cannot be addressed on the ISA bus.

ISA I/O Recovery
ISA I/O Recovery Time

These options specify the length of the delay (in BUSCLK) inserted between consecutive 8-bit/16-bit I/O operations.

7.5 PERIPHERAL SETUP

This section is used to configure peripheral features.

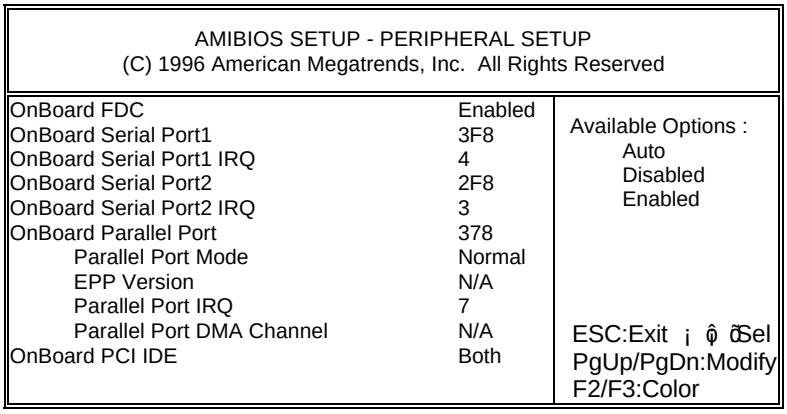


Figure 7-5 BIOS: Peripheral Setup

OnBoard FDC

This option enables the floppy drive controller on the AR-B1462.

OnBoard Serial Port

This option enables the serial port on the AR-B1462.

OnBoard Parallel Port

This option enables the parallel port on the AR-B1462.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications.

Parallel Port DMA Channel

This option is only available if the setting for the parallel Port Mode option is ECP.

OnBoard PCI IDE/IDE Prefetch

This option specifies the onboard IDE controller channels that will be used.

7.6 AUTO-DETECT HARD DISKS

This option detects the parameters of an IDE hard disk drive, and automatically enters them into the Standard CMOS Setup screen.

7.7 PASSWORD SETTING

This BIOS Setup has an optional password feature. The system can be configured so that all users must enter a password every time the system boots or when BIOS Setup is executed. User can set either a Supervisor password or a User password.

7.7.1 Setting Password

Select the appropriate password icon (Supervisor or User) from the Security section of the BIOS Setup main menu. Enter the password and press [Enter]. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press [Enter].

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press [Esc] to return to the BIOS Main Menu. The password is stored in CMOS RAM after BIOS completes. The next time the system boots, you are prompted for the password function is present and is enabled.

```
Enter new supervisor password:
```

7.7.2 Password Checking

The password check option is enabled in Advanced Setup by choosing either ***Always*** (the password prompt appears every time the system is powered on) or ***Setup*** (the password prompt appears only when BIOS is run). The password is stored in CMOS RAM. User can enter a password by typing on the keyboard. As user select Supervisor or User. The BIOS prompts for a password, user must set the Supervisor password before user can set the User password. Enter 1-6 character as password. The password does not appear on the screen when typed. Make sure you write it down.

7.8 LOAD DEFAULT SETTING

In this section permit user to select a group of setting for all BIOS Setup options. Not only can you use these items to quickly set system configuration parameters, you can choose a group of settings that have a better chance of working when the system is having configuration related problems.

7.8.1 Auto Configuration with Optimal Setting

User can load the optimal default settings for the BIOS. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the optimal settings are loaded automatically.

```
Load high performance settings (Y/N) ?
```

7.8.2 Auto Configuration with Fail Safe Setting

User can load the Fail-Safe BIOS Setup option settings by selecting the Fail-Safe item from the Default section of the BIOS Setup main menu.
The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

```
Load failsafe settings (Y/N) ?
```

7.9 BIOS EXIT

This section is used to exit the BIOS main menu in two types situation. After making your changes, you can either save them or exit the BIOS menu and without saving the new values.

7.9.1 Save Settings and Exit

This item set in the <Standard CMOS Setup>, <Advanced CMOS Setup>, <Advanced Chipset Setup> and the new password (if it has been changed) will be stored in the CMOS. The CMOS checksum is calculated and written into the CMOS.

As you select this function, the following message will appear at the center of the screen to assist you to save data to CMOS and Exit the Setup.

```
Save current settings and exit (Y/N) ?
```

7.9.2 Exit Without Saving

When you select this option, the following message will appear at the center of the screen to help to Abandon all Data and Exit Setup.

```
Quit without saving (Y/N) ?
```

7.10 BIOS UPDATE

The BIOS program instructions are contained within computer chips called FLASH ROMs that are located on your system board. The chips can be electronically reprogrammed, allowing you to upgrade your BIOS firmware without removing and installing chips.

The AR-B1462 BIOS provides a menu-based interface to the console subsystem. The console subsystem contains special software, called firmware that interacts directly with the hardware components and facilitates interaction between the system hardware and the operating system.

The AR-B1462 provides FLASH BIOS update function for you to easily upgrade newer BIOS version. Please follow the operating steps for updating new BIOS:

Step 1: Insert the FLASH BIOS diskette into the floppy disk drive.

Step 2: Turn on your system and press [Ctrl]+[Home[(Hit the [Ctrl] key and [Home] key simultaneously just powered on. Then the onboard BIOS will read new BIOS file named and AMIBOOT.ROM from floppy drive and write to FLASH.

Step 3: If all steps is correctly, the system will reboot. But the system did not boot up, please check everything and try again. If still not work, please contact your Acrosser distributor for technology supports at once.

NOTE: 1. After turn on the computer and the system didn't detect the boot procedure, please press the [Ctrl]+[Home] key immediately. The system will detect the BIOS file from floppy drive.

2. The BIOS Flash disk is not the standard accessory. It supports to add some functions, if it is necessary to update in the future. User can download the suitable BIOS. The address is as follows:

http:\\www.acrosser.com

8. SPECIFICATIONS & SSD TYPES SUPPORTED

8.1 SPECIFICATIONS

CPU:	Supports25 to 133 Mhz Intel / AMD / Cyrix / ST / IBM 486 CPU .
Chipset:	ALI M1489/M1487 and C & T 65545
Bus Interface:	ISA (PC/AT) and non-stack through PC/104 bus
RAM Memory:	Supports FPM/EDO RAM, 72 MB maximum (8MB on-board and one 72-pin SIMMs w/o DRAM)
Cache Size:	512KB for standard
VGA/LCD Display:	AR-B1462: 1 MB VRAM (PCI bus, 1024X768/256 colors) ARB1462A: 2 MB VRAM (PCI bus, 1024X768/256 colors)
HDC:	One PCI IDE Supports LBA/Block mode access
FDC:	Supports two 5.25" or 3.5" floppy disk drives
Parallel Port:	1 bi-directional centronics type parallel port Supports SPP/EPP/ECP mode
Serial Port:	1 RS-232C and 1 RS-232C/RS-485
Keyboard:	PC/AT compatible keyboard
Watchdog:	Programmable watchdog timer 3 to 42 seconds time interval
Speaker:	On-board Buzzer and external speaker
Real Time Clock:	BQ3287MT or compatible chips with 128 bytes data RAM
BIOS:	AMI Flash BIOS (128KB, including VGA BIOS)
Flash Disk:	Supports 1 DiskOnChip socket
BUS Drive Cap.:	15 TTL level loads maximum
CE Design-In:	Add EMI components to COM ports, parallel port, CRT, keyboard, and PS/2 mouse
Indicator:	Power LED, and watchdog LED
Power Req.:	+5V only, 2.0A maximum (base on Intel DX4-100)
PC Board:	8 layers, EMI considered
Dimensions:	185 mmX122mm (7.29"X4.80")

8.2 SSD TYPES SUPPORTED

The following list contains SRAMs supported by the AR-B1462:

AKM	AKM628128	(128Kx8, 1M bits)
HITACHI	HM628128	(128Kx8, 1M bits)
NEC	UPD431000A	(128Kx8, 1M bits)
SONY	CXK581000P/M	(128Kx8, 1M bits)
HITACHI	HM628512	(512Kx8, 4M bits)
NEC	UPD434000	(512Kx8, 4M bits)
SONY	CXK584000P/M	(512Kx8, 4M bits)

The following list contains large page 5V FLASHs supported by the AR-B1462:

AMD	Am29F512	(64Kx8, 512K bits)
AMD	Am29F010	(128Kx8, 1M bits)
AMD	Am29F020	(256Kx8, 2M bits)
AMD	Am29F040	(512Kx8, 4M bits)

The following list contains small page 5V FLASHs supported by the AR-B1462:

ATMEL	AT29C512	(64Kx8, 512K bits)
SST	PH29EE512	(64Kx8, 512K bits)
ATMEL	AT29C010	(128Kx8, 1M bits)

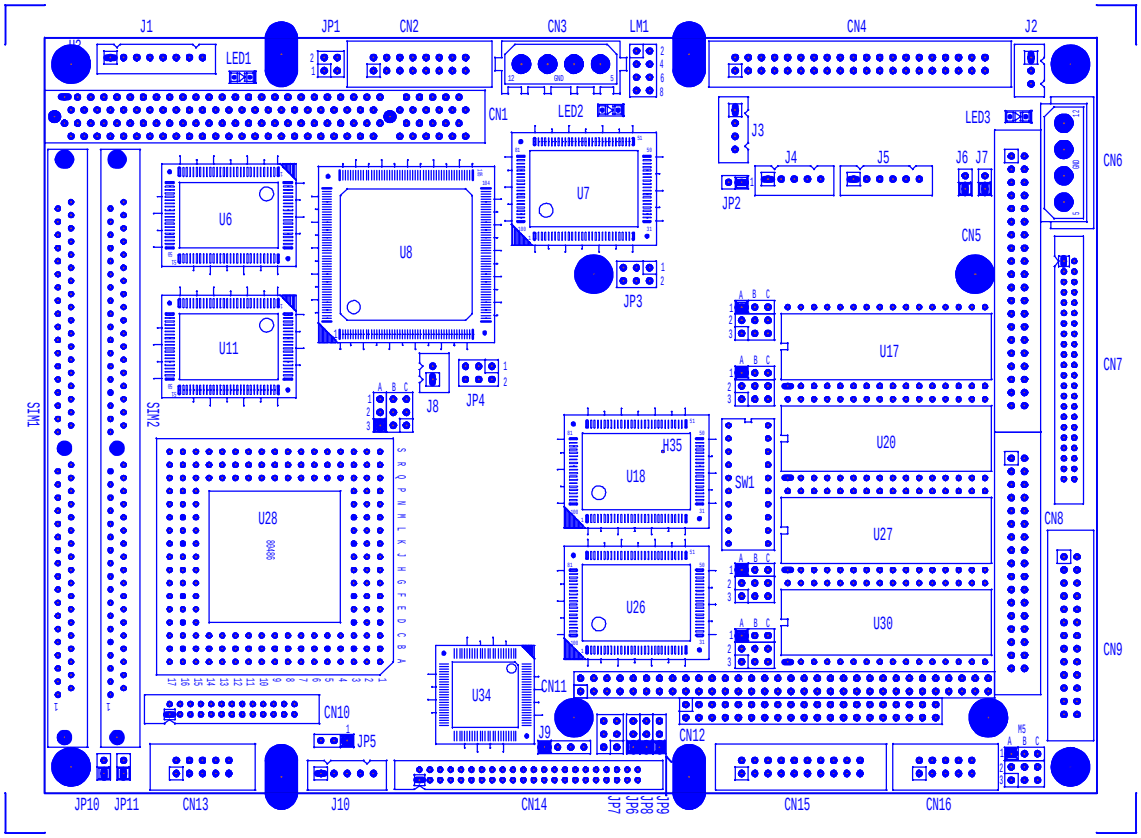
SST	28EE010	(128Kx8, 1M bits)
SST	28EE011	(128Kx8, 1M bits)
SST	PH29EE010	(128Kx8, 1M bits)
WINBOND	W29EE011	(128Kx8, 1M bits)
ATMEL	AT29C020	(256Kx8, 2M bits)
ATMEL	AT29C040	(512Kx8, 4M bits)
ATMEL	AT29C040A	(512Kx8, 4M bits)
SST	PH28SF040	(512Kx8, 4M bits)

The following list contains EPROMs supported by the AR-B1462:

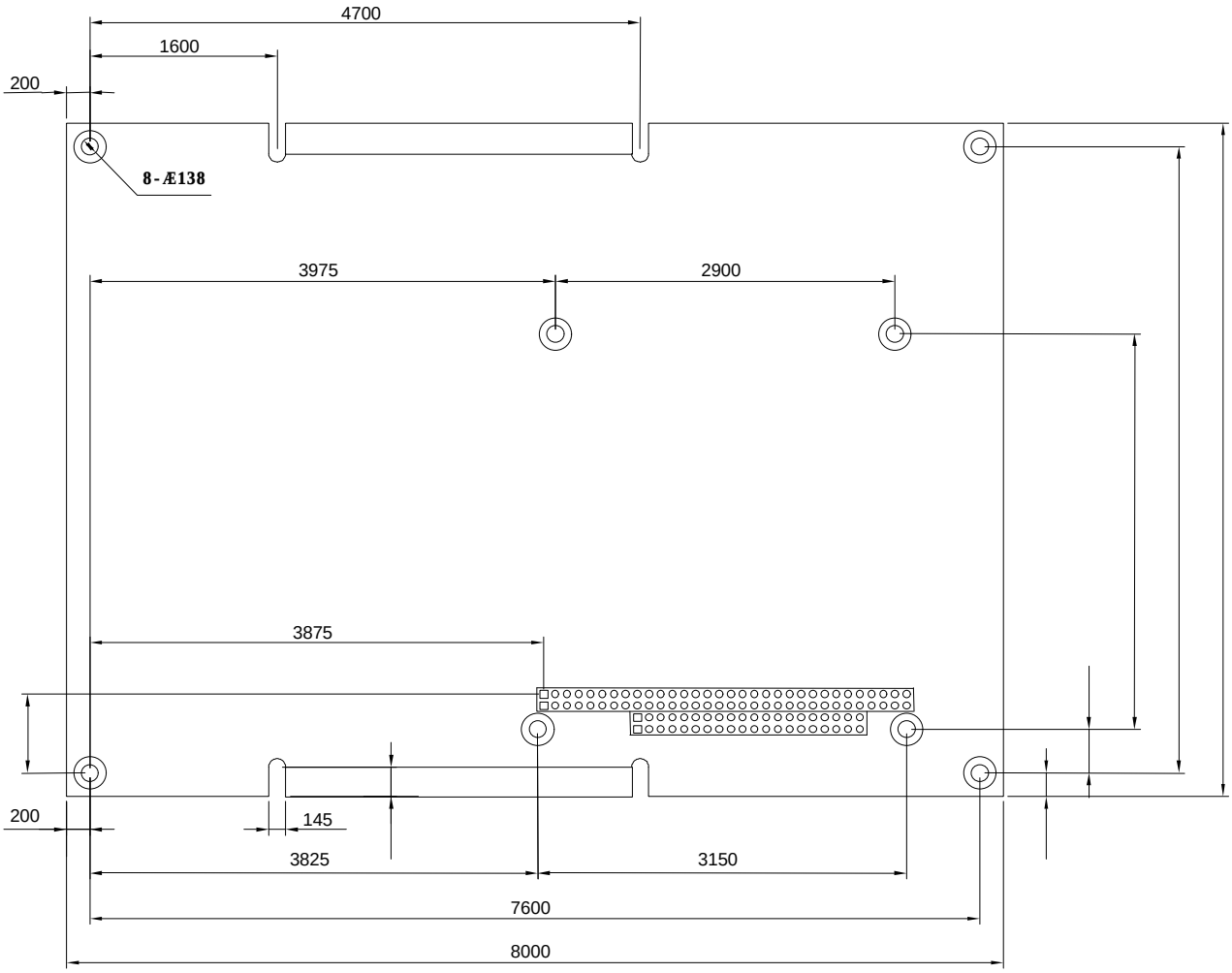
AMD	Am27C010	(128Kx8, 1M bits)
ATMEL	AT27C010	(128Kx8, 1M bits)
FUJITSHU	MBM27C1001	(128Kx8, 1M bits)
HITACHI	HN27C101	(128Kx8, 1M bits)
INTEL	D27C010	(128Kx8, 1M bits)
MITSHUBISHI	M5M27C101	(128Kx8, 1M bits)
NEC	D27C1001	(128Kx8, 1M bits)
NS	NM27C010	(128Kx8, 1M bits)
SGS-THOMSON	M27C1001	(128Kx8, 1M bits)
TI	TMS27C010	(128Kx8, 1M bits)
TOSHIBA	TCS711000	(128Kx8, 1M bits)
AMD	Am27C020	(256Kx8, 2M bits)
ATMEL	AT27C020	(256Kx8, 2M bits)
FUJITSU	MBM27C2001	(256Kx8, 2M bits)
HITACHI	HN27C201	(256Kx8, 2M bits)
INTEL	D27C020	(256Kx8, 2M bits)
MITSHUBISHI	M5M27C201	(256Kx8, 2M bits)
NEC	D27C2001	(256Kx8, 2M bits)
NS	NM27C020	(256Kx8, 2M bits)
SGS-THOMSON	M27C2001	(256Kx8, 2M bits)
TI	TMS27C020	(256Kx8, 2M bits)
TOSHIBA	TCS712000	(256Kx8, 2M bits)
AMD	Am27C040	(512Kx8, 4M bits)
ATMEL	AT27C040	(512Kx8, 4M bits)
FUJITSU	MBM27C4001	(512Kx8, 4M bits)
HITACHI	HN27C401	(512Kx8, 4M bits)
INTEL	D27C040	(512Kx8, 4M bits)
MITSUBISHI	M5M27C401	(512Kx8, 4M bits)
NEC	D27C4001	(512Kx8, 4M bits)
NS	NM27C040	(512Kx8, 4M bits)
SGS-THOMSON	M27C4001	(512Kx8, 4M bits)
TI	TMS27C040	(512Kx8, 4M bits)
TOSHIBA	TCS714000	(512Kx8, 4M bits)
ATMEL	AT27C080	(1Mx8, 8M bits)

9. PLACEMENT & DIMENSIONS

9.1 PLACEMENT



9.2 DIMENSIONS



Unit: mil (1 inch = 25.4 mm = 1000 mil)

10. PROGRAMMING RS-485 & INDEX

10.1 PROGRAMMING RS-485

The majority communicative operation of the RS-485 is in the same of the RS-232. When the RS-485 proceeds the transmission which needs control the TXC signal, and the installing steps are as follows:

Step 1: Enable TXC

Step 2: Send out data

Step 3: Waiting for data empty

Step 4: Disable TXC

NOTE: Please refer to the section of the "Serial Port" in the chapter "System Control" for the detail description of the COM port's register.

(1) Initialize COM port

Step 1: Initialize COM port in the receiver interrupt mode, and /or transmitter interrupt mode. (All of the communication protocol buses of the RS-485 are in the same.)

Step 2: Disable TXC (transmitter control), the bit 0 of the address of offset+4 just sets "0".

NOTE: Control the AR-B1462 CPU card's DTR signal to the RS-485's TXC communication.

(2) Send out one character (Transmit)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write this character to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

(3) Send out one block data (Transmit – the data more than two characters)

Step 1: Enable TXC signal, and the bit 0 of the address of offset+4 just sets "1".

Step 2: Send out the data. (Write all data to the offset+0 of the current COM port address)

Step 3: Wait for the buffer's data empty. Check transmitter holding register (THRE, bit 5 of the address of offset+5), and transmitter shift register (TSRE, bit 6 of the address of offset+5) are all sets must be "0".

Step 4: Disabled TXC signal, and the bit 0 of the address of offset+4 sets "0"

(4) Receive data

The RS-485's operation of receiving data is in the same of the RS-232's.

(5) Basic Language Example

a.) Initial 86C450 UART

```
10      OPEN "COM1:9600,m,8,1" AS #1 LEN=1
20      REM Reset DTR
30      OUT &H3FC, (INP(%H3FC) AND &HFA)
40      RETURN
```

b.) Send out one character to COM1

```
10      REM Enable transmitter by setting DTR ON
20      OUT &H3FC, (INP(&H3FC) OR &H01)
30      REM Send out one character
40      PRINT #1, OUTCHR$
50      REM Check transmitter holding register and shift register
60      IF ((INP(&H3FD) AND &H60) >0) THEN 60
70      REM Disable transmitter by resetting DTR
80      OUT &H3FC, (INP(&H3FC) AND &HEF)
90      RETURN
```

c.) Receive one character from COM1

```
10      REM Check COM1: receiver buffer
20      IF LOF(1)<256 THEN 70
30      REM Receiver buffer is empty
40      INPSTR$"
50      RETURN
60      REM Read one character from COM1: buffer
70      INPSTR$=INPUT$(1,#1)
80      RETURN
```

10.2 INDEX