

**FEATURES**

- RoHS compliant
- Compliant to SFP+ Electrical MSA SFF-8431
- Compliant with SFF-8472 MSA
- Standard LC duplex fiber-optic connector
- I<sup>2</sup>C for integrated Digital Optical Monitoring
- Power consumption < 1W

**Description**

The LCP-10G3A4EDR is a hot pluggable 10Gbps small form factor plus transceiver module integrated with the high performance 850nm VCSEL transmitter, high sensitivity PIN receiver and limiting amplifier for 10Gbps applications. It is compliant with the SFF-8431 SFP+ Electrical Multi-source Agreement (MSA) with five digital monitoring functions: Temperature, Vcc, Tx optical power, Tx laser bias current and Rx received optical power.

**Applications**

- 10G LAN switch
- 10G Ethernet switch/router
- 10G Fiber channel
- SAN applications

**Absolute Maximum Ratings**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	$T_S$	-40		85	°C
Supply Voltage Range @3.3V	$V_{CC3}$	-0.5		3.6	V

**Recommended Operating Conditions**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	$T_C$	-5		+70	°C
Supply Voltage @3.3V	$V_{CC3}$	3.135	3.30	3.465	V
DC Common Mode Voltage	$V_{CM}$	0		3.6	V

**Low Speed Electrical Characteristics**

( $V_{CC}$ =3.135V to 3.465V)

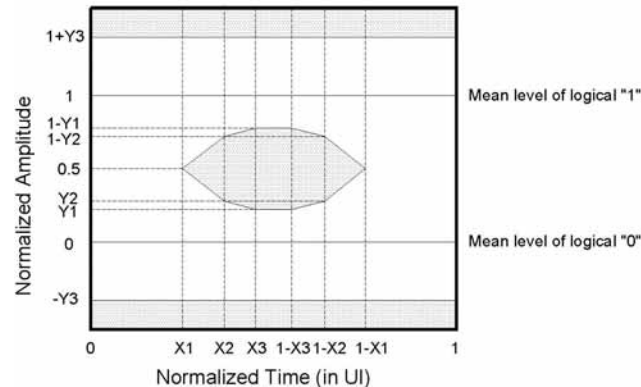
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Total Supply Current	$I_{CC}$			300	mA	
Power Consumption				1	W	
TX_Fault, RX_LOS	$V_{OL}$	0		0.4	V	
	$V_{OH}$	Host_Vcc-0.5		Host_Vcc+0.3	V	
TX_Disable	$V_{IL}$	-0.3		0.8	V	1
	$V_{IH}$	2.0		VccT+0.3	V	1
RS0, RS1	$V_{IL}$	-0.3		0.8	V	2
	$V_{IH}$	2.0		VccT+0.3	V	2

1. Shall be pulled up with 4.7k-10k ohms to VccT in the module.
2. Shall be pulled low to VeeT with a > 30k ohms resistor in the module.

**Optical Transmitter Characteristics ( $T_c = -5^\circ\text{C}$  to  $70^\circ\text{C}$ )**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data Rate	R		10.3125		Gb/s	
Signaling speed variation from nominal.				$\pm 100$	ppm	
Average Output Power	$P_{avg}$	-5		-1.8	dBm	
Wavelength	$\lambda$	840		860	nm	
Spectral Width RMS				0.45	nm	
Transmitter OFF Output Power	$P_{off}$			-30	dBm	
Extinction Ratio	ER	3				
Optical Modulation Amplitude	OMA	Compliant with Minimum OMA relation table			dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss	ORL			12	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.40, 0.45, 0.25, 0.28, 0.40}					

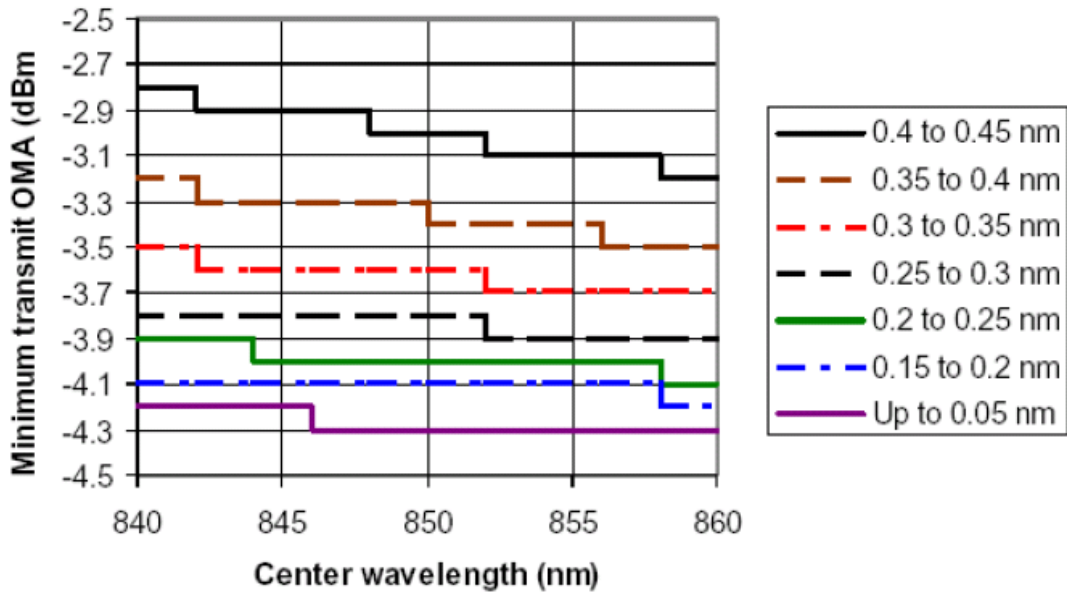
**Transmitter eye mask definition**



**Minimum optical modulation amplitude (dBm) relation table**

Center Wavelength (nm)	RMS Spectral width (nm)									
	Up to 0.05	0.05 to 0.1	0.1 to 0.15	0.15 to 0.2	0.2 to 0.25	0.25 to 0.3	0.3 to 0.35	0.35 to 0.4	0.4 to 0.45	
840 to 842	-4.2	-4.2	-4.1	-4.1	-3.9	-3.8	-3.5	-3.2	-2.8	
842 to 844	-4.2	-4.2	-4.2	-4.1	-3.9	-3.8	-3.6	-3.3	-2.9	
844 to 846	-4.2	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9	
846 to 848	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9	
848 to 850	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-3.0	
850 to 852	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.4	-3.0	
852 to 854	-4.3	-4.2	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1	
854 to 856	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1	
856 to 858	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.5	-3.1	
858 to 860	-4.3	-4.3	-4.2	-4.2	-4.1	-3.9	-3.7	-3.5	-3.2	

Triple tradeoff curve



**Optical Receiver Characteristics ( $T_c = -5^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Signaling speed (nominal)	$T_s$		10.3125		Gb/s	
Signaling speed variation from nominal.				$\pm 100$	ppm	
Center Wavelength	$\lambda$	840		860	nm	
Overload	$P_o$			-1	dBm	
Receiver sensitivity in OMA	RSO			-11.1	dBm	1
LOS De-assert	$LOS_D$			-11	dBm	
LOS Assert	$LOS_A$	-27			dBm	2
LOS Hysteresis	$LOS_D - LOS_A$	0.5			dB	
Receiver Reflectance				-12	dB	3
Differential Output Amplitude		150		850	mV	
Stressed Receive sensitivity OMA				-7.5	dBm	

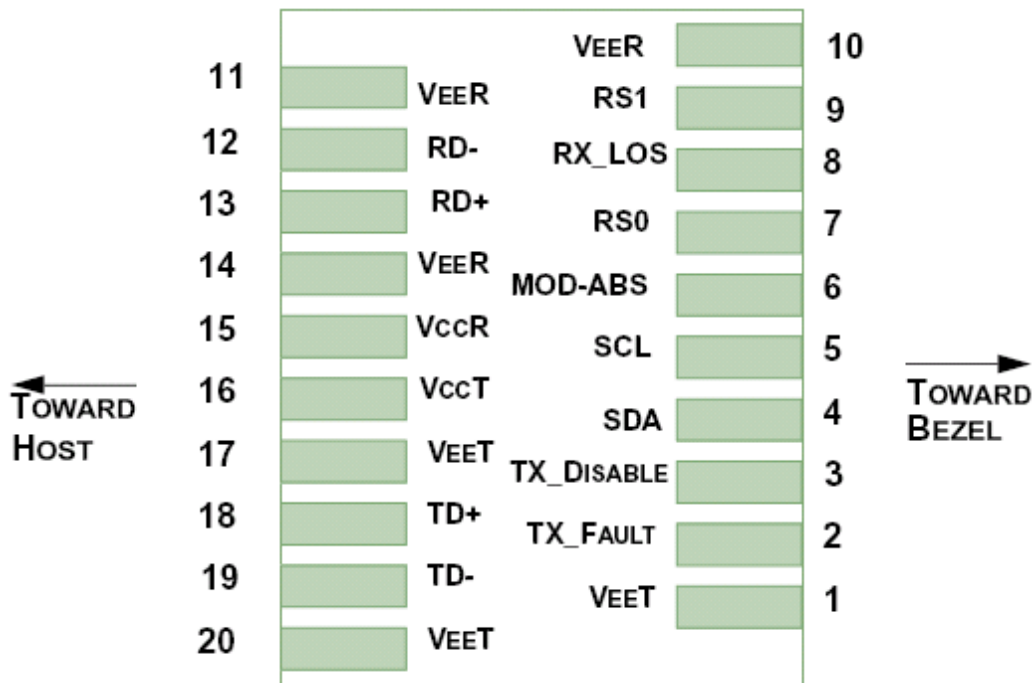
Notes:

1. Measured by reference TX with 4.75dB extinction ratio at  $10^{-12}$  BER
2. When LOS asserted, the data output is Low-Level (fixed)
3. When the terminal is viewed from the optical path, the reflection toward the optical path of the optical signal with a central wavelength of 840nm to 860nm transmitted to terminal.
4. Distance, shown in the "Link Length" table, are calculated for worst case fiber and transceiver characteristics based on the optical and electrical specifications shown in this document using techniques utilized in IEEE 802.3. In the nominal case, longer distance are achievable.

### Link Length

Fiber type	Minimum modal bandwidth @ 850nm (MHz*km)	Operating range (meters)	Note
62.5 um MMF	160	2 to 26	4
	200	2 to 33	4
50 um MMF	400	2 to 66	4
	500	2 to 82	4
	2000	2 to 300	4

### SFP+ Transceiver Electrical Pad Layout



**Module Electrical Pin Definition**

Pin	Logic	Symbol	Name/Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	2
3	LVTTL-I	TX_Disable	Transmitter Disable; Turns off transmitter laser output	3
4	LVTTL-I/O	SDA	2- write Serial Interface Data Line	
5	LVTTL-I/O	SCL	2- write Serial Interface Clock	
6		MOD_ABS	Module Absent, connected to V <sub>ee</sub> T or V <sub>ee</sub> R in the module	4
7	LVTTL-I	RS0	Not Implement	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication	2
9	LVTTL-I	RS1	Not Implement	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Non-Inverter Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3V Supply	
16		VccT	Module Transmitter 3.3V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Griund	1

Note:

1. The module signal ground pins, VeeR and VeeT, shall be isolated from the module case.
2. This pin is an open collector/drain output pin and shall be pulled up with 4.7k-10k ohms to Host\_Vcc on the host board. Pull ups can be connected to multiple power supplies, however the host board design shall ensure that no module pin has voltage exceeding module VccT/R + 0.5V.
3. This pin is an open collector/drain input pin and shall be pulled up with 4.7k-10k ohms to VccT in the Module.
4. This pin shall be pulled up with 4.7k-10k ohms to Host\_Vcc on the host board.

## Low speed electrical control pins and 2-wire interface

In addition to the 2-wire serial interface, the SFP+ module has the following low speed pins for control and status:

- TX\_Fault
- TX\_Disable
- RS0/RS1
- MOD\_ABS
- RX\_LOS

### 1 TX\_Fault

.TX\_Fault is a module output pin that when High, indicates that the module transmitter has detected a fault condition related to laser operation or safety.

The TX\_Fault output pin is an open drain/collector and must be pulled p to the Host\_Vcc with 4.7k-10k ohms on the host board

### 2 TX\_Disable

TX\_Disable is a module input pin. When TX\_Disable is asserted High or Left open, the SFP+ module transmitter output must be turned off. The TX\_DIS pin must be pulled up to VccT in the SFP+ module..

### 3 RS0/RS1

RS0 and RS1 are module input rate select pins and are pulled low to VeeT with a > 30k $\Omega$  resistor in the module. RS0 is an input hardware pin which optionally selects the optical receive data path rate coverage for an SFP+ module. RS1 is an input hardware pin which optionally selects the optical transmit path data rate coverage for an SFP+ module. RS1 is commonly connected to VeeT or VeeR in the legacy SFP modules. The host needs to ensure that it will not be damaged if this pin is connected to VeeT or VeeR in the module.

### 4 MOD\_ABS

Mod\_ABS is pulled up to Host\_Vcc with 4.7k-10k ohms on the host board and connected to VeeT or VeeR in the SFP+ module. MOD\_ABS is then asserted “High” when the SFP+ module is physically absent from a host slot. In the SFP MSA (INF8074i) this pin had the same function but is called MOD\_DEF0.

### 5 SCL/SDA

SCL is the 2-wire interface clock and SDA is the 2-wire interface data line. SCL and SDA are pulled up to a voltage in the range of 3.14V to 3.46V on the host.

### 6 RX\_LOS

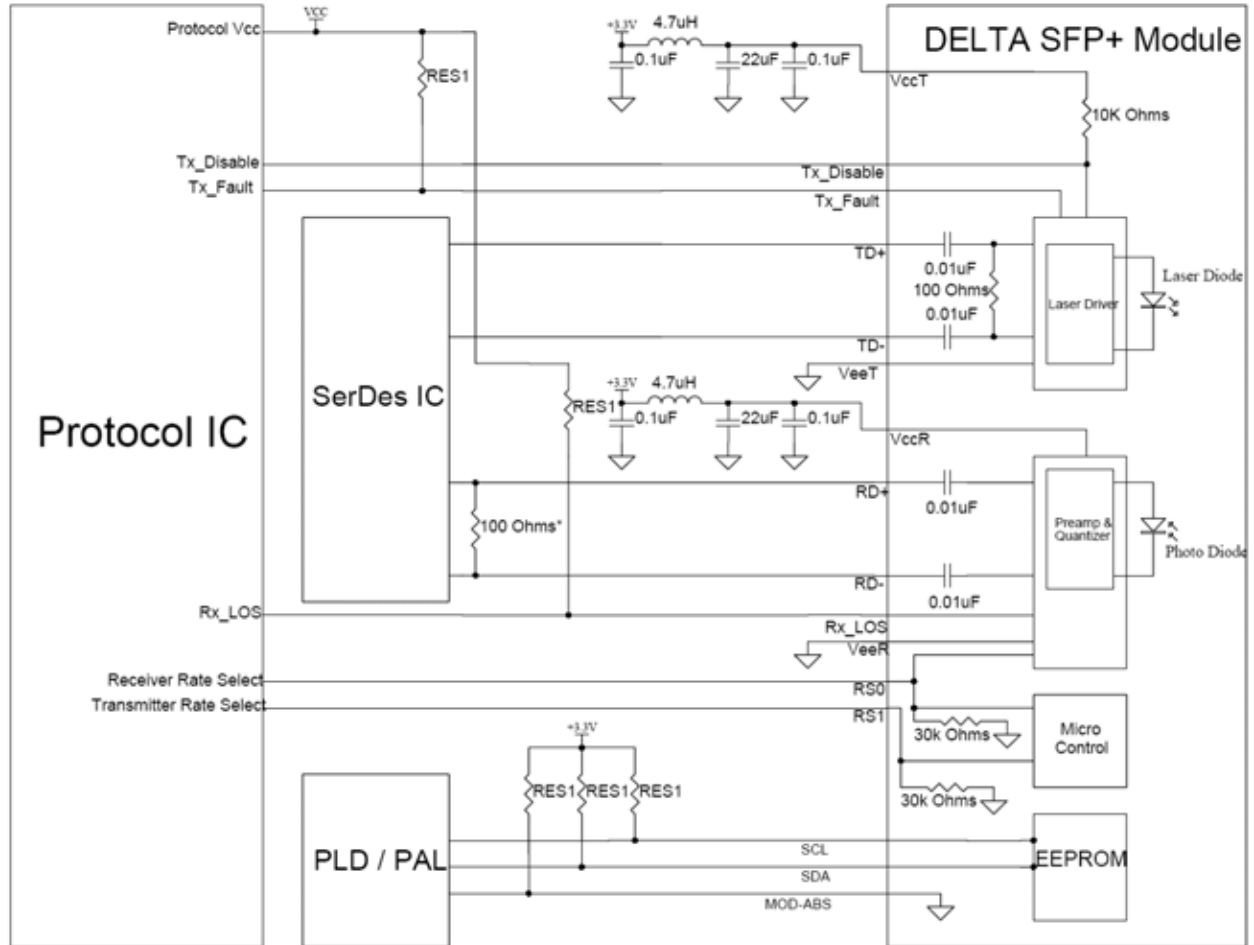
RX\_LOS when High indicated an optical signal level below that specified in the relevant standard. The RX\_LOS pin is an open drain/collector output and must be pulled up to host Vcc with a 4.7k-10k ohms on

the host board.

RX\_LOS assert min and de-assert max are defined in the relevant standard. To avoid spurious transition of RX\_LOS a minimum hysteresis of 0.5 dB is recommended.



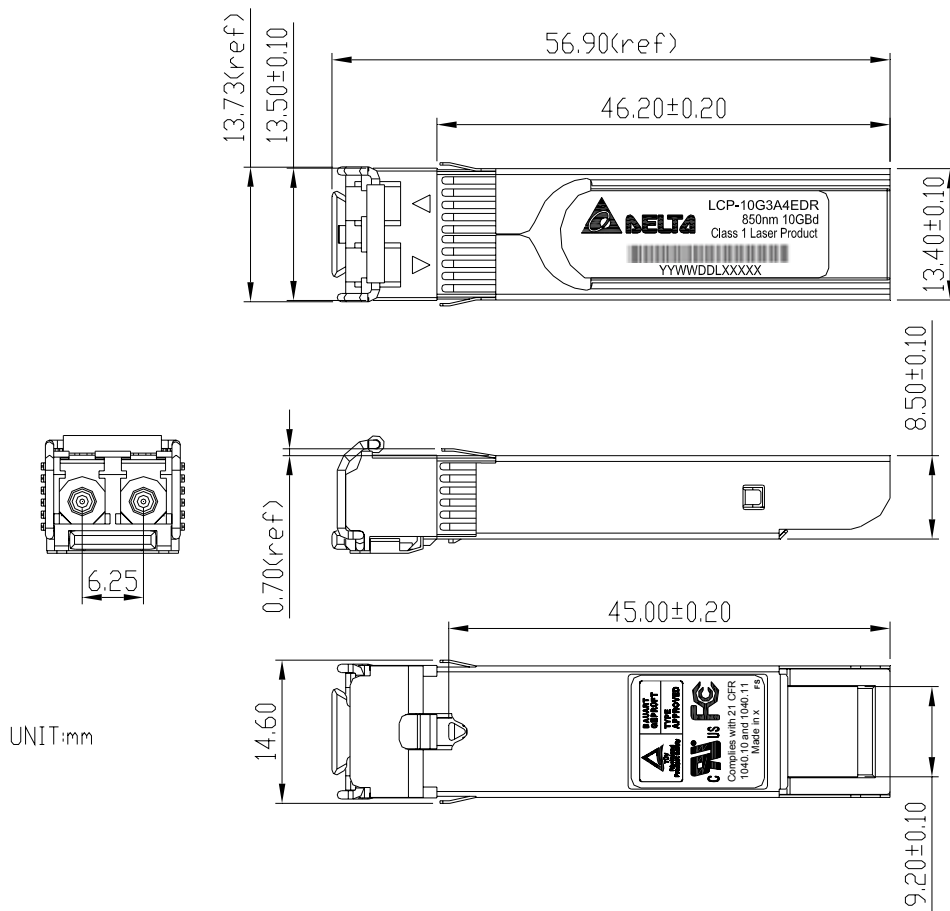
Recommend Circuit Schematic



RES1 = 4.7k TO 10k Ohms  
 \* Depends on SerDes IC used

Package Outline Drawing for Metal Housing with Bail de-latch

<b>Latch Color Identifier</b>
Black



**Timing parameters for SFP+ management**

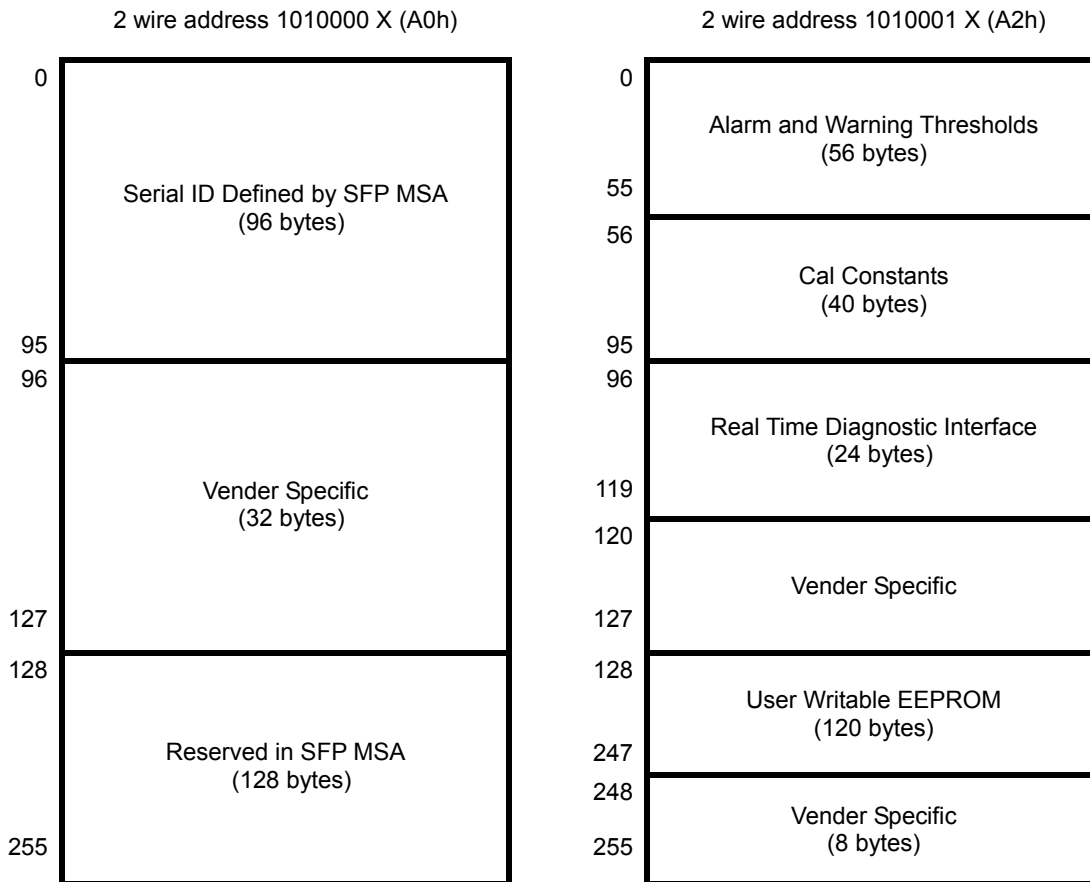
Parameter	Symbol	Min.	Max.	Unit	Note
TX_DISABLE Assert time	t_off		10	μsec	1
TX_DISABLE Negate time	t_on		2	msec	2
Time to initialize 2-wire interphase	t_2w_start_up		300	msec	3
Time to initialize	t_start_up		300	msec	4
Time to initialize cooled module	t_start_up_cooled		90	sec	4
Time to Power Up to Level 2	t_power_level2		300	msec	5
Time to Power Down from Level 2	T_power_down		300	msec	6
TX_Fault assert	TX_Fault_on		1	msec	7
TX_Fault assert for cooled module	TX_Fault_on		50	msec	7
TX_Fault Reset	t_reset	10		μsec	8
Module Reset	t_module_reset		TBD	msec	TBD
RS0, RS1 rate select timing for FC	t_RS0_FC, RS1_FC		500	μsec	9
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		10	msec	9
RX_LOS assert delay	t_los_on		100	μsec	10
RX_LOS negate delay	t_los_off		100	μsec	11

**Notes:**

- 1) Rising edge of TX\_Disable to fall of output signal below 10% of nominal.
- 2) Falling edge of TX\_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
- 3) From power on or negation of TX\_Disable.
- 4) From power on or TX\_Disable negated during power up, or TX\_Fault recovery, until non-cooled power level 1 part (or non-cooled power level 2 part already enabled at power level 2 for TX\_Fault recovery) is fully operational.
- 5) From falling edge of stop bit enabling power level 2 until non-cooled module is fully operational.
- 6) From falling edge of stop bit disabling power level 2 until module is within power level 1 requirements.
- 7) From Occurrence of fault to assertion of TX\_Fault.
- 8) Time TX\_Disable must be held High to reset TX\_Fault.
- 9) From assertion till stable output.
- 10) From Occurrence of loss of signal to assertion of LOS
- 11) From Occurrence of presence of signal to negation of RX\_LOS.

## Enhanced Digital Diagnostic Interface

The memory map in the following describes an extension to the memory map defined in SFP MSA. The enhanced interface uses the two wire serial bus address 1010001X(A2h) to provide diagnostic information about the module's present operating conditions.



Digital Diagnostic Memory Map Specific Data Field Descriptions

**EEPROM Serial ID Memory Contents (2-Wire Address A0h)**

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
00	03		43	2D	-	86	DC	
01	04		44	31	1	87	DC	
02	07		45	30	0	88	DC	
03	10		46	47	G	89	DC	
04	00		47	33	3	90	DC	
05	00		48	41	A	91	DC	
06	00		49	34	4	92	68	
07	00		50	45	E	93	F0	
08	00		51	44	D	94	03	
09	00		52	52	R	95	CS2	Note 4
10	00		53	20		96	00	
11	03		54	20		97	00	
12	67		55	20		98	00	
13	00		56	41		99	00	
14	00		57	20		100	00	
15	00		58	20		101	00	
16	08		59	20		102	00	
17	03		60	03		103	00	
18	00		61	52		104	00	
19	1E		62	00		105	00	
20	44	D	63	CS1	Note 1	106	00	
21	45	E	64	00		107	00	
22	4C	L	65	1A		108	00	
23	54	T	66	00		109	00	
24	41	A	67	00		110	00	
25	20		68	SN	Note 2	111	00	
26	20		69	SN		112	00	
27	20		70	SN		113	00	
28	20		71	SN		114	00	
29	20		72	SN		115	00	
30	20		73	SN		116	00	
31	20		74	SN		117	00	
32	20		75	SN		118	00	
33	20		76	SN		119	00	
34	20		77	SN		120	00	
35	20		78	SN		121	00	
36	00		79	SN		122	00	
37	00		80	SN		123	00	
38	00		81	SN		124	00	
39	00		82	SN		125	00	
40	4C	L	83	SN		126	00	
41	43	C	84	DC	Note 3	127	00	
42	50	P	85	DC		128	00	Note 5

**Notes:**

- 1) Byte 63: Check sum of bytes 0-62.
- 2) Byte 68-83: Serial number.
- 3) Byte 84-91: Date code.
- 4) Byte 95: Check sum of bytes 64-94.
- 5) Byte 128 to 255 had been set hex 00.

**Digital Diagnostic Monitoring Interface**
**Alarm and Warning Thresholds (2-Wire Address A2h)**

Address	# Bytes	Name	Value (Dec.)	Unit	Note
00-01	2	Temp High Alarm	85 degree Celsius	°C	1
02-03	2	Temp Low Alarm	-10 degree Celsius		
04-05	2	Temp High Warning	80 degree Celsius		
06-07	2	Temp Low Warning	-5 degree Celsius		
08-09	2	Voltage High Alarm	3.6V	Volt	
10-11	2	Voltage Low Alarm	3.0V		
12-13	2	Voltage High Warning	3.5V		
14-15	2	Voltage Low Warning	3.1V		
16-17	2	Bias High Alarm	I <sub>OP</sub> +10 mA	mA	2
18-19	2	Bias Low Alarm	I <sub>OP</sub> -5 mA		
20-21	2	Bias High Warning	I <sub>OP</sub> +7 mA		
22-23	2	Bias Low Warning	I <sub>OP</sub> -3 mA		
24-25	2	TX Power High Alarm	P +3dB	dBm	3
26-27	2	TX Power Low Alarm	P -3dB		
28-29	2	TX Power High Warning	P +2dB		
30-31	2	TX Power Low Warning	P -2dB		
32-33	2	RX Power High Alarm	0dBm	dBm	4
34-35	2	RX Power Low Alarm	-13.1dBm		
36-37	2	RX Power High Warning	-1dBm		
38-39	2	RX Power Low Warning	-11.1dBm		
40-45	16	Reversed			
56-91	36	External Calibration Constants			
92-94	3	Reversed			
95	1	Checksum			5
96-97	2	Real Time Temperature			
98-99	2	Real Time Supply Voltage			
100-101	2	Real Time Tx Bias Current			
102-103	2	Real Time Tx Optical Power			
104-105	2	Real Time Rx Received Power			
106-109	4	Reserved			
110	1	Optional Status/ Control Bits			
111	1	Reserved			
112-119	8	Optional Set of Alarm and Warning			

**Notes:**

- 1) T<sub>C</sub>: Case Operating temperature
- 2) I<sub>OP</sub>: Operating current at room temperature. The min. setting current is 0 mA.
- 3) P: Operating optical power of transmitter at room temperature.
- 4) P<sub>0</sub>: Overload optical power of receiver  
P<sub>S</sub>: Sensitivity optical power of receiver
- 5) Byte 95 contains the low order 8bits of sum of bytes 0-94

6)

**State/ Control Bits**

Byte	Bit	Name	Description
110	7	Tx Disable State	Digital state of the Tx disable input pin
110	6	Soft Tx Disable	Read/ Write bit that allow software disable of laser
110	5	Reserved	
110	4	Rate Select State	Rate Select State
110	3	Soft Rate Select	Software Rate Select State
110	2	Tx Fault	Digital state of the Tx fault output pin
110	1	LOS	Digital state of the LOS output pin.
110	0	Data_Ready_Bar	NA

7)

**Optional Set of Alarm and Warning**

Byte	Bit	Name	Description
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level
112	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level
112	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level
112	3	Tx Bias High Alarm	Set when Tx Bias current exceeds high alarm level
112	2	Tx Bias Low Alarm	Set when Tx Bias current is below low alarm level
112	1	Tx Power High Alarm	Set when Tx output power exceeds high alarm level
112	0	Tx Power Low Alarm	Set when Tx output power is below low alarm level
113	7	Rx Power High Alarm	Set when received power exceeds high alarm level
113	6	Rx Power Low Alarm	Set when received power is below low alarm level
113	5-0	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level
116	6	Temp Low Warning	Set when internal temperature is below low warning level
116	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level
116	4	Vcc Low Warning	Set when internal supply voltage is below low warning level
116	3	Tx Bias High Warning	Set when Tx Bias current exceeds high warning level
116	2	Tx Bias Low Warning	Set when Tx Bias current is below low warning level
116	1	Tx Power High Warning	Set when Tx output power exceeds high warning level
116	0	Tx Power Low Warning	Set when Tx output power is below low warning level
117	7	Rx Power High Warning	Set when received power exceeds high warning level
117	6	Rx Power Low Warning	Set when received power is below low warning level
117	5-0	Reserved	

**Digital Diagnostic Monitor Accuracy**

Parameter	Typical Value	Note
Transceiver Temperature	$\pm 3^{\circ}\text{C}$	1
Power Supply Voltage	$\pm 3\%$	2
TX Bias Current	$\pm 10\%$	
TX Optical Power	$\pm 1.5\text{dB}$	
RX Optical Power	$\pm 3\text{dB}$	

**Notes:**

- 1) Temperature is measured internal to the transceiver
- 2) Voltage is measured internal to the transceiver

**Regulatory Compliance**

Feature	Test Method	Reference	Performance
Electromagnetic Interference (EMI)		FCC Part15 Class B EN 55022 Class B (CISPR 22A)	(1) Satisfied with electrical characteristics of product spec.  (2) No physical damage
Radio Frequency Electromagnetic Field Immunity		IEC/EN 61000-4-3	
Electrostatic Discharge (ESD) to the Duplex LC Receptacle	Contact Discharge	IEC/EN 61000-4-2	
	Air Discharge	IEC/EN 61000-4-2	
Electrostatic Discharge (ESD) to the Electrical Pins	Human Body Model (HBM)	MIL-STD-883E Method 3015.7 EIA-JESD22-A114	
	Machine Model (MM)	EIA-JESD22-A115	
Laser Eye Safety	FDA/CDRH	US FDA CDRH AEL Class 1	
	TUV	IEC/EN 60825-1 IEC/EN 60825-2	
Component Recognition	TUV	IEC/EN 60950-1	
	UL/CSA	UL60950	