



**Connect Tech Inc.**  
*Industrial Strength Communications*

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# FreeForm/PCI-104

## User Manual



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### Email/Internet

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## Introduction

Connect Tech's FreeForm/PCI-104 features Xilinx's Virtex-5 multi-platform FPGA offering users a flexible, reconfigurable computing platform that also takes advantage of the high bandwidth capabilities of the PCI bus while communicating with various I/O interfaces.

## Product Features

- PCI-104 form factor – 32-Bit/33MHz
- Xilinx multi-platform Virtex-5 FPGA with 3 million logic gates
- 2MB Flash for FPGA configuration storage
- 8MB Flash for embedded code storage
- Designed for embedded processing using MicroBlaze™
- 100MHz input clock
- 128MB DDR2-400 memory
- 2 x 10/100 Ethernet with modular jacks
- 2 x RS-485 serial interface
- High-speed serial connector 4 x Rocket I/O (GTP) channels
- 64 single ended or 32 LVDS general purpose I/O
- External 5V power connection for programming and development
- JTAG test and programming chain
- Industrial temperature range of -40°C to 85°C
- Ships preconfigured with a reference design

## About this manual

This manual will provide the user with the following information:

- System overview
- Introduction to the reference design
- Description of jumpers, switches, and connector pinouts
- Hardware installation instructions
- Software installation instructions
- FPGA configuration details
- Specifications

## System Overview

The following conceptual block diagram provides a high level overview of the FreeForm/PCI-104 and illustrates the general interconnection between components and connectors.

For the actual orientation and description of components refer to Figure 2 and Table 1 respectively.

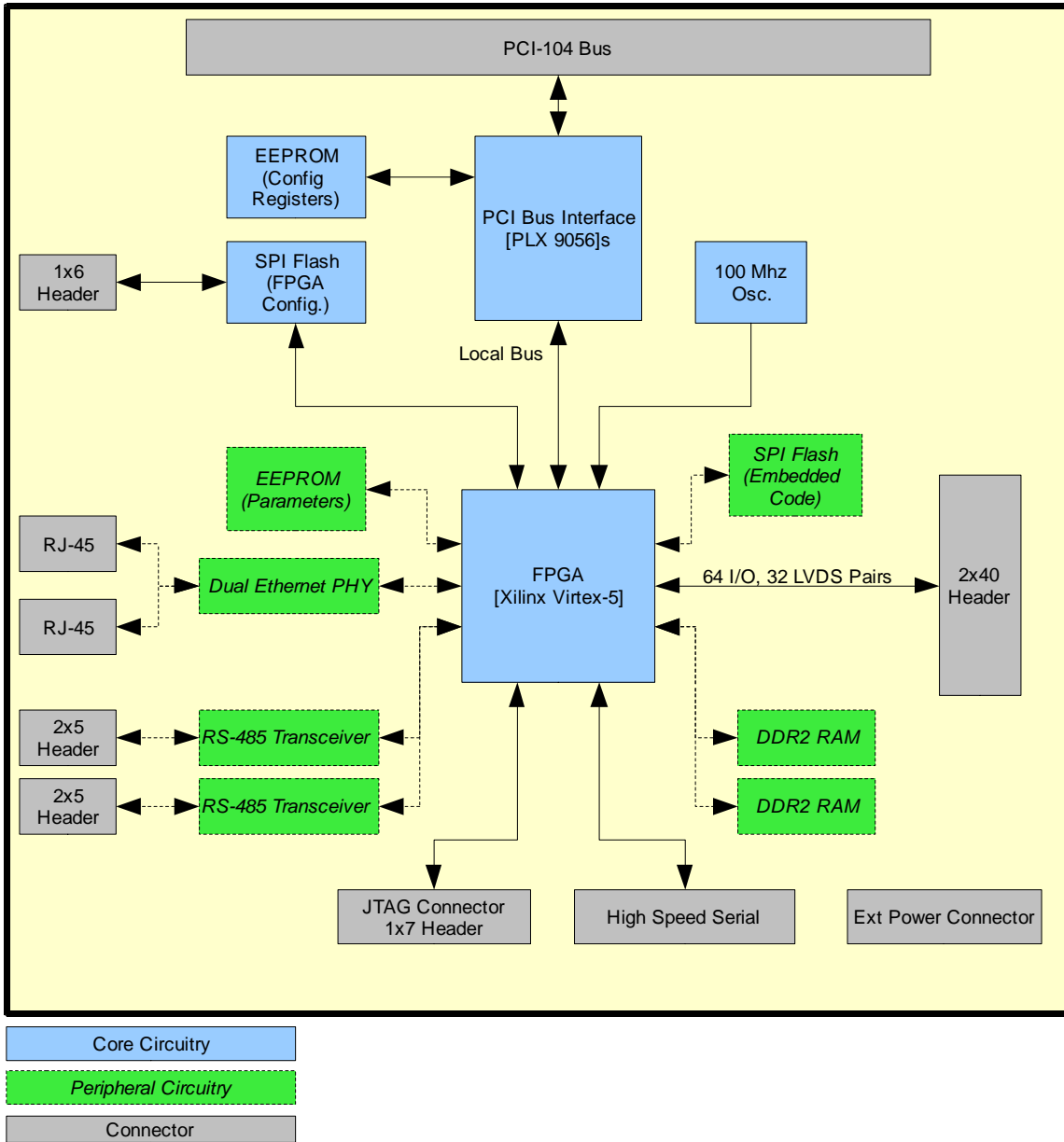


Figure 1: FreeForm/PCI-104 Block Diagram

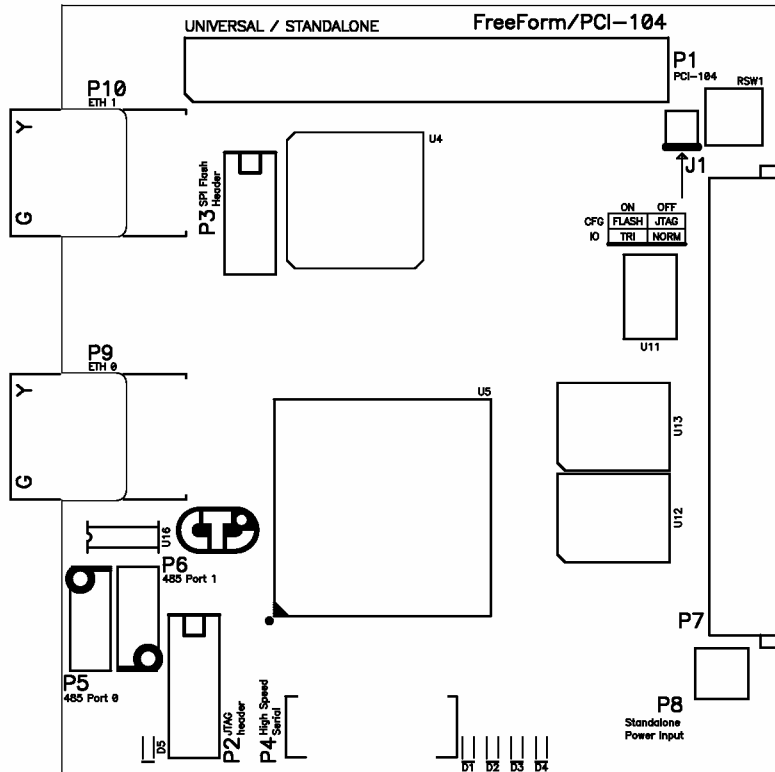


Figure 2: FreeForm/PCI-104 Layout

Table 1: FreeForm/PCI-104 Components

Connectors	Description
P1	PCI-104 connector
P2	JTAG programming header
P3	SPI flash programming header
P4	High-speed serial connector
P5, P6	RS-485 header
P7	GPIO header
P8	External power header
P9	RJ-45 A
P10	RJ-45 B
Jumpers /Switches	Description
RSW1	Slot selection
J1	FPGA configuration settings
Components	Description <i>(not all on top side)</i>
D1-D4	User LEDs
D5	FPGA load complete LED
U4	PLX PCI-local bus bridge
U5	Virtex-5 FPGA
U10	FPGA configuration flash
U11	Embedded code flash
U12, U13	DDR2 memory
U14	Parameter EEPROM
U15, U16	RS-485 transceiver
U17	Dual 10/100 PHY
O1,O2, O3	Oscillators



## Reference Design

The FreeForm/PCI-104 ships with a pre-installed reference design that is loaded into the FPGA's configuration flash. This reference design demonstrates how to interface the FreeForm/PCI-104 (Virtex-5 FPGA) with the PLX PCI 9056 PCI to Local Bus Bridge, as well as the various peripherals.

The PLX 9056 provides a generic local bus that is capable of operating at up to 66MHz (this design forwards a 50MHz clock to the PLX). The PLX bridge has been set in the C-Mode of operation. The reference logic operates as a local bus slave, as well as a local bus master.

The reference design contains examples demonstrating:

- Loading of PLX 9056's registers via the local bus
- Local bus slave transfers
- Local bus master transfers
- GPIO control
- Programming the SPI Flash
- Interfacing to the built-in Virtex-5 TEMACs
- RS-485 serial data transfers
- Reading/writing to the serial EEPROM
- Reading/writing to DDR2 memory
- Interfacing to the Virtex-5 Rocket I/O transceivers

Most of the example VHDL modules demonstrate how to interface with the various peripherals through a register set, which is accessible by the host system over the PCI bus. A set of software applications has been created to show how the host system can communicate with each FPGA sub-module. In most applications, the host system will not directly control these peripherals. In a custom application, these modules can be easily modified to interconnect with each other through the FPGA fabric.

To obtain the source code, refer to [Software Installation](#). For further details on the reference design, refer to *FreeForm/PCI-104 Reference Design Guide (CTIM-00042)*

## Hardware Description

The following sections describe the function of all switches/jumpers and provide details on connector pinouts.

### *Jumpers and Switches*

#### Slot Selection (RSW1)

This rotary switch selects a slot position in the PCI-104 stack. When mounting on a PCI adapter card, ensure slot one is selected.




**Table 2: Slot Selection (RSW1)**

Position	Slot
0,4	0
1,5	1
2,6	2
3,7	3

#### FPGA Configuration Settings (J1)

Jumper J1 is used to control FPGA configuration.

**Table 3: FPGA Configuration Settings (J1)**

Location	Function
	FPGA waits for configuration over JTAG (using P2)
	FPGA reads configuration from SPI flash
	FPGA is tri-stated, flash is isolated from FPGA and can be programmed directly

## Connector Pinouts

### PCI-104 Header (P1)

Refer to [PCI-104 specifications](#).

Note: P1 must be connected to a PCI-104 stack supplying both 3.3V and 5V.

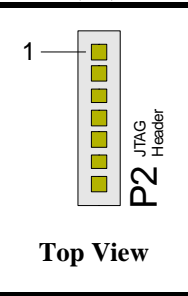
### JTAG Programming Header (P2)

Use P2 to configure the FPGA via JTAG. Refer to [FPGA Configuration](#) for more information. Power pins are for voltage reference only; they do not provide power to the configuration circuitry.

Note that the FPGA can always be programmed via JTAG, regardless of the [J1](#) configuration setting.

**Table 4: JTAG Programming Header Pinout (P2)**

Pin	Signal	Direction
1	TRST	Input
2	TMS	Input
3	TDI	Input
4	TDO	Output
5	TCK	Input
6	GND	Reference
7	3.3V	Reference



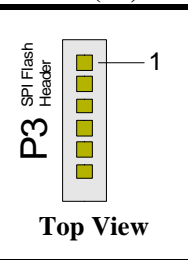
**Top View**

### SPI Flash Programming Header (P3)

P3 may be used to directly program the SPI flash, providing that [J1](#) is set correctly to the tri-state FPGA position. The power pins are for voltage reference only. They do not provide power to the configuration circuitry.

**Table 5: SPI Flash Programming Header Pinout (P3)**

Pin	Signal	Direction
1	SPI_CSN	Input
2	SPI_MOSI	Input
3	SPI_MISO	Output
4	SPI_CLK	Input
5	GND	Reference
6	3.3V	Reference



**Top View**

### High-speed Serial (P4)

The high-speed serial connector carries four Rocket (GTP) I/O channels, each with a dedicated transmit and receive differential pair. These channels are capable of operating up to 3.125 Gbps, depending on configuration. For more information on Rocket I/O capabilities, visit the Xilinx website: [http://www.xilinx.com/products/silicon\\_solutions/fpgas/virtex/virtex5/](http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/)

**Table 6: High-Speed serial Connector Pinout (P4)**

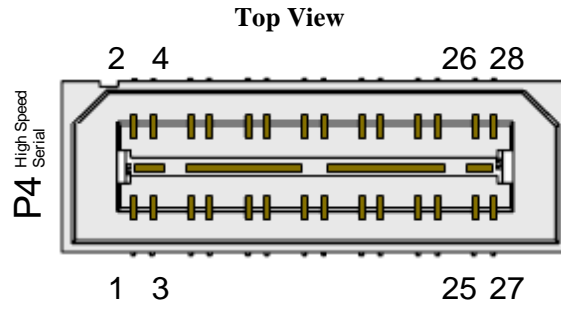
Pin	Signal	Direction	Notes
1	MTGRXN0_112	Input	(b)
3	MTGRXP0_112	Input	(b)
2	MTGTYN0_112	Output	(b)
4	MTGTXP0_112	Output	(b)
5	HSS_USER_IO(0)	Input/Output	(a), (d)
7	HSS_USER_IO(1)	Input/Output	(a), (d)
6	HSS_USER_IO(2)	Input/Output	(a), (d)
8	HSS_USER_IO(3)	Input/Output	(a), (d)
9	MTGRXN1_112	Input	(b)
11	MTGRXP1_112	Input	(b)
10	MTGTYN1_112	Output	(b)
12	MTGTXP1_112	Output	(b)
13	3.3V	Power	(a)
15	3.3V	Power	(a)
14	3.3V	Power	(a)
16	3.3V	Power	(a)
17	MTGRXN0_114	Input	(c)
19	MTGRXP0_114	Input	(c)
18	MTGTYN0_114	Output	(c)
20	MTGTXP0_114	Output	(c)
21	3.3V	Power	(a)
23	3.3V	Power	(a)
22	3.3V	Power	(a)
24	3.3V	Power	(a)
25	MTGRXN1_114	Input	(c)
27	MTGRXP1_114	Input	(c)
26	MTGTYN1_114	Output	(c)
28	MTGTXP1_114	Output	(c)

Notes:

- a) Pins have a different function from Revision B.
- b) The Rocket I/O (GTP) are organized into tiles, where each tile has two transceivers and shares a common PLL. In this design, tiles 112 and 114 are used.
- c) Tile 112 has AC coupling capacitors on the TX pairs, validated at PCI Express data rates (2.5 Gbps).
- d) Tile 114 has AC coupling capacitors on both the RX and TX pairs, validated at SATA data rates (1.5 Gbps).
- e) HSS\_USER\_IO are flexible LVCMOS side-band signals.

**WARNING**

If connecting two FreeForm/PCI-104's together using the Rocket I/O interface in a cross-over fashion; care must be taken. Ensure that only cables provided by Connect Tech are used. Cables ordered directly from Samtec or a third party could result in damage to the cable and/or the FreeForm/PCI-104 board itself.



**RS-485 Headers (P5, P6)**

**Table 7: RS-485 Port 1 Pinout (P5)**

Pin	Signal	Direction
1	RXD+1	Input
2		
3	RXD-1	Input
4		
5	TXD+1	Output
6		
7	TXD-1	Output
8		
9	GND	Power
10		

**Top View**

**Table 8: RS-485 Port 2 Pinout (P6)**

Pin	Signal	Direction
1	RXD+2	Input
2		
3	RXD-2	Input
4		
5	TXD+2	Output
6		
7	TXD-2	Output
8		
9	GND	Power
10		

**Top View**

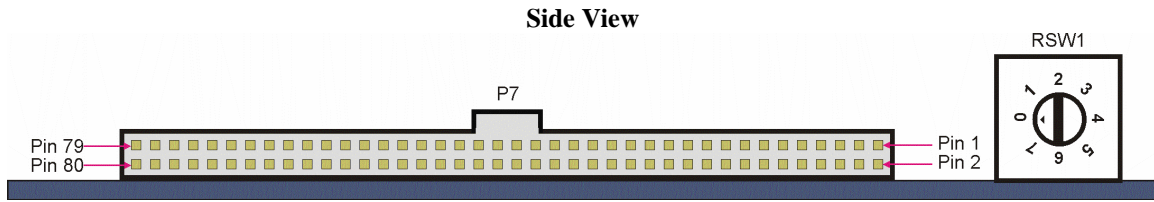
**GPIO Header (P7)**

When in differential mode, the GPIO header positive (P) and negative (N) signals are adjacent on a standard ribbon cable. Note that the GPIO voltage level is set via hardware.

- FCG001: L12 populated, enabling 2.5V I/O, including LVDS
- FCG002: L13 populated, enabling 3.3V I/O

**Table 9: GPIO Header Pinout**

Pin	Signal	Direction	Pin	Signal	Direction
1	GPION(0)	Input/Output	41	GPION(16)	Input/Output
2	GPIOP(0)	Input/Output	42	GPIOP(16)	Input/Output
3	GPION(1)	Input/Output	43	GPION(17)	Input/Output
4	GPIOP(1)	Input/Output	44	GPIOP(17)	Input/Output
5	GPION(2)	Input/Output	45	GPION(18)	Input/Output
6	GPIOP(2)	Input/Output	46	GPIOP(18)	Input/Output
7	GPION(3)	Input/Output	47	GPION(19)	Input/Output
8	GPIOP(3)	Input/Output	48	GPIOP(19)	Input/Output
9	GND	Power	49	GND	Power
10	GND	Power	50	GND	Power
11	GPION(4)	Input/Output	51	GPION(20)	Input/Output
12	GPIOP(4)	Input/Output	52	GPIOP(20)	Input/Output
13	GPION(5)	Input/Output	53	GPION(21)	Input/Output
14	GPIOP(5)	Input/Output	54	GPIOP(21)	Input/Output
15	GPION(6)	Input/Output	55	GPION(22)	Input/Output
16	GPIOP(6)	Input/Output	56	GPIOP(22)	Input/Output
17	GPION(7)	Input/Output	57	GPION(23)	Input/Output
18	GPIOP(7)	Input/Output	58	GPIOP(23)	Input/Output
19	GND	Power	59	GND	Power
20	GND	Power	60	GND	Power
21	GPION(8)	Input/Output	61	GPION(24)	Input/Output
22	GPIOP(8)	Input/Output	62	GPIOP(24)	Input/Output
23	GPION(9)	Input/Output	63	GPION(25)	Input/Output
24	GPIOP(9)	Input/Output	64	GPIOP(25)	Input/Output
25	GPION(10)	Input/Output	65	GPION(26)	Input/Output
26	GPIOP(10)	Input/Output	66	GPIOP(26)	Input/Output
27	GPION(11)	Input/Output	67	GPION(27)	Input/Output
28	GPIOP(11)	Input/Output	68	GPIOP(27)	Input/Output
29	GND	Power	69	GND	Power
30	GND	Power	70	GND	Power
31	GPION(12)	Input/Output	71	GPION(28)	Input/Output
32	GPIOP(12)	Input/Output	72	GPIOP(28)	Input/Output
33	GPION(13)	Input/Output	73	GPION(29)	Input/Output
34	GPIOP(13)	Input/Output	74	GPIOP(29)	Input/Output
35	GPION(14)	Input/Output	75	GPION(30)	Input/Output
36	GPIOP(14)	Input/Output	76	GPIOP(30)	Input/Output
37	GPION(15)	Input/Output	77	GPION(31)	Input/Output
38	GPIOP(15)	Input/Output	78	GPIOP(31)	Input/Output
39	GND	Power	79	GND	Power
40	GND	Power	80	GND	Power



**External Power Connector (P8)**

The external connector provides 5V to the power regulation circuitry.

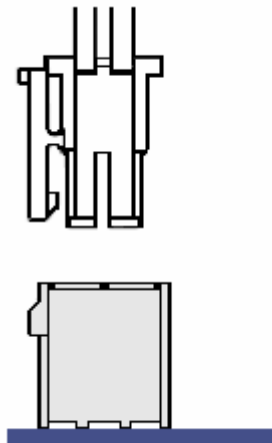
The external power connector should only be used when the FreeForm/PCI-104 is being programmed outside of a PCI/PCI-104 system.

**Table 10: External Power Connector Pinout (P8)**

Pin	Signal	Direction
1	5V	Power
2		
3	GND	Power
4	VIO (connect to 5V)	Power

The diagram shows a 4-pin connector labeled P8 Standalone Power Input. The pins are numbered 1, 2, 3, and 4. Pin 1 is at the top left, pin 2 at the top right, pin 3 at the bottom left, and pin 4 at the bottom right.

It is recommended that a Connect Tech Inc. FreeForm/PCI-104 power supply is used for providing external power. Orientation of the power supply connector is important. Ensure that the clip on the cable aligns with the catch on P8, as shown below.



**Figure 3: External Power Connection**

## Connector's Mating Components and Cables

The following table lists the manufacturer and part number for connectors on the FreeForm/PCI-104, as well as potential mating components.

**Table 11: Connector Mate Listing**

Connector	Component on FreeForm/PCI-104	Mating components	Mating cable assembly
P2	Samtec TSW-107-07-L-S (0.100" pitch, 1x7)	Samtec SSW-107-xx-G-S (Socket, other options available)	Connect Tech Inc. CBG027 (JTAG programming cable)
P3	Samtec TSW-106-07-L-S (0.100" pitch, 1x6)	Samtec SSW-106-xx-G-S (Socket, other options available)	Connect Tech Inc. CBG027 (JTAG programming cable)
P4	Samtec QSE-014-01-L-D-DP-A (0.8mm pitch, 2x14, arranged as 14 differentials pairs)	Samtec QTE-014-01-L-D-DP-A (5mm mated height, other heights available)	Connect Tech. Please contact sales for more information.
P5/P6	Samtec TSW-105-07-L-D (0.100" pitch, 2x5)	Samtec SSW-105-xx-G-D (Socket, other options available)	Connect Tech Inc. CAG104 (Header to DB9)
P7	Tyco 5-104069-3 (0.050"x0.100" pitch, 2x40)	Tyco 3-111196-3 (ribbon cable mate)  <i>or</i>  Tyco 8-487937-0 (discrete wire housing) Tyco 1-487547-1 (crimps for housing)	-
P8	Samtec IPL1-102-01-S-D (0.100" pitch, 2x2)	Samtec IPD1-02-D (discrete wire housing) Samtec CC79L-2024-01-S (crimps for housing)  <i>or</i>  Samtec MMSD-02-22-S-03-25-S (pre-assembled housing and wiring)	Connect Tech Inc. MSG037 (5V power supply, for development purposes)

Note: CBG027 and MSG037 are available as part of development kit DEV002

For more details on mating components, visit:

- Samtec (<http://www.samtec.com/>)
- Tyco Electronics (<http://www.tycoelectronics.com/>)



## Hardware Installation

Before installing the FreeForm/PCI-104 into a PCI-104 stack, ensure the following:

- Slot selection is properly set using the rotary switch [RSW1](#).
- FPGA configuration jumper [J1](#) is set to read from flash.

Once installed in the system and power is applied, the LED D1 will illuminate to indicate that FreeForm/PCI-104 is functioning.

## Heat Sink Installation

Each FreeForm/PCI-104 ships with a FPGA heat sink (27 mm x 27 mm); to be installed by the user. Simply peel of the sticker backing and press firmly onto the FPGA, using proper ESD precautions.

If the heat sink size is not suitable for your application, please contact Connect Tech Inc.

<p><b>WARNING</b> In many applications, including high speed memory operations, the FPGA dissipates a significant amount of power. Failure to use any heat sinking will result in the product warranty being voided.</p>
--

## Stand-alone Operation

Operating the FreeForm/PCI-104 outside of a PCI-104 stack or a PCI system for extended periods of time is not recommended. The PCI to local bus bridge (PCI PLX 9056) requires the pull-up/pull-down resistors provided on a system's main board.

Configuring or programming the FreeForm/PCI-104 in stand-alone mode is acceptable, providing that it is not left powered on in stand-alone state for an extended period of time.

<p><b>WARNING</b> The power supply MSG037 included with the development kit DEV002 is intended for desktop programming only. It is not intended or warranted to be used in any other situation.</p>
---

## Software Installation

### ***FPGA Development Environment***

FreeForm/PCI-104 has been developed with Xilinx WebPACK 9.2, available free of charge at:

[http://www.xilinx.com/ise/logic\\_design\\_prod/webpack.htm](http://www.xilinx.com/ise/logic_design_prod/webpack.htm)

### ***PLX Software Development Kit (SDK)***

PLX provides a software development kit (SDK) to aid in the creation of applications using the PLX 9056 bridge. The SDK provides a generic driver for Windows 2000/XP and Linux. A common API is also included; which encapsulates functions like:

- Configuration register read / write
- Block read / block write to local address space (i.e. memory / registers in the FPGA)
- Physical memory allocation, for bus mastering or DMA purposes
- Interrupt handling
- EEPROM read/write by address

The SDK is available for download from:

<http://www.plxtech.com/products/sdk/>

In order to download the SDK, you will need to register with PLX.

### ***Reference Design & Application Examples***

The FreeForm/PCI-104 ships with a CD containing:

- Documentation and manuals
- FPGA VHDL reference design
- Software program examples

The reference design and example programs help users quickly develop custom hardware and software applications. Refer to the CD for installation instructions.

The latest reference design is always available from:

<http://devel.connecttech.com/>

If a username and password have not already been provided, please contact Connect Tech Support via email [support@connecttech.com](mailto:support@connecttech.com).

## FPGA Configuration

The Virtex-5 FPGA can be configured via two methods:

- JTAG programming chain, using [P2](#)
- SPI Flash, read on, power-up by FPGA

The configuration flash can be programmed (loaded) through three methods:

- JTAG programming chain (through FPGA), using [P2](#)
- Direct with cable, using [P3](#)
- Indirect programming through FPGA, only possible after configuration is complete (refer to reference design for more details)

To configure the FPGA via the JTAG / boundary scan programming chain, three items are required:

- FPGA bitstream (\*.bit), generated at end FPGA implementation using ISE
- PLX 9056 boundary scan definition file (\*.bdsl)
- Ethernet PHY boundary scan definition file

To program the SPI flash, a hex file must be generated (\*.mcs) then written to the flash. To generate the hex file, the following is required:

- FPGA Bitstream
- Setting PROM file format to MCS (important since bits are swapped)
- Setting SPI PROM density to 16M
- Setting SPI Flash type to M25P16

For a complete procedure, refer to [Appendix A](#).

## Power and Thermal Considerations

The FreeForm/PCI-104's Virtex-5 FPGA is a versatile, flexible device, with many built-in features like termination, PLLs, and high speed gigabit transceivers. The drawback of these on-chip features is that they consume a lot of power and hence dissipate a lot of heat.

As a result Connect Tech, is recommending the installation of a heatsink, included with the product (see section [Heat Sink Installation](#)). As well, the FPGA designer *must* perform power analysis on their design to determine that they are not stressing the Virtex-5 component (i.e. exceeding the junction temperature).

Power analysis can be performed using the Xpower Analyzer (part of the ISE design suite) and the XPE spreadsheets (Xilinx Power Estimator Spreadsheets).

[http://www.xilinx.com/products/design\\_resources/power\\_central/](http://www.xilinx.com/products/design_resources/power_central/)

### Reference Design FPGA power analysis

Power analysis was performed on the FCG001 when configured with the reference design. The Virtex-5 XPE spreadsheet was used to determine an effective junction to ambient thermal resistance ( $\theta_{JA\_effective}$ ). The following parameters are entered into the spreadsheet to determine  $\theta_{JA\_effective}$ .

Device	
Part	XC5VLX30T
Package	FF665
Grade	Industrial
Process	Typical
Speed Grade	-1
Stepping	Stepping - 1
Thermal Information	
Ambient Temp (°C)	50
Airflow (LFM)	250
Heat Sink	Custom
Custom $\Theta_{SA}$ (°C/W)	8 (*)
Board Selection	Small (4"x4")
# of Board Layers	12 to 15

( $\theta_{SA}$  is the surface to ambient temperature for a heatsink with dimensions 27 mm x 27 mm x 6.4 mm and 250 LFM airflow. The  $\theta_{SA}$  improves (decreases) with a taller heatsink.)

Three scenarios were developed and the XPE parameters Airflow and Custom  $\Theta_{SA}$  were varied. The  $\theta_{JA\_effective}$  was entered into the Xpower Analyzer yielding a Junction Temperature @ 50 °C and a maximum ambient temperature. The following table summarizes the scenarios and the results. For complete details of the scenarios, see Appendix B.

Scenario	$\theta_{JA\_effective}$ (°C/W)	$T_{ambient\_max}$	$T_{junction}$ at 50 °C
Heatsink attached, 250 LFM	4.9	82.7	67.3
No Heatsink, 250 LFM	6.4	72.7	72.7
No heatsink, 0 LFM	9.7	65.1	84.9

Calculation details:

$$T_{junction} = T_{ambient} + (P_{FPGA} * \theta_{JA\_effective}) = 50^{\circ}C + (3.53W * 4.9^{\circ}C/W) = 67.297^{\circ}C$$

$$T_{ambient\_max} = T_{junction\_max} - (P_{FPGA} * \theta_{JA\_effective}) = 100^{\circ}C - (3.53W * 4.9^{\circ}C/W) = 82.7^{\circ}C$$

Note  $T_{junction\_absolute\_max} = 125^{\circ}C$  is not used, since this is the absolute point of failure.

## Specifications

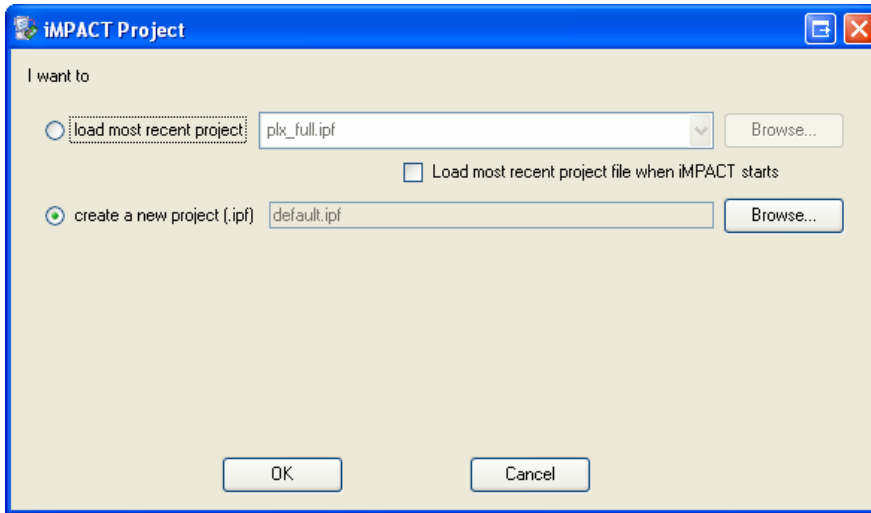
<b>Programmable FPGA</b>	Virtex-5 FPGA LX30T
<b>Input Clock</b>	100MHz
<b>Memory / Flash</b>	128MB DDR2-400 2MB Flash – FPGA configuration 8MB Flash – Embedded code 4K serial EEPROM – parameter storage
<b>General Purpose User I/O</b>	64 single ended I/O 32 LVDS I/O
<b>Serial</b>	2 x RS-485
<b>Ethernet</b>	2 x 10Base-T, 100Base-TX
<b>High-speed serial</b>	4 x Rocket I/O transceivers (GTP)
<b>Operating Environment</b>	Storage Temperature: -65°C to 150°C  Operating Temperature: 0°C to 70°C (commercial) -40°C to 85°C (industrial)
<b>Power Requirements</b>	+5V DC, in PCI-104 stack +5V DC standalone  Current requirements are configuration dependant
<b>Dimensions</b>	PC/104-Plus 2.2 compliant PCI-104 1.0 compliant
<b>Connectors</b>	Two RJ-45 modular jacks (Ethernet) Two 2x5 0.100" headers (serial) One 2x40 0.050 x 0.100" header (general I/O) One 1x6 0.100" header (flash programming) One 2x14 0.8 mm differential pair terminal (high speed serial)

## Appendix A: iMPACT Instructions for FPGA Configuration

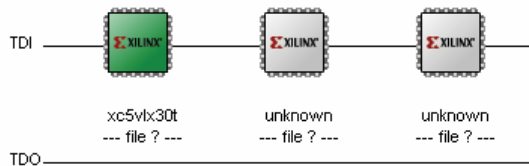
To configure the FPGA via JTAG, connect the JTAG programming cable to [P2](#) ensuring that all JTAG signals align correctly. It is important to note that [P2](#) also has the TRST signal on pin 1, which is not part of Xilinx's Parallel or USB programming cables.

### Launch Impact

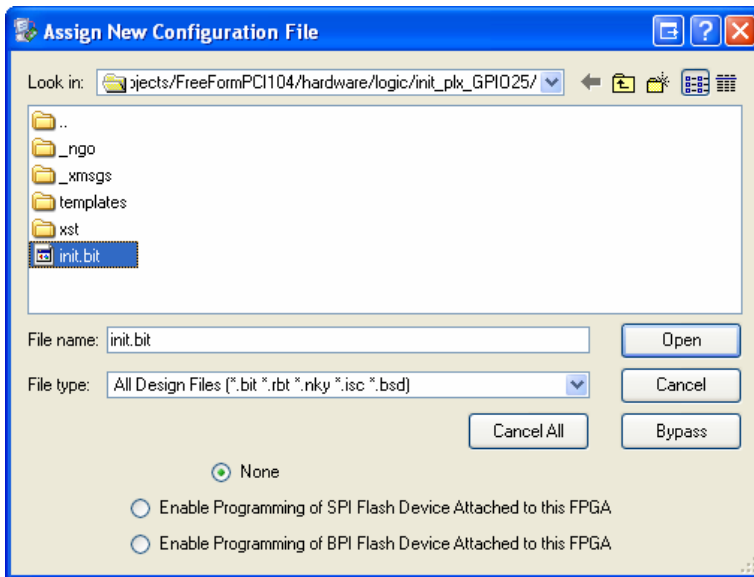
- 1) Open iMPACT, and select create a new project



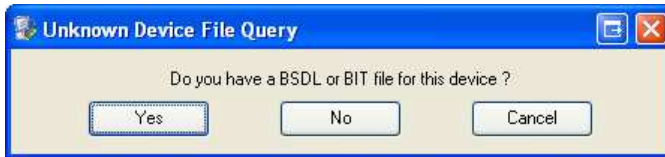
- 2) Select configure devices using boundary scan. iMPACT will scan the JTAG chain, and identify three devices. The first device will be the FPGA.



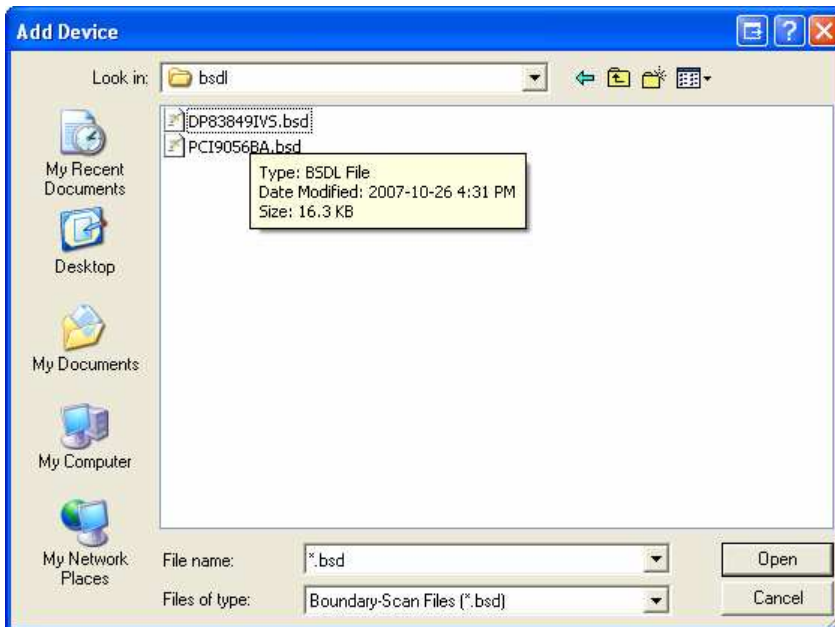
- 3) A prompt will ask for a new configuration file. Select the bitstream from the project directory.



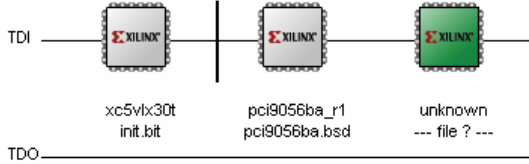
- 4) A prompt will ask for a BSDL file for device number 2 (PLX PCI9056). Click Yes.



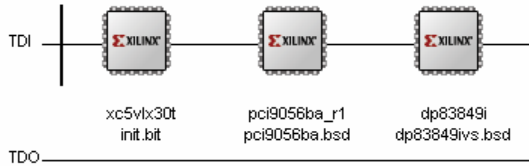
- 5) Browse to the bsd folder and select PCI9056BA.bsd



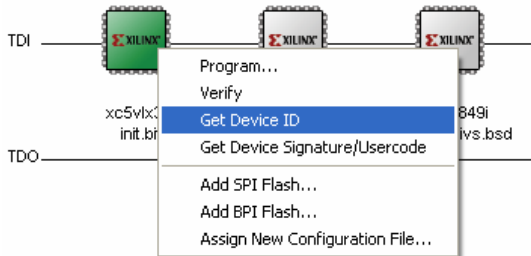
- 6) iMPACT will add the device to the JTAG chain.



- 7) Again, a prompt will ask for device number three (National PHY). Browse to the bsd folder and select DP83849IVS.bsd. The device will be added to the JTAG chain.



- 8) To test stream integrity, right click on the FPGA and select Get Device ID. The console will report IDCODE = 82a6e093

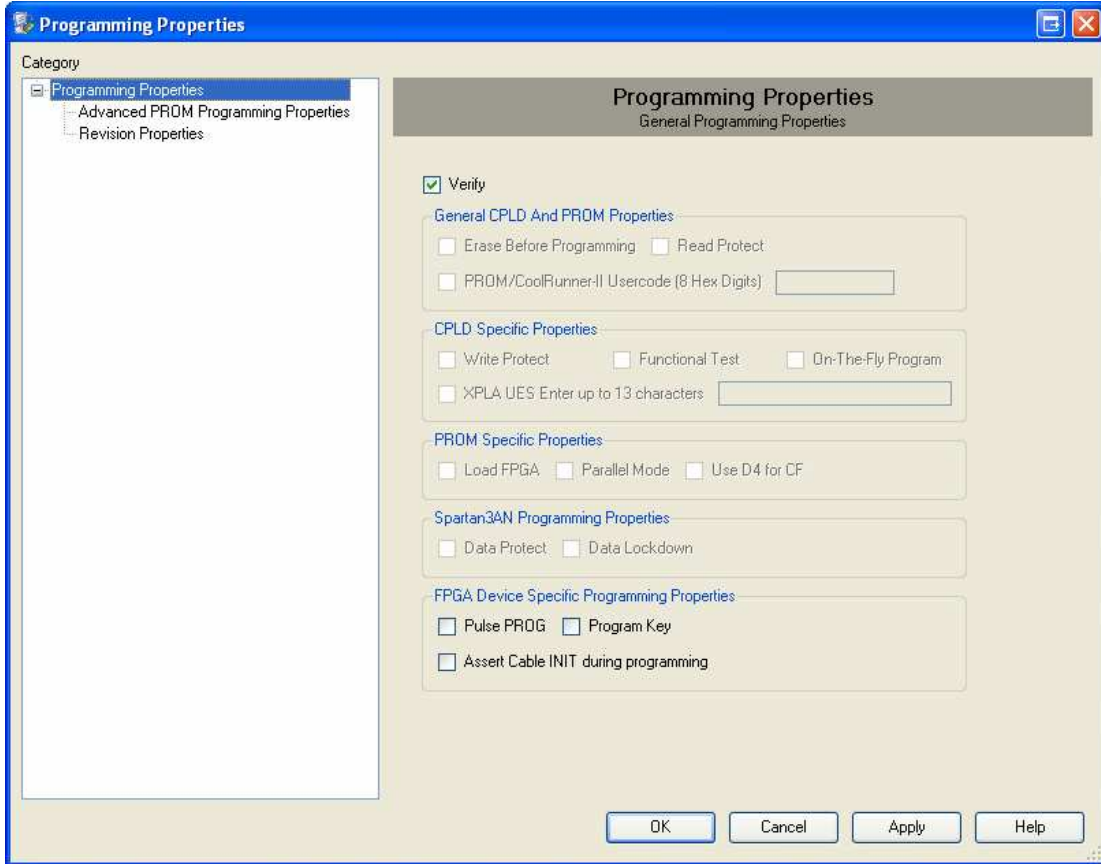


```
// *** BATCH CMD : ReadIdcode -p 1
Maximum TCK operating frequency for this device chain: 10000000.
Validating chain...
Boundary-scan chain validated successfully.
0: Device Temperature: Current Reading: -273.00 C
0: VCCINT Supply: Current Reading: 0.000 V
0: VCCAUX Supply: Current Reading: 0.000 V
'1': IDCODE is '10000010101001101110000010010011'
'1': IDCODE is '82a6e093' (in hex).
'1': : Manufacturer's ID =Xilinx xc5vlx30t, Version : 8
```



## Programming the FPGA

- 1) Right click on device number one (Virtex-5 FPGA), and select program. The following diagram will appear. Note that verification will only work if an msk file has been created.

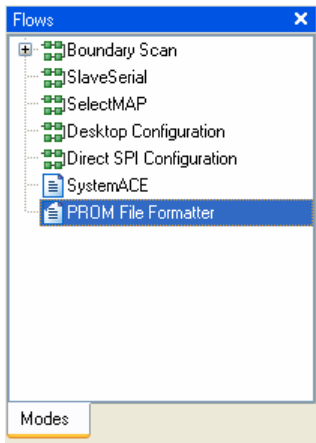


- 2) Select OK to begin programming. After programming is complete, the status window will report:

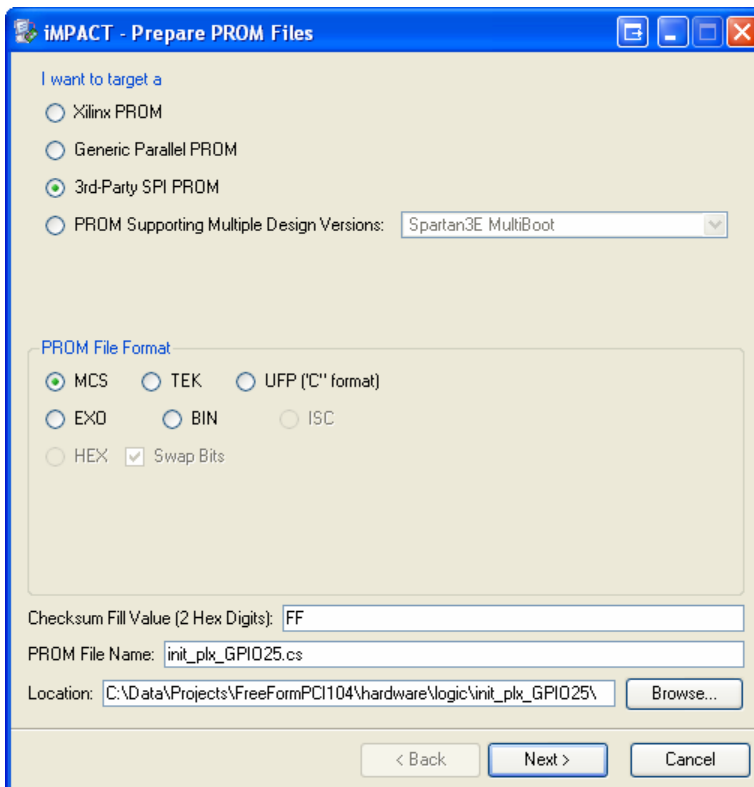
```
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1111 1001 1110 0000 1010 1110 0000
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
'1': Verifying device...INFO:iMPACT:2502 - Complete word count is 9363744/32=292617'.
INFO:iMPACT:2495 - Readback Size is 9363744.
done.
'1': Verification completed successfully.
INFO:iMPACT:579 - '1': Completed downloading bit file to device.
INFO:iMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time =      8 sec. |
```

## Generating a PROM (MCS) File

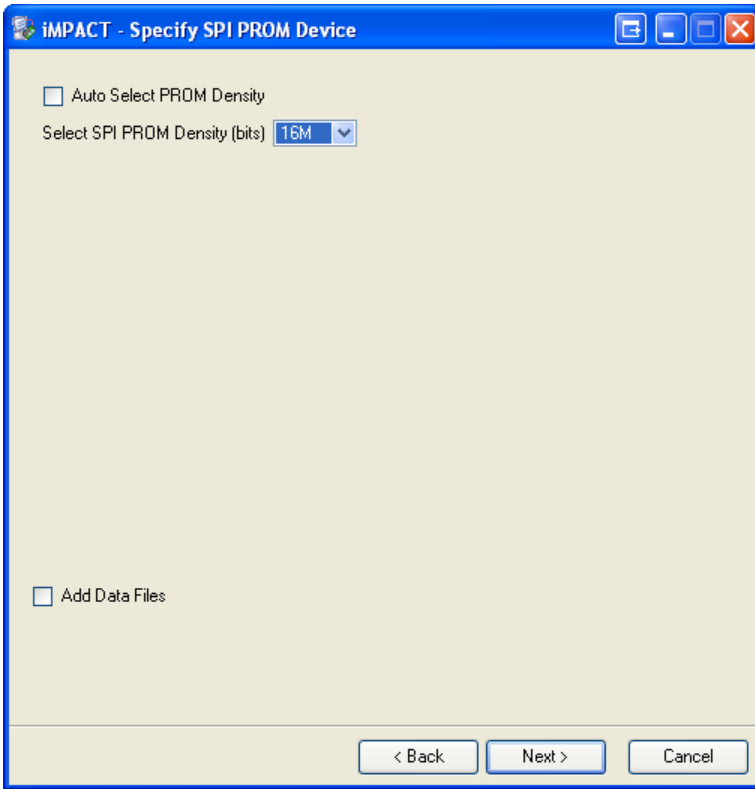
- 1) Double click Prom File Formatter in the Flows window.



- 2) The “Prepare PROM Files” dialog will appear. Ensure that the following settings are selected:  
3<sup>rd</sup> Party SPI PROM  
MSC PROM File Format
- 3) Give the file a name, and click Next.

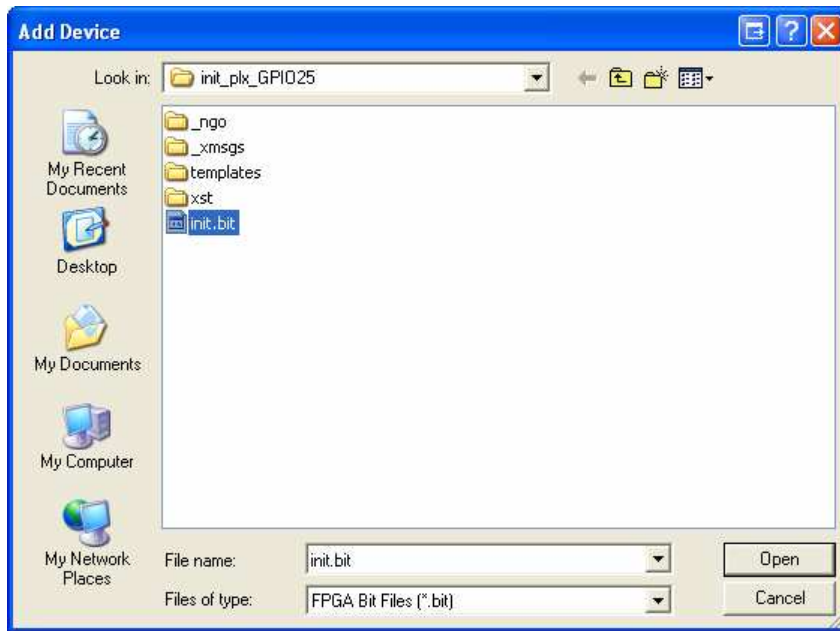


- 4) Select the PROM density (16M) → click Next → click Finish.

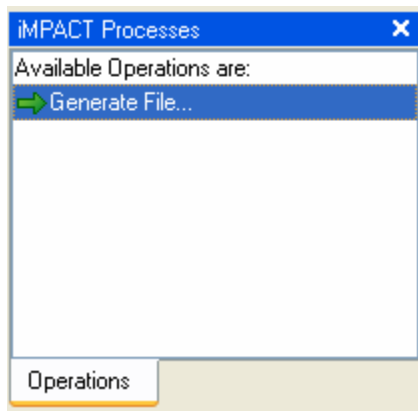


- 5) A prompt will ask to add device to data stream 0. Click OK. Select the bitstream from the project directory.





- 6) Click “No” when asked if another device is to be added. Click “OK” to accept the setup.
- 7) Double Click “Generate File” from the “iMPACT” processes menu. The status will be reported in the console.



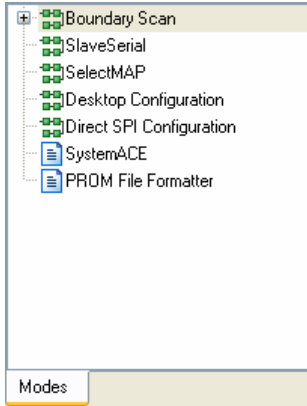
```
// *** BATCH CMD : setMode -pff
// *** BATCH CMD : setSubmode -pffparallel
// *** BATCH CMD : setAttribute -configdevice -attr fillValue -value "FF"
// *** BATCH CMD : setAttribute -configdevice -attr swapBit -value "true"
// *** BATCH CMD : setAttribute -configdevice -attr fileFormat -value "mcs"
// *** BATCH CMD : setAttribute -configdevice -attr dir -value "UP"
// *** BATCH CMD : setAttribute -configdevice -attr path -value
"C:\Data\Projects\FreeFormPCI104\hardware\logic\init_plx_GPIO25\"
// *** BATCH CMD : setAttribute -configdevice -attr name -value "init_plx_GPIO25.cs"
Total configuration bit size = 9371136 bits.
Total configuration byte size = 1171392 bytes.
// *** BATCH CMD : setCurrentDesign -version 0
// *** BATCH CMD : generate -spi
Swap bit can only be disabled in Hex file format only.
0x11dfc0 (1171392) bytes loaded up from 0x0
Using user-specified prom size of 2048K
Writing file
"C:\Data\Projects\FreeFormPCI104\hardware\logic\init_plx_GPIO25\\init_plx_GPIO25.mcs"
.
Writing file
"C:\Data\Projects\FreeFormPCI104\hardware\logic\init_plx_GPIO25\\init_plx_GPIO25.prm"
.
```

## Configuring the FPGA with the SPI Flash

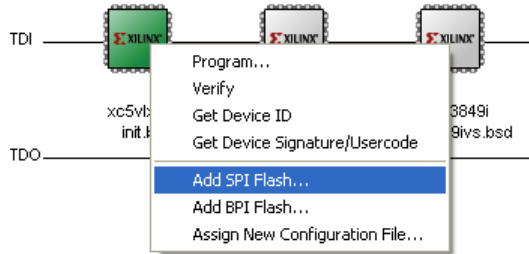
In previous Xilinx FPGA configurations, the SPI flash required programming via 3<sup>rd</sup> party JTAG test software or through in-system methods. The following features are new to ISE 9.1/9.2, and are only available on select FPGAs, including the Virtex-5. Your FreeForm/PCI-104 card featuring the Xilinx Virtex-5 FPGA includes a standard core to enable programming of BPI and SPI flashes over JTAG.

### Configuring the FPGA / SPI flash Association

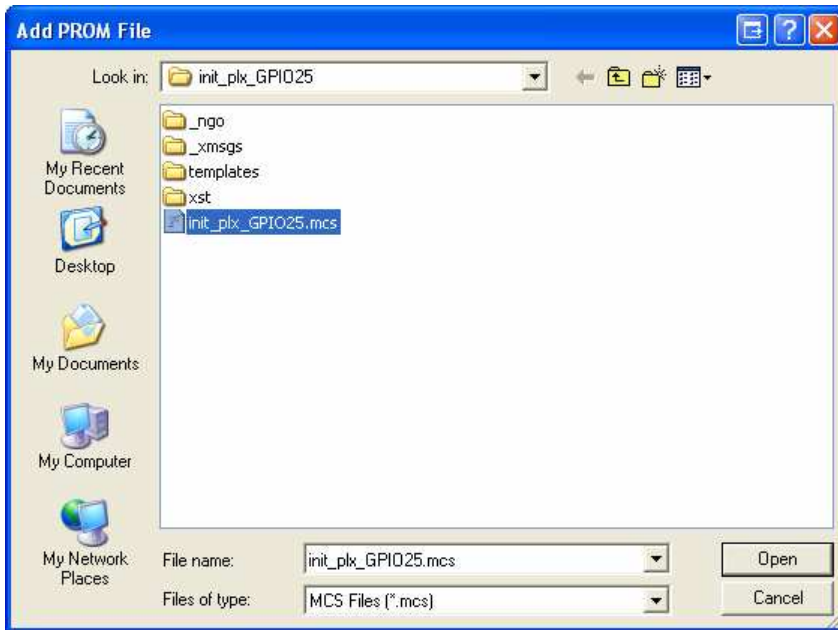
- 1) Select “Boundary Scan” from the “Flows” tab.



- 2) Right click on the FPGA and select “Add SPI Flash...”



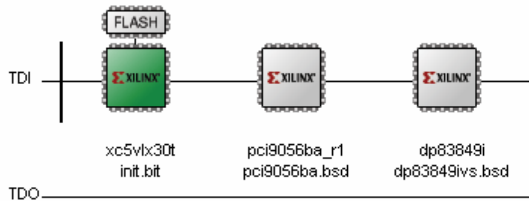
- 3) Browse to the directory containing the previously generated MCS file. Select and click “Open”.



- 4) The “FPGA SPI Flash Association” window will appear; select “M25P16” (this is the flash device connected to the FPGA).



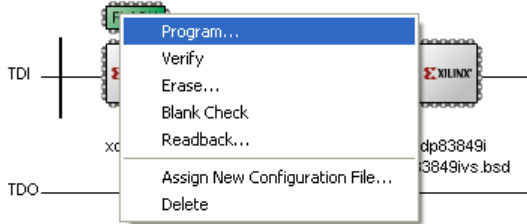
- 5) The flash will be added to the FPGA. Note that this flash is not part of the JTAG chain.



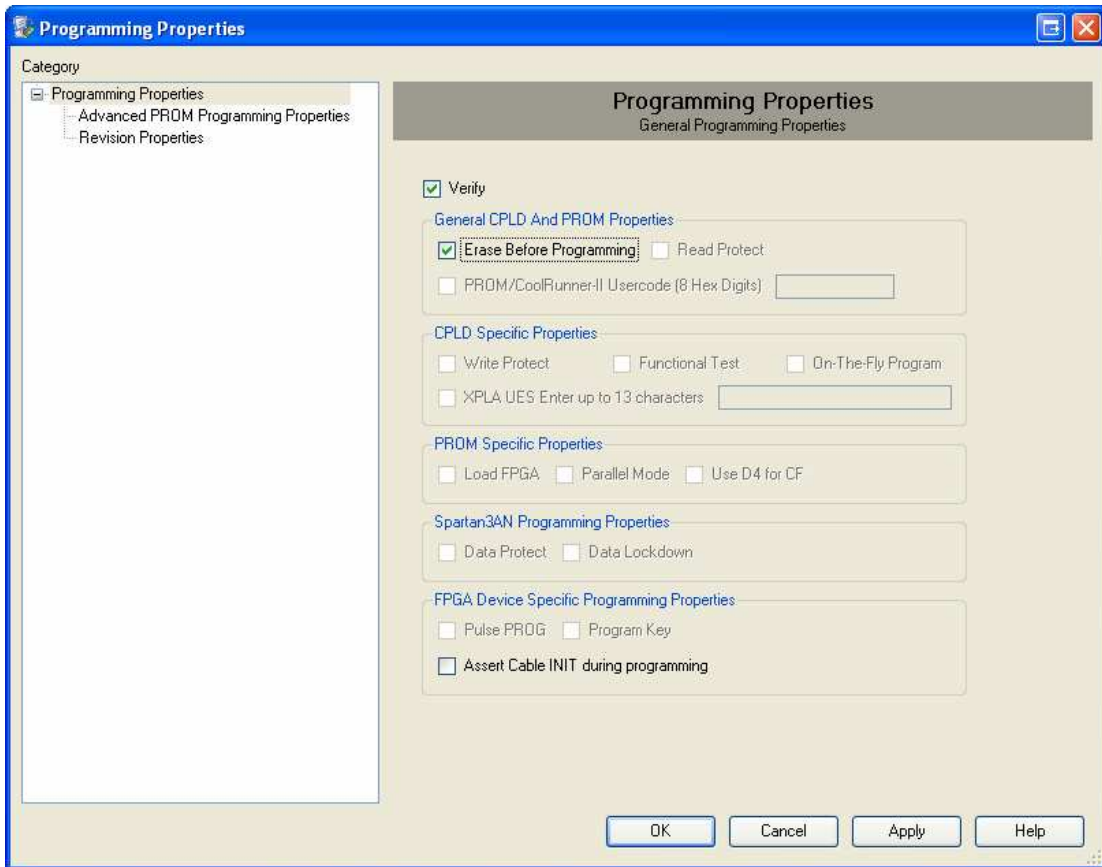
## Programming the Flash

- 1) Right click the previously associated flash device, and select program.

Right click device to select operations



- 2) The programming dialog will appear. Select “Verify” and “Erase Before Programming”, then click “OK.”



- 3) Observe the results in the transcript window.
  - a. The SPI core is first download to the FPGA device
  - b. The IDCODE is checked and verified
  - c. Flash is erased
  - d. Flash is programmed

After completion of the flash programming, the FPGA will attempt to configure itself from the flash. If the SPI flash setting is not selected with [J1](#); this step will fail. This does not mean the flash is not programmed, but rather the verification of the programmed contents has failed.

```
'1': SPI access core not detected. SPI access core will be downloaded to the
device to enable operations.
PROGRESS_START - Starting Operation.
'1': Downloading core...
done.
'1': Reading status register contents...
INFO:IMPACT:2219 - Status register values:
INFO:IMPACT - 0011 1111 1001 1110 0000 1010 1000 0000
INFO:IMPACT:2492 - '1': Completed downloading core to device.
INFO:IMPACT - '1': Checking done pin....done.
'1': Core downloaded successfully.
'1': IDCODE is '202015' (in hex).
'1': ID Check passed.
'1': IDCODE is '202015' (in hex).
'1': ID Check passed.
'1': Erasing Device.
'1': Programming Device.
'1': Reading device contents...
done.
'1': Verification completed.
INFO:IMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
INFO:IMPACT - '1': Checking done pin....done.
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time = 179 sec.
```



## Appendix B: Power calculations

### Scenario 1: Heatsink attached, 250 LFM

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.26375 (w)	16	---	---
Logic	0.01646 (w)	3759	19200	19.6
Signals	0.05521 (w)	7757	---	---
IOs	2.06396 (w)	453	402	112.7
BRAMs	0.15807 (w)	23	36	63.9
DCMs	0.22787 (w)	3	4	75.0
GTP_DUALs	0.20747 (w)	2	4	50.0
TEMACs	0.00000 (w)	1	2	50.0
Total Quiescent Power	<b>0.66765 (w)</b>			
Total Dynamic Power	<b>2.86209 (w)</b>			
Total Power	<b>3.52974 (w)</b>			
Junction Temp	<b>67.3 (degrees C)</b>			

Name	Value	Range
Ambient Temp (degrees C)	50.0	-40.0 to 100.0
Use custom ThetaJA ?	Yes <input type="button" value="v"/>	
Custom ThetaJA (degrees C/w)	4.9	
Airflow (LFM)	NA	0 to 750
Effective ThetaJA (degrees C/w)	4.9	
Max Ambient (degrees C)	82.7	
Junction Temp (degrees C)	<b>67.3</b>	

**Scenario 2: No Heatsink, 250 LFM**

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.26375 (W)	16	---	---
Logic	0.01646 (W)	3759	19200	19.6
Signals	0.05521 (W)	7757	---	---
IOs	2.06396 (W)	453	402	112.7
BRAMs	0.15807 (W)	23	36	63.9
DCMs	0.22787 (W)	3	4	75.0
GTP_DUALs	0.20747 (W)	2	4	50.0
TEMACs	0.00000 (W)	1	2	50.0
<b>Total Quiescent Power</b>	<b>0.68723 (W)</b>			
<b>Total Dynamic Power</b>	<b>2.86209 (W)</b>			
<b>Total Power</b>	<b>3.54933 (W)</b>			
<b>Junction Temp</b>	<b>72.7 (degrees C)</b>			

Name	Value	Range
Ambient Temp (degrees C)	50.0	-40.0 to 100.0
Use custom ThetaJA ?	Yes <input type="button" value="v"/>	
Custom ThetaJA (degrees C/W)	6.4	
Airflow (LFM)	NA	0 to 750
Effective ThetaJA (degrees C/W)	6.4	
Max Ambient (degrees C)	77.3	
Junction Temp (degrees C)	<b>72.7</b>	

**Scenario 3: No heatsink, 0 LFM**

Name	Value	Used	Total Available	Utilization (%)
Clocks	0.26375 (w)	16	---	---
Logic	0.01646 (w)	3759	19200	19.6
Signals	0.05521 (w)	7757	---	---
IDs	2.06396 (w)	453	402	112.7
BRAMs	0.15807 (w)	23	36	63.9
DCMs	0.22787 (w)	3	4	75.0
GTP_DUALs	0.20747 (w)	2	4	50.0
TEMACs	0.00000 (w)	1	2	50.0
Total Quiescent Power	<b>0.73730 (w)</b>			
Total Dynamic Power	<b>2.86209 (w)</b>			
Total Power	<b>3.59939 (w)</b>			
Junction Temp	<b>84.9 (degrees C)</b>			

Name	Value	Range
Ambient Temp (degrees C)	50.0	-40.0 to 100.0
Use custom ThetaJA ?	Yes <input type="button" value="v"/>	
Custom ThetaJA (degrees C/w)	9.7	
Airflow (LFM)	NA	0 to 750
Effective ThetaJA (degrees C/w)	9.7	
Max Ambient (degrees C)	65.1	
Junction Temp (degrees C)	<b>84.9</b>	

## Appendix C: Hardware Changes from Revision B

This appendix lists the changes between hardware revision B and hardware revision C.

The following is a summary of changes:

- PCB requires only 5V over PCI-104; it previously required 3.3V and 5V
- A dedicated local bus oscillator was added to generate 50Mhz. A clock is no longer forwarded from FPGA to the PLX PCI 9056.
- The DDR2 FPGA pinout has been changed to increase timing margins
- The pinout of connector P4 (high-speed serial) has changed. The sideband signals have been relocated and 3.3V has been added.
- The orientation of connector P5 (RS-485 port 0) has rotated 180 degrees
- The Location of P8 (external power connector) has changed. The 3.3V enable signal has also been removed

## Reference Design

The top level reference design contains a generic parameter which will correctly configure the FPGA for Revision B or Revision C. A separate constraint file UCF is created for Revision B and Revision C, which need to be added to the ISE project manually.

### Revision B

#### Local Clock Generation

Pin	Signal Name	Local clock generated in FPGA and forwarded to PLX bridge. Clock feedback to FPGA via pin Y21.
Y21	lb_lclkfb	
A20	lb_lclko_loop	
B21	lb_lclko_plx	

#### DDR2 Pinout

Pin	Signal Name	Pin	Signal Name
AA9	ddr2_a<0>	AD21	ddr2_dq<0>
Y8	ddr2_a<1>	AD15	ddr2_dq<1>
AD8	ddr2_a<2>	AC21	ddr2_dq<2>
Y7	ddr2_a<3>	AD14	ddr2_dq<3>
AB9	ddr2_a<4>	AE13	ddr2_dq<4>
W9	ddr2_a<5>	AE22	ddr2_dq<5>
AC8	ddr2_a<6>	AD16	ddr2_dq<6>
AD6	ddr2_a<7>	AE17	ddr2_dq<7>
AA8	ddr2_a<8>	AF10	ddr2_dq<8>
V8	ddr2_a<9>	AE5	ddr2_dq<9>
AC7	ddr2_a<10>	AE12	ddr2_dq<10>
AB7	ddr2_a<11>	AF3	ddr2_dq<11>
AB6	ddr2_a<12>	AF4	ddr2_dq<12>
AC9	ddr2_a<13>	AF12	ddr2_dq<13>
AE7	ddr2_ba<0>	AF5	ddr2_dq<14>
AA5	ddr2_ba<1>	AF9	ddr2_dq<15>
V9	ddr2_ba<2>	AD24	ddr2_dq<16>
AE8	ddr2_cas_n	AE25	ddr2_dq<17>
AE11	ddr2_ck<0>	AC26	ddr2_dq<18>
AD11	ddr2_ck_n<0>	AC23	ddr2_dq<19>
AD18	ddr2_cke<0>	AB22	ddr2_dq<20>
AC22	ddr2_cs_n<0>	AC24	ddr2_dq<21>
AE16	ddr2_dm<0>	AE26	ddr2_dq<22>
AE6	ddr2_dm<1>	AD26	ddr2_dq<23>
AD25	ddr2_dm<2>	AD23	ddr2_dq<24>
AE18	ddr2_dm<3>	AE15	ddr2_dq<25>
AD19	ddr2_dqs<0>	AF24	ddr2_dq<26>
AF7	ddr2_dqs<1>	AF13	ddr2_dq<27>
AF20	ddr2_dqs<2>	AF14	ddr2_dq<28>
AF22	ddr2_dqs<3>	AF25	ddr2_dq<29>
AD20	ddr2_dqs_n<0>	AF15	ddr2_dq<30>
AF8	ddr2_dqs_n<1>	AF23	ddr2_dq<31>
AE20	ddr2_dqs_n<2>	AD13	ddr2_odt<0>
AE21	ddr2_dqs_n<3>	AA7	ddr2_ras_n
		AB5	ddr2_we_n

### Revision C

Pin	Signal Name	Dedicated oscillator generates local bus clock. Clock is driven to FPGA on pin Y21, which drives an internal global clock net.
Y21	lb_lclkfb	
A20		
B21		

Pin	Signal Name	Pin	Signal Name
AA9	ddr2_a<0>	AC21	ddr2_dq<0>
Y8	ddr2_a<1>	AD15	ddr2_dq<1>
AD8	ddr2_a<2>	AC23	ddr2_dq<2>
Y7	ddr2_a<3>	AE13	ddr2_dq<3>
AB9	ddr2_a<4>	AD14	ddr2_dq<4>
W9	ddr2_a<5>	AE22	ddr2_dq<5>
AE8	ddr2_a<6>	AD16	ddr2_dq<6>
AD6	ddr2_a<7>	AD21	ddr2_dq<7>
AA8	ddr2_a<8>	AF10	ddr2_dq<8>
V8	ddr2_a<9>	AE5	ddr2_dq<9>
AC7	ddr2_a<10>	AE12	ddr2_dq<10>
AB7	ddr2_a<11>	AF3	ddr2_dq<11>
AB6	ddr2_a<12>	AF4	ddr2_dq<12>
AD10	ddr2_a<13>	AF12	ddr2_dq<13>
AE7	ddr2_ba<0>	AF5	ddr2_dq<14>
AA5	ddr2_ba<1>	AF9	ddr2_dq<15>
V9	ddr2_ba<2>	AC26	ddr2_dq<16>
AC9	ddr2_cas_n	AE26	ddr2_dq<17>
AE11	ddr2_ck<0>	AC24	ddr2_dq<18>
AD11	ddr2_ck_n<0>	AD24	ddr2_dq<19>
AC8	ddr2_cke<0>	AE25	ddr2_dq<20>
W8	ddr2_cs_n<0>	AB22	ddr2_dq<21>
AE16	ddr2_dm<0>	AD26	ddr2_dq<22>
AE6	ddr2_dm<1>	AD25	ddr2_dq<23>
AE17	ddr2_dm<2>	AD23	ddr2_dq<24>
AE18	ddr2_dm<3>	AE15	ddr2_dq<25>
AD19	ddr2_dqs<0>	AF25	ddr2_dq<26>
AF7	ddr2_dqs<1>	AF13	ddr2_dq<27>
AF20	ddr2_dqs<2>	AF14	ddr2_dq<28>
AF22	ddr2_dqs<3>	AF24	ddr2_dq<29>
AD20	ddr2_dqs_n<0>	AF15	ddr2_dq<30>
AF8	ddr2_dqs_n<1>	AF23	ddr2_dq<31>
AE20	ddr2_dqs_n<2>	AD9	ddr2_odt<0>
AE21	ddr2_dqs_n<3>	AA7	ddr2_ras_n
		AB5	ddr2_we_n

## Hardware Description

### Connector Pinouts

#### High-speed Serial (P4)

The sideband LVCMOS signals (HSS) have been rearranged so that when two FreeForm units are connected:

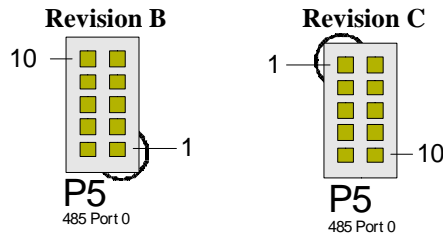
HSS\_USER\_IO(0) maps to HSS\_USER\_IO(2)  
 HSS\_USER\_IO(1) maps to HSS\_USER\_IO(3)

Also, 3.3V pins replace the GND pins; this is because the connector has embedded GND blades.

Revision B		Revision C	
Pin	Signal	Pin	Signal
1	MTGRXN0_112	1	MTGRXN0_112
3	MTGRXP0_112	3	MTGRXP0_112
2	MTGTXXN0_112	2	MTGTXXN0_112
4	MTGTXP0_112	4	MTGTXP0_112
5	GND	5	HSS_USER_IO(0)
7	GND	7	HSS_USER_IO(1)
6	HSS_USER_IO(0)	6	HSS_USER_IO(2)
8	HSS_USER_IO(1)	8	HSS_USER_IO(3)
9	MTGRXN1_112	9	MTGRXN1_112
11	MTGRXP1_112	11	MTGRXP1_112
10	MTGTXXN1_112	10	MTGTXXN1_112
12	MTGTXP1_112	12	MTGTXP1_112
13	GND	13	3.3V
15	GND	15	3.3V
14	GND	14	3.3V
16	GND	16	3.3V
17	MTGRXN0_114	17	MTGRXN0_114
19	MTGRXP0_114	19	MTGRXP0_114
18	MTGTXXN0_114	18	MTGTXXN0_114
20	MTGTXP0_114	20	MTGTXP0_114
21	GND	21	3.3V
23	GND	23	3.3V
22	HSS_USER_IO(2)	22	3.3V
24	HSS_USER_IO(3)	24	3.3V
25	MTGRXN1_114	25	MTGRXN1_114
27	MTGRXP1_114	27	MTGRXP1_114
26	MTGTXXN1_114	26	MTGTXXN1_114
28	MTGTXP1_114	28	MTGTXP1_114

#### RS-485 Headers (P5)

The orientation of the connector has changed. The pinout remains the same.



**External Power Connector (P8)**

The connector no longer enables 3.3V regulation – it is always enabled.

Revision B		Revision C	
Pin	Signal	Pin	Signal
1	5V	1	5V
2	3.3 enable (connect to 5V)	2	
3	GND	3	GND
4	VIO (connect to 5V)	4	VIO (connect to 5V)

**Specifications**

	Revision B	Revision C
<b>Power Requirements</b>	+3.3V DC and +5V DC, in PCI-104 stack +5V DC stand-alone  Current requirements are configuration dependant.	+5V DC, in PCI-104 stack +5V DC stand-alone