MPR603HSU-03
(IBM Order Number)

MPC603EC/D
(Motorola Order Number)

5/95
REV 2

PowerPC™

Advance Information

PowerPC 603™ RISC Microprocessor Hardware Specifications

The PowerPC 603 microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical characteristics of the 603. For functional characteristics of the processor, refer to the *PowerPC 603 RISC Microprocessor User's Manual.*

This document contains the following topics:

In this document, the term "603" is used as an abbreviation for the phrase, "PowerPC 603 Microprocessor." The PowerPC 603 microprocessors are available from Motorola as MPC603 and from IBM as PPC603.

IBM

MOTOROLA

1.1 Overview

The 603 is the first low-power implementation of the PowerPC microprocessor family of RISC microprocessors. The 603 implements the 32-bit portion of the PowerPC Architecture™ specification, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The 603 provides four software controllable power-saving modes. Three of the modes (doze, nap, and sleep modes) are static in nature, and progressively reduce the amount of power dissipated by the processor. The fourth is a dynamic power management mode that causes the functional units in the 603 to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The 603 is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the 603 makes completion appear sequential.

The 603 integrates five execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for 603-based systems. Most integer instructions execute in one clock cycle. The FPU is pipelined so a single-precision multiply-add instruction can be issued every clock cycle.

The 603 provides independent on-chip, 8-Kbyte, two-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least recently used (LRU) replacement algorithm. The 603 also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The 603 has a selectable 32- or 64-bit data bus and a 32-bit address bus. The 603 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The 603 provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The 603 supports single-beat and burst data transfers for memory accesses; it also supports both memory-mapped I/O and direct-store addressing.

The 603 uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

1.1.1 PowerPC 603 Microprocessor Features

Major features of the 603 are as follows:

- High-performance, superscalar microprocessor
  - — As many as three instructions issued and retired per clock
  - — As many as five instructions in execution per clock
  - — Single-cycle execution for most instructions
  - — Pipelined FPU for all single-precision and most double-precision operations

- Five independent execution units and two register files
  - BPU featuring static branch prediction
  - A 32-bit IU
  - Fully IEEE 754-compliant FPU for both single- and double-precision operations
  - LSU for data transfer between data cache and GPRs and FPRs
  - SRU that executes condition register (CR) and special-purpose register (SPR) instructions
  - Thirty-two GPRs for integer operands
  - Thirty-two FPRs for single- or double-precision operands
- High instruction and data throughput
  - Zero-cycle branch capability (branch folding)
  - Programmable static branch prediction on unresolved conditional branches
  - Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - A six-entry instruction queue that provides look-ahead capability
  - Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - 8-Kbyte data cache—two-way set-associative, physically addressed; LRU replacement algorithm
  - 8-Kbyte instruction cache—two-way set-associative, physically addressed; LRU replacement algorithm
  - Cache write-back or write-through operation programmable on a per page or per block basis
  - BPU that performs CR look-ahead operations
  - Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - A 64-entry, two-way set-associative ITLB
  - A 64-entry, two-way set-associative DTLB
  - Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - Software table search operations and updates supported through fast trap mechanism
  - 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - A 32- or 64-bit split-transaction external data bus with burst transfers
  - Support for one-level address pipelining and out-of-order bus transactions
  - Bus extensions for direct-store operations
- Integrated power management
  - Low-power 3.3 volt design
  - Internal processor/bus clock multiplier that provides 1/1, 2/1, 3/1 and 4/1 ratios
  - Three power saving modes: doze, nap, and sleep
  - Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through JTAG boundary-scan capability

1.2 General Parameters

The following list provides a summary of the general parameters of the 603.

Technology	0.5 μ CMOS (four-layer metal)
Die size	11.5 mm x 7.4 mm
Transistor count	1.6 million
Logic design	Fully-static
Max. internal frequency	80 MHz
Max. bus frequency	66.67 MHz
Package	Surface mount, 240-pin CQFP
Power supply	3.3 ± 5% V dc

For ordering information, refer to Section 1.8, “Ordering Information.”

1.3 Electrical and Thermal Characteristics

This section provides both the AC and DC electrical specifications and thermal characteristics for the 603. The following specifications are preliminary and subject to change without notice.

1.3.1 DC Electrical Characteristics

Table 1 and Table 2 provide the absolute maximum ratings, thermal characteristics, and DC electrical characteristics for the 603.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Supply voltage	Vdd	–0.3 to 4.0	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes: 1. Functional operating conditions are given in AC and DC electrical specifications. Stresses beyond the maximum listed may affect device reliability or cause permanent damage to the device.

2. **Caution**: Input voltage must not be greater than the supply voltage by more than 2.5 V at all times including during power-on reset.

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Rating
Motorola wire-bond CQFP package thermal resistance, junction-to-case (typical)	θ_{JC}	2.2	°C/W
IBM C4-CQFP package thermal resistance, junction-to-heat sink base	θ_{JS}	1.1	°C/W

Note: Refer to Section 1.7, “System Design Information,” for more information about thermal management.

Table 3 provides the DC electrical characteristics for the 603.

Table 3. DC Electrical Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

Characteristic	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.2	5.5	V
Input low voltage (all inputs except SYSCLK)	V_{IL}	GND	0.8	V
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V
SYSCLK input low voltage	CV_{IL}	GND	0.4	V
Input leakage current, V_{in} = 3.465 V[1]	I_{in}	—	10	µA
V_{in} = 5.5 V[1]	I_{in}	—	TBD	µA
Hi-Z (off-state) leakage current, V_{in} = 3.465 V[1]	I_{TSI}	—	10	µA
V_{in} = 5.5 V[1]	I_{TSI}	—	TBD	µA
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 14 mA	V_{OL}	—	0.4	V
Capacitance, V_{in} = 0 V, f = 1 MHz[2] (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	10.0	pF
Capacitance, V_{in} = 0 V, f = 1 MHz[2] (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	15.0	pF

Notes: 1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK, and JTAG signals). For detailed leakage information, please contact your local Motorola or IBM sales office.

2. Capacitance is periodically sampled rather than 100% tested.

Table 4 provides the power dissipation for the 603.

Table 4. Power Dissipation

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_j \le 105$ °C

CPU Clock: SYSCLK		Bus Frequency (SYSCLK)					Unit
		25 MHz	33 MHz	40 MHz	50 MHz	66 MHz	
Full-On Mode							
1:1	Typical					1.8	W
	Max.					2.5	W
2:1	Typical		1.8	2.0			W
	Max.		2.5	2.9			W
Doze Mode[1]							
1:1	Typical					740	mW
2:1	Typical		745	800			mW

Table 4. Power Dissipation (Continued)

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T_j ≤ 105 °C

CPU Clock: SYSCLK	Bus Frequency (SYSCLK)					Unit
	25 MHz	33 MHz	40 MHz	50 MHz	66 MHz	
Nap Mode[1]						
1:1 Typical					160	mW
2:1 Typical		140	160			mW
Sleep Mode[1]						
1:1 Typical					125	mW
2:1 Typical		110	130			mW
Sleep Mode—PLL Disabled[1]						
1:1 Typical					70	mW
2:1 Typical		30	40			mW
Sleep Mode—PLL and SYSCLK Disabled[1]						
1:1 Typical					2.0	mW
2:1 Typical		2.0	2.0			mW

Note: 1. The values provided for this mode do not include pad driver power (OVDD) or analog supply power (AVDD). Worst-case AVDD = 15 mW.

1.3.2 AC Electrical Characteristics

This section provides the clock and AC electrical characteristics for the 603.

1.3.2.1 Clock AC Specifications

Table 5 provides the clock AC timing specifications as defined in Figure 1. These specifications are for 25, 33.33, 40, 50, and 66.67 MHz bus clock (SYSCLK) frequencies.

Table 5. Clock AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
	Frequency of operation	16.67	25.0	25.0	33.33	33.33	40.0	40.0	50.0	50.0	66.67	MHz	
1	SYSCLK cycle time	40.0	60.0	30.0	40.0	25.0	30.0	20.0	25.0	15.0	20.0	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	ns	1
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	40.0	60.0	%	3

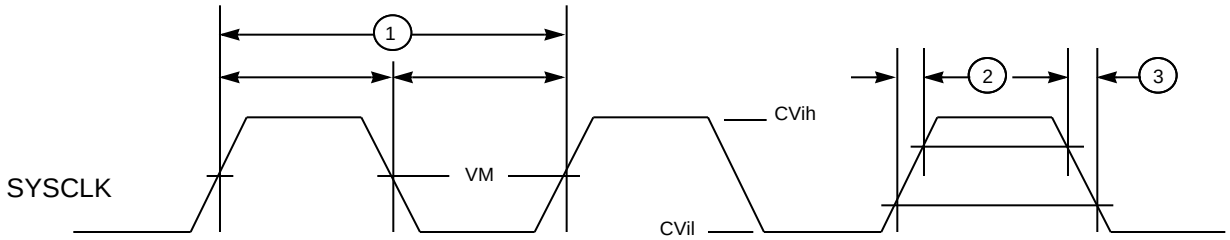
Table 5. Clock AC Timing Specifications (Continued)

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_J \le 105$ °C

Num	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
8	SYSCLK short- and long-term jitter	—	±150	—	±150	—	±150	—	±150	—	±150	ps	2
9	603 internal PLL relock time	—	100	—	100	—	100	—	100	—	100	µs	3,4

Notes: 1. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.

2. This is the sum total of both short- and long-term jitter, and is guaranteed by design.
3. Timing is guaranteed by design and characterization, and is not tested.
4. PLL relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 µs) during the power-on reset sequence.
5. **Caution**: The SYSCLK frequency and PLL_CFG0–PLL_CFG3 settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG0–PLL_CFG3 signal description in Section 1.7, “System Design Information,” for valid PLL_CFG0–PLL_CFG3 settings, and to Section 1.8, “Ordering Information,” for available frequencies and part numbers.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.3.2.2 Input AC Specifications

Table 6 provides the input AC timing specifications for the 603 as defined in Figure 2 and Figure 3. These specifications are for 25, 33.33, 40, 50, and 66.67 MHz bus clock (SYSCLK) frequencies.

Table 6. Input AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, $0 \le T_J \le 105$ °C

Num	Characteristic	25 MHz		33.33 MHz		40 MHz		50 MHz		66.67 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	4.5	—	4.0	—	3.5	—	3.0	—	2.5	—	ns	2
10b	All other inputs valid to SYSCLK (input setup)	6.5	—	6.0	—	5.5	—	5.0	—	4.5	—	ns	3
10c	Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$)	8 * t_{sys}	—	8 * t_{sys}	—	8 * t_{sys}	—	8 * t_{sys}	—	8 * t_{sys}	—	ns	4,5, 6,7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	2
11b	SYSCLK to all other inputs invalid (input hold)	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$)	0	—	0	—	0	—	0	—	0	—	ns	4,6,7

Notes: 1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 2.

2. Address/data/transfer attribute input signals are composed of the following: A0–A31, AP0–AP3, TT0–TT4, TC0–TC1, $\overline{\text{TBST}}$, TSIZ0–TSIZ2, $\overline{\text{GBL}}$, DH0–DH31, DL0–DL31, DP0–DP7.

3. All other input signals are composed of the following: $\overline{\text{TS}}$, $\overline{\text{XATS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$,$\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.

4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$. See Figure 3.

5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds.

6. These values are guaranteed by design, and are not tested.

7. This specification is for configuration mode only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 μs) during the power-on reset sequence.

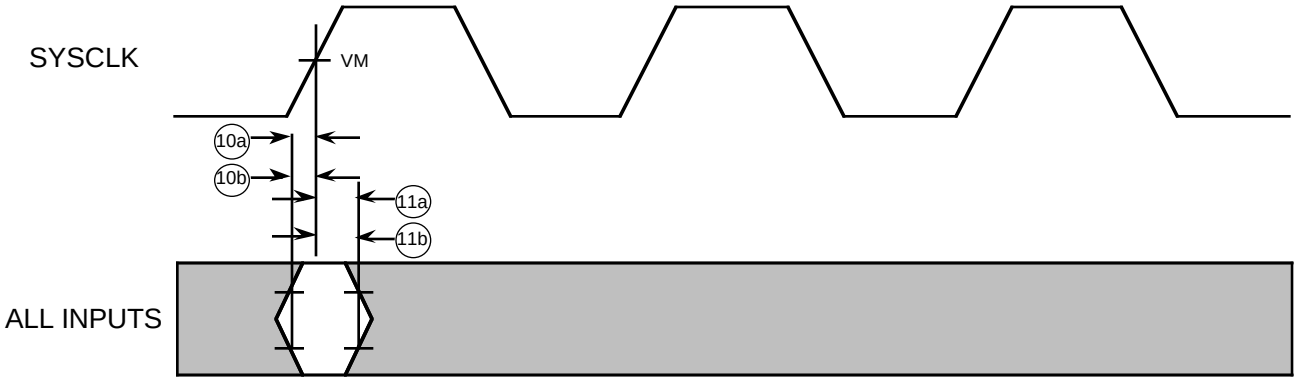


Figure 2. Input Timing Diagram

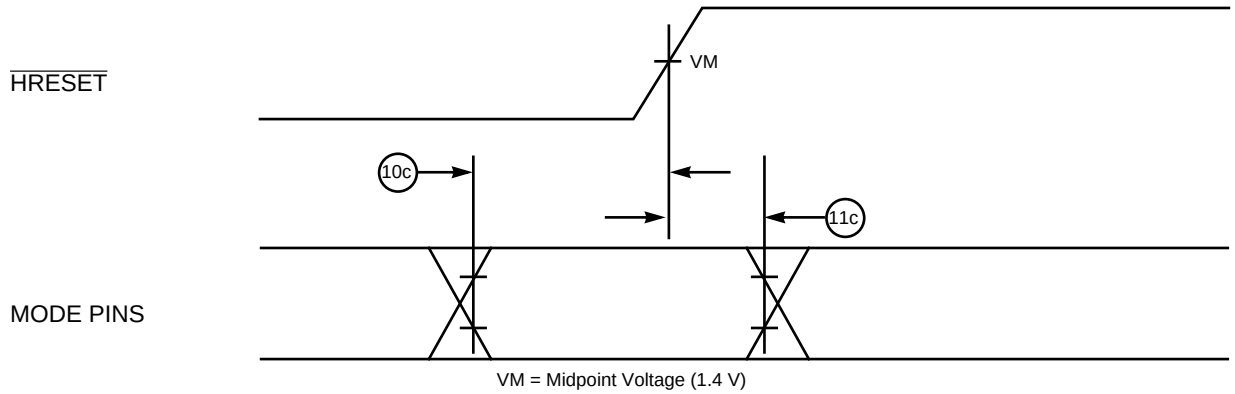


Figure 3. Mode Select Input Timing Diagram

1.3.2.3 Output AC Specifications

Table 7 provides the output AC timing specifications for the 603 (shown in Figure 4). These specifications are for 25, 33.33, 40, 50, and 66.67 MHz bus clock (SYSCLK) frequencies.

Table 7. Output AC Timing Specifications

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	25		33.33		40		50		66.67		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V— $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	14.0	—	13.0	—	12.0	—	11.0	—	10.0	ns	4
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	13.0	—	12.0	—	11.0	—	10.0	—	9.0	ns	6

Table 7. Output AC Timing Specifications (Continued)

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	25		33.33		40		50		66.67		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
14a	SYSCLK to output valid (5.5 V to 0.8 V— all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	16.0	—	15.0	—	14.0	—	13.0	—	12.0	ns	4
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	14.0	—	13.0	—	12.0	—	11.0	—	10.0	ns	6
15	SYSCLK to output invalid (output hold)	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	3
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	—	12.5	—	11.5	—	10.5	—	9.5	—	8.5	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	—	1.0	—	1.0	—	1.0	—	1.0	—	1.2	t_{sys}	5, 7
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	—	12.0	—	11.0	—	10.0	—	9.0	—	8.0	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 * t_{sys} + 1.0	—	0.2 * t_{sys} + 1.0	—	0.2 * t_{sys} + 1.0	—	0.2 * t_{sys} + 1.0	—	0.2 * t_{sys} + 1.0	—	ns	3, 5, 8
20	Maximum delay to $\overline{ARTRY}$ precharge	—	1.0	—	1.0	—	1.0	—	1.0	—	1.2	t_{sys}	5, 8
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	—	2.0	—	2.0	—	2.0	—	2.0	—	2.25	t_{sys}	5, 8

Notes: 1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin. See Figure 4.

2. All maximum timing specifications assume C_L = 50 pF.

3. This minimum parameter assumes C_L = 0 pF.

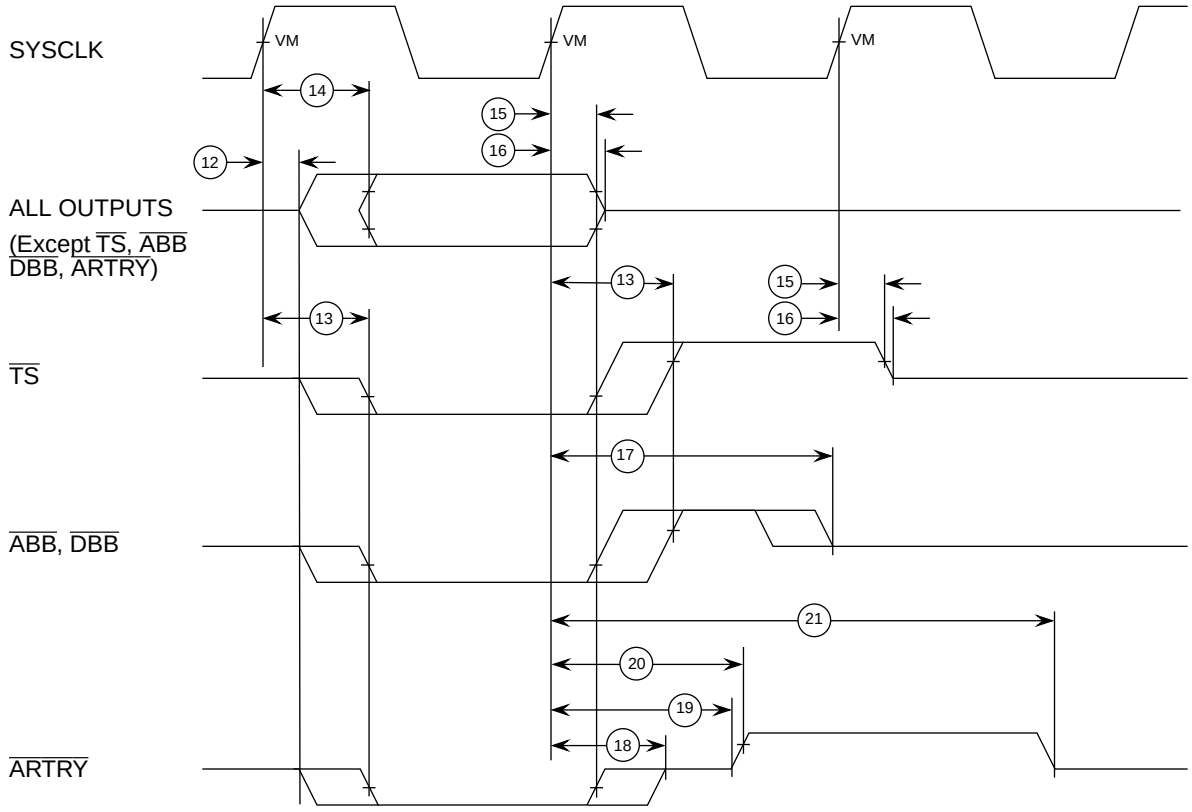
4. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5 V CMOS levels instead of 3.3 V CMOS levels).

5. t_{SYS} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.

6. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.

7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.

8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.



VM = Midpoint Voltage (1.4 V)

Figure 4. Output Timing Diagram

1.3.3 JTAG AC Timing Specifications

Table 8 provides the JTAG AC timing specifications.

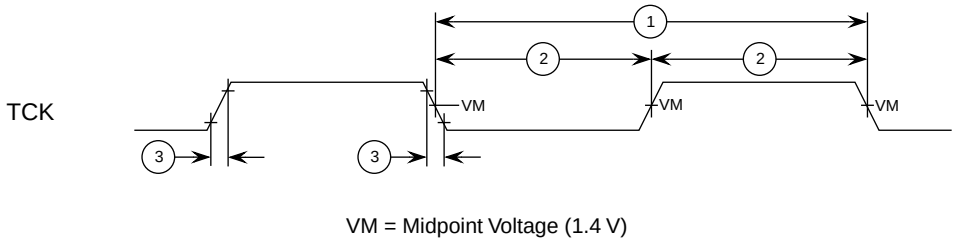
Table 8. JTAG AC Timing Specifications (Independent of SYSCLK)

Vdd = 3.3 ± 5% V dc, GND = 0 V dc, C_L = 50 pF, 0 ≤ T_J ≤ 105 °C

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	6	—	ns	2
7	Boundary-scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3
9	TCK to output high impedance	3	24	ns	3
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes: 1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 5 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 5. Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

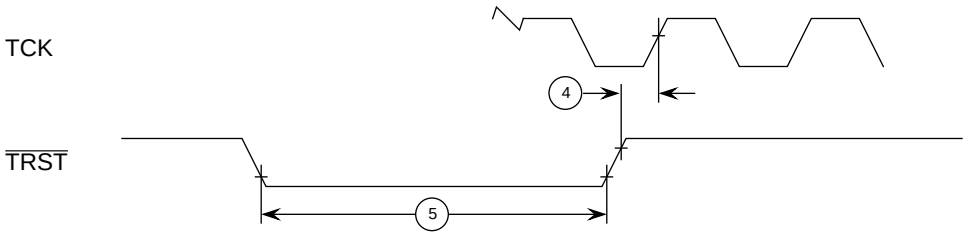


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

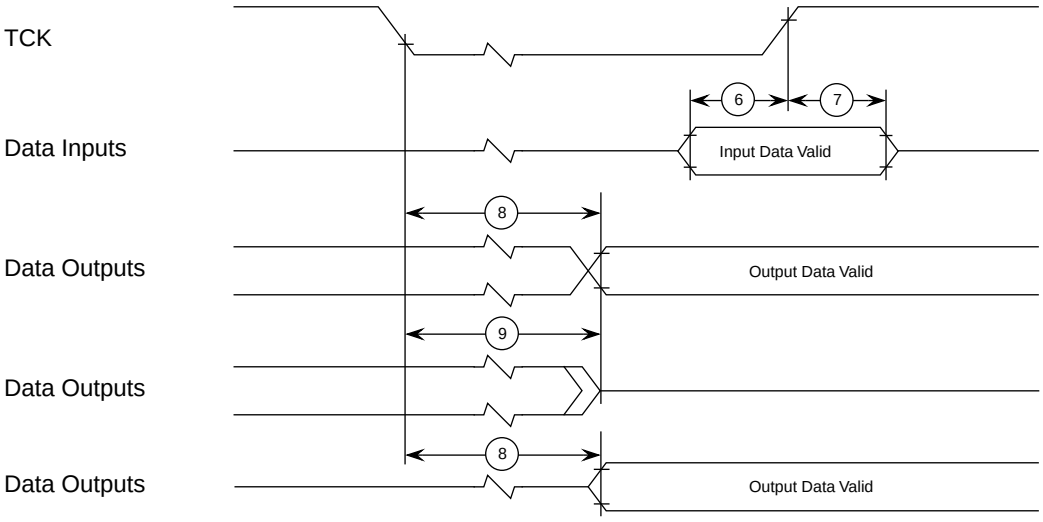


Figure 7. Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

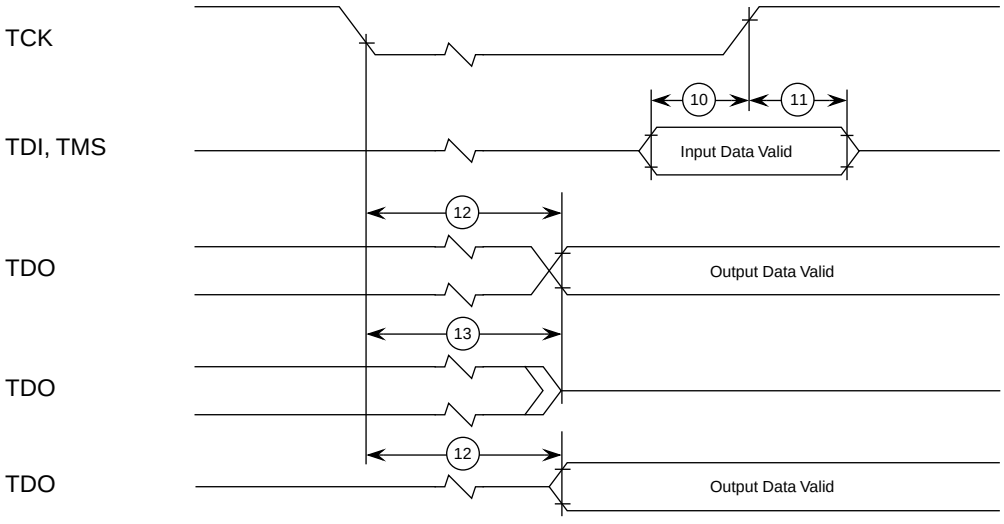


Figure 8. Test Access Port Timing Diagram

1.4 Pinout Diagram

Figure 9 contains the pin assignments for the 603.

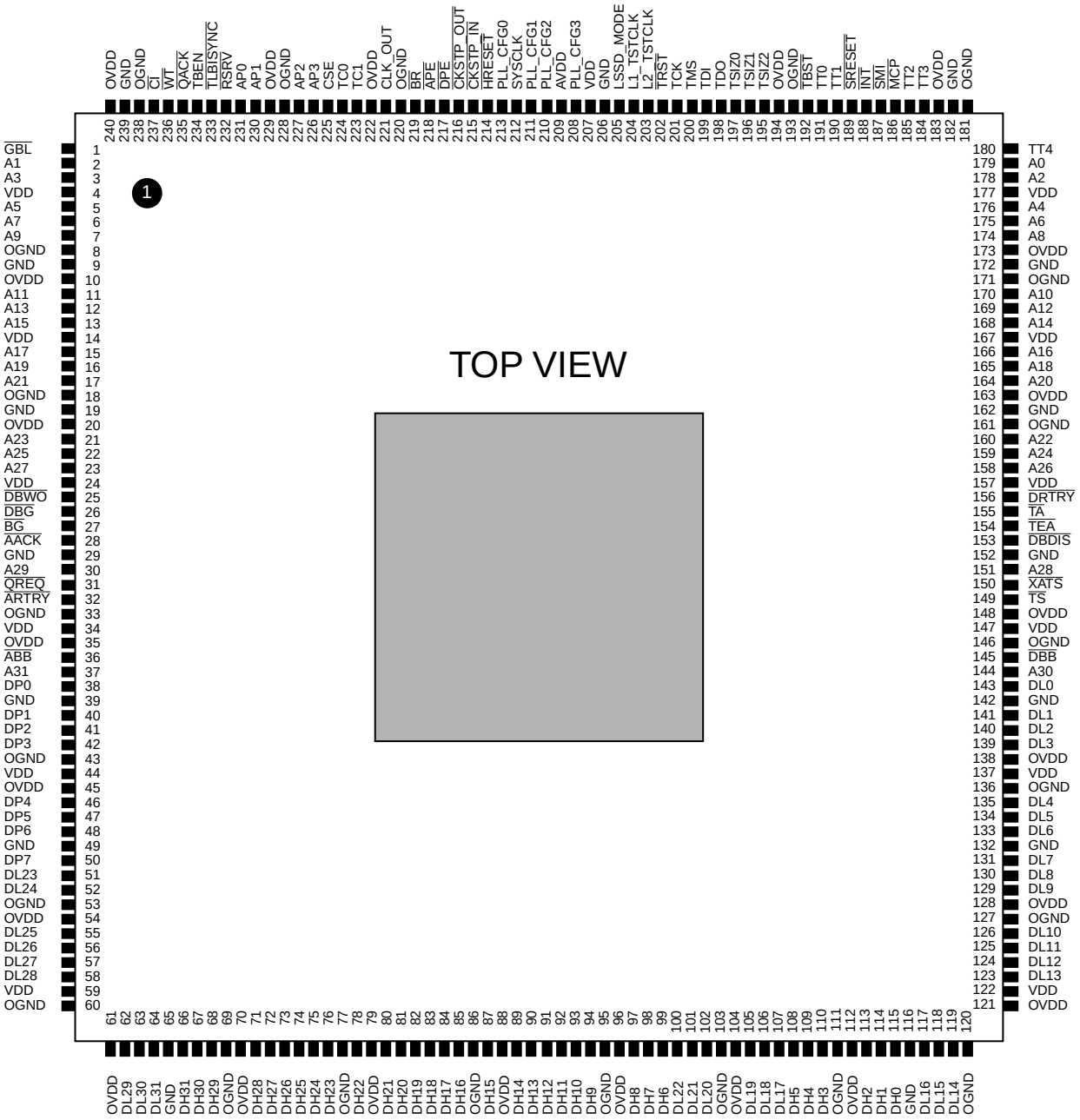


Figure 9. PowerPC 603 Microprocessor Pin Assignments

1.5 Pinout Listing

Table 9 provides the pinout listing for the 603.

Table 9. PowerPC 603 Microprocessor Pinout Listing

Signal Name	Pin Number	Active	I/O
A0–A31	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37	High	I/O
$\overline{\text{AACK}}$	28	Low	Input
$\overline{\text{ABB}}$	36	Low	I/O
AP0–AP3	231, 230, 227, 226	High	I/O
$\overline{\text{APE}}$	218	Low	Output
$\overline{\text{ARTRY}}$	32	Low	I/O
AVDD	209	High	Input
$\overline{\text{BG}}$	27	Low	Input
$\overline{\text{BR}}$	219	Low	Output
$\overline{\text{CI}}$	237	Low	Output
CLK_OUT	221	—	Output
$\overline{\text{CKSTP\_IN}}$	215	Low	Input
$\overline{\text{CKSTP\_OUT}}$	216	Low	Output
CSE	225	High	Output
$\overline{\text{DBB}}$	145	Low	I/O
$\overline{\text{DBDIS}}$	153	Low	Input
$\overline{\text{DBG}}$	26	Low	Input
$\overline{\text{DBWO}}$	25	Low	Input
DH0–DH31	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66	High	I/O
DL0–DL31	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64	High	I/O
DP0–DP7	38, 40, 41, 42, 46, 47, 48, 50	High	I/O
$\overline{\text{DPE}}$	217	Low	Output
$\overline{\text{DRTRY}}$	156	Low	Input
$\overline{\text{GBL}}$	1	Low	I/O
GND	9, 19, 29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239	Low	Input

Table 9. PowerPC 603 Microprocessor Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{HRESET}}$	214	Low	Input
$\overline{\text{INT}}$	188	Low	Input
$\overline{\text{LSSD\_MODE}}$[1]	205	Low	Input
L1_TSTCLK[1]	204	—	Input
L2_TSTCLK[1]	203	—	Input
$\overline{\text{MCP}}$	186	Low	Input
OGND	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238	Low	Input
OVDD	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	High	Input
PLL_CFG0–PLL_CFG3	213, 211, 210, 208	High	Input
$\overline{\text{QACK}}$	235	Low	Input
$\overline{\text{QREQ}}$	31	Low	Output
$\overline{\text{RSRV}}$	232	Low	Output
$\overline{\text{SMI}}$	187	Low	Input
$\overline{\text{SRESET}}$	189	Low	Input
SYSCLK	212	—	Input
$\overline{\text{TA}}$	155	Low	Input
TBEN	234	High	Input
$\overline{\text{TBST}}$	192	Low	I/O
TC0–TC1	224, 223	High	Output
TCK	201	—	Input
TDI	199	High	Input
TDO	198	High	Output
$\overline{\text{TEA}}$	154	Low	Input
$\overline{\text{TLBISYNC}}$	233	Low	Input
TMS	200	High	Input
$\overline{\text{TRST}}$	202	Low	Input
TSIZ0–TSIZ2	197, 196, 195	High	I/O

Table 9. PowerPC 603 Microprocessor Pinout Listing (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{TS}$	149	Low	I/O
TT0–TT4	191, 190, 185, 184, 180	High	I/O
VDD	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	High	Input
$\overline{WT}$	236	Low	Output
$\overline{XATS}$	150	Low	I/O

Notes:
1. These are test signals for factory use only and must be pulled up to VDD for normal machine operation.
2. OVDD inputs supply power to the I/O drivers and VDD inputs supply power to the processor core. Future members of the 603 family may use different OVDD and VDD input levels; for example, OVDD = 3.3 V or 5.0 V, with VDD = 2.5 V.

1.6 Package Description

The following sections provide the package parameters and the mechanical dimensions for the 603. Note that the 603 is currently offered in two types of CQFP packages—the Motorola wire-bond CQFP and the IBM C4-CQFP.

1.6.1 Motorola Wire-Bond CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola wire-bond CQFP package.

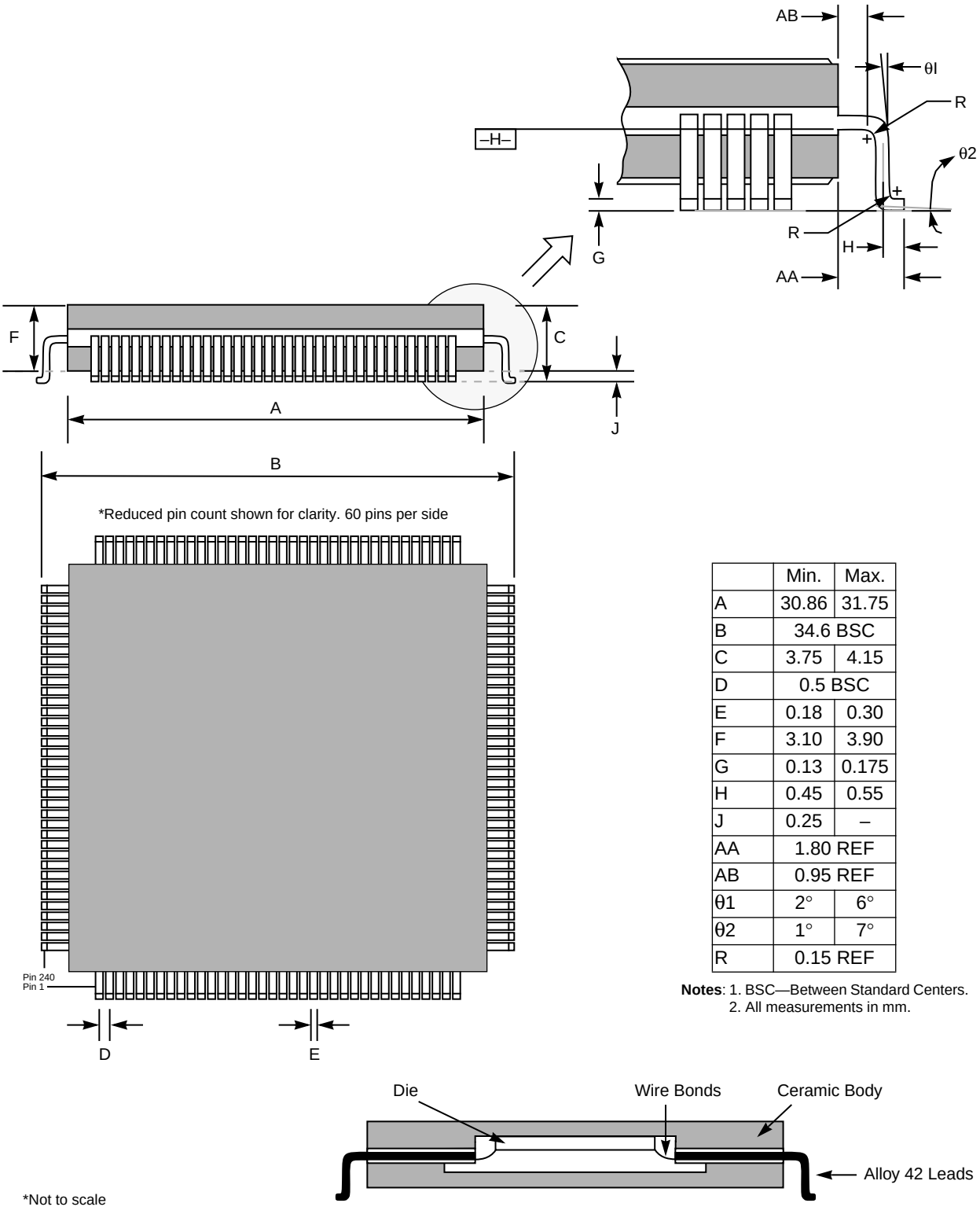
1.6.1.1 Package Parameters

The package parameters are as provided in the following list. The package type is 32 mm x 32 mm, 240-pin ceramic quad flat pack.

Package outline	32 mm x 32 mm
Interconnects	240
Pitch	0.5 mm

1.6.1.2 Mechanical Dimensions of the Motorola Wire-Bond CQFP Package

Figure 10 shows the mechanical dimensions for the wire-bond CQFP package.



	Min.	Max.
A	30.86	31.75
B	34.6 BSC	
C	3.75	4.15
D	0.5 BSC	
E	0.18	0.30
F	3.10	3.90
G	0.13	0.175
H	0.45	0.55
J	0.25	–
AA	1.80 REF	
AB	0.95 REF	
θ1	2°	6°
θ2	1°	7°
R	0.15 REF	

Notes: 1. BSC—Between Standard Centers.
2. All measurements in mm.

Figure 10. Mechanical Dimensions of the Motorola Wire-Bond CQFP Package

1.6.2 IBM C4-CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the IBM C4-CQFP package.

1.6.2.1 Package Parameters

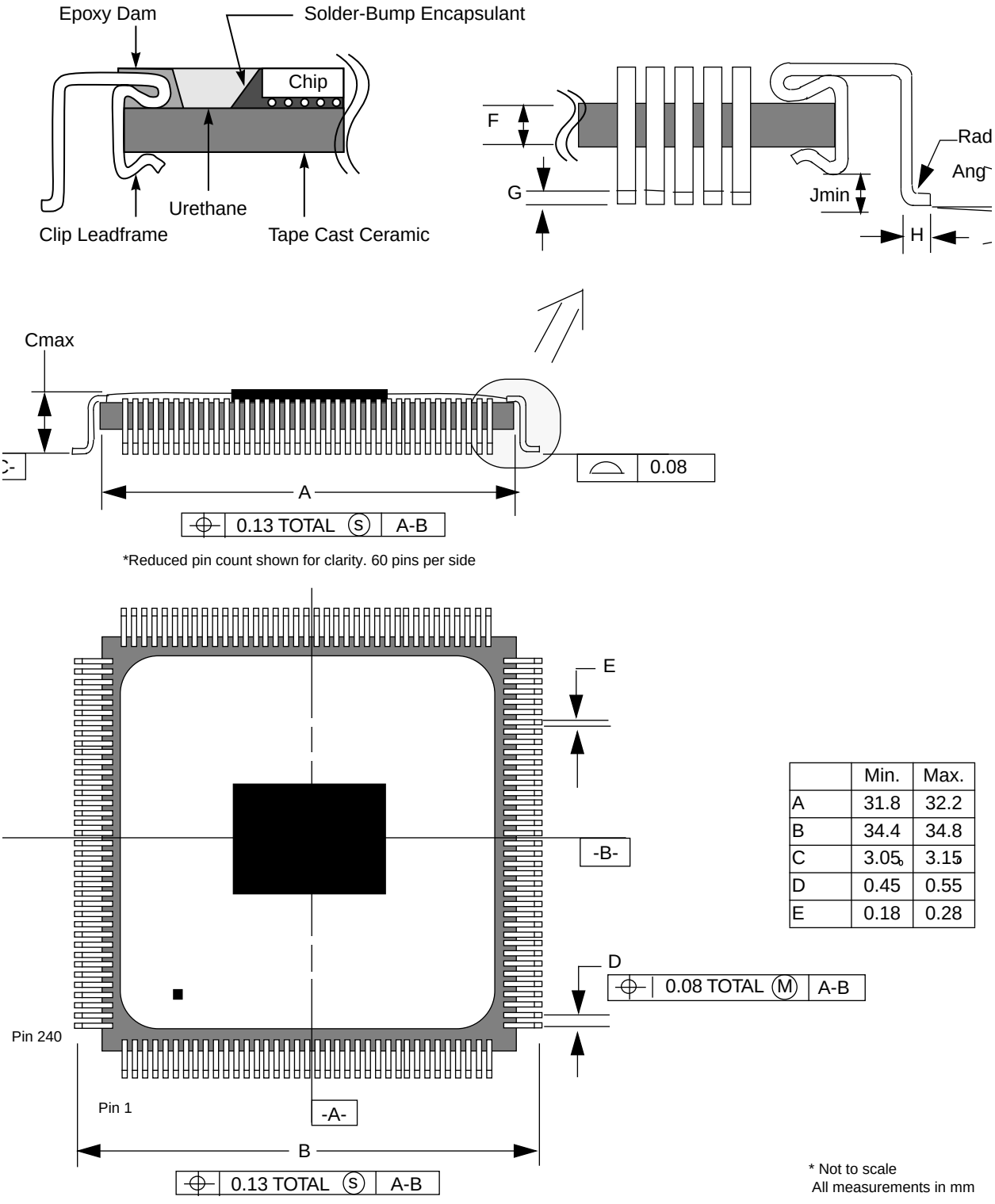
The package parameters are as provided in the following list. The package type is 32 mm x 32 mm, 240-pin ceramic quad flat pack.

Package outline	32 mm x 32 mm
Interconnects	240
Pitch	0.5 mm
Lead plating	Ni Au
Solder joint	Sn/PB (10/90)
Lead encapsulation	Epoxy
Solder-bump encapsulation	Epoxy
Maximum module height	3.1 mm
Co-planarity specification	0.08 mm

Note: No solvent can be used with the C4-CQFP package. See Appendix A, “General Handling Recommendations for the IBM Package,” for details.

1.6.2.2 Mechanical Dimensions of the IBM C4-CQFP Package

Figure 11 shows the mechanical dimensions for the C4-CQFP package.



	Min.	Max.
A	31.8	32.2
B	34.4	34.8
C	3.05	3.15
D	0.45	0.55
E	0.18	0.28

Figure 11. Mechanical Dimensions of the IBM C4-CQFP Package

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the 603.

1.7.1 PLL Configuration

A 603 part number corresponds to a particular combination of internal (CPU core) and SYSCLK (external bus) frequency ranges which the device has been tested to. The PLL is configured by the PLL_CFG0–PLL_CFG3 pins. For a given SYSCLK (bus) frequency, the PLL configuration pins set the internal CPU frequency of operation.

Table 10. PLL Configuration

PLL_CFG 0–3	Bus, CPU, and PLL Frequencies							
	CPU/ SYSCLK Ratio	Bus 16.6 MHz	Bus 20 MHz	Bus 25 MHz	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 66.6 MHz
00 00	1:1	—	—	—	—	—	—	66.6 (133)
0001	1:1	—	—	—	33.3 (133)	40 (160)	50 (200)	—
0010	1:1	16.6 (133)	20 (160)	25 (200)	—	—	—	—
0100	2:1	—	—	—	66.6 (133)	80 (160)	100 (200)	—
0101	2:1	33.3 (133)	40 (160)	50 (200)	—	—	—	—
1000	3:1	—	—	75 (150)	100 (200)	—	—	—
1001	3:1	50 (200)	—	—	—	—	—	—
1100	4:1	66.6 (133)	80 (160)	100 (200)	—	—	—	—
1101	4:1	—	—	—	—	—	—	—
0011	PLL bypass							
1111	Clock off							

Notes: 1. Some PLL configurations may select bus, CPU, or PLL frequencies which are not useful, not supported, or not tested for by the 603. PLL frequencies (shown in parenthesis in Table 10) should not fall below 133 MHz, and should not exceed 200 MHz.

2. In PLL bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. Note that the AC timing specifications given in this document do not apply in PLL bypass mode.
3. In clock-off mode, no clocking occurs inside the 603 regardless of the SYSCLK input.
4. PLL_CFG0–PLL_CFG1 signals select the CPU-to-bus ratio (1:1, 2:1, 3:1, 4:1), PLL_CFG2–PLL_CFG3 signals select the CPU-to-PLL multiplier (x2, x4, x8).

1.7.2 PLL Power Supply Filtering

The AVdd power signal is provided on the 603 to provide power to the clock generation phase-lock loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 12. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible.

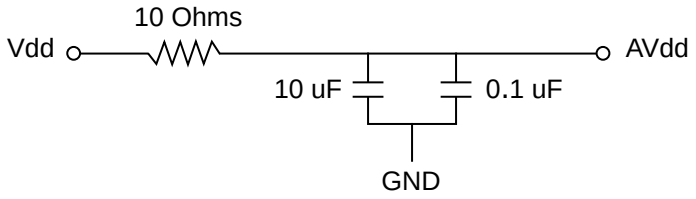


Figure 12. PLL Power Supply Filter Circuit

1.7.3 Decoupling Recommendations

Due to the 603's dynamic power management feature, large address and data buses, and high operating frequencies, the 603 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the 603 system, and the 603 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place a decoupling capacitor with a low ESR (effective series resistance) rating at each Vdd and OVdd pin of the 603.

These capacitors should range in value from 220 pF to 10 μF to provide both high and low frequency filtering, and should be placed as close as possible to their associated Vdd pin. Surface-mount tantulum or ceramic devices are preferred. It is also recommended that these decoupling capacitors receive their power from Vdd and GND power planes in the PCB, utilizing short traces to minimize inductance in the traces. Power and ground connections must be made to all external Vdd and GND pins of the 603.

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active-low inputs should be connected to Vdd. Unused active-high inputs should be connected to GND.

1.7.5 Thermal Management Information for the Motorola Package

This section provides a thermal management example for the 603; this example is based on a typical desktop configuration using a 240 lead, 32 mm x 32 mm, Motorola wire-bond CQFP package. The heat sink used for this data is a pinfin configuration from Thermalloy, part number 2338.

1.7.5.1 Thermal Characteristics for the Motorola Wire-Bond CQFP Package

The thermal characteristics for a wire-bond CQFP package are as follows:

Thermal resistance (junction-to-case) $= R_{\theta jc}$ or θ_{jc} = 2.2 °C/Watt (junction-to-case)

1.7.5.2 Thermal Management Example

The following example is based on a typical desktop configuration using a Motorola wire-bond CQFP package. The heat sink used for this data is a pinfin heat sink #2338 attached to the wire-bond CQFP package with thermal grease.

Figure 13 provides a thermal management example for the Motorola wire-bond CQFP package.

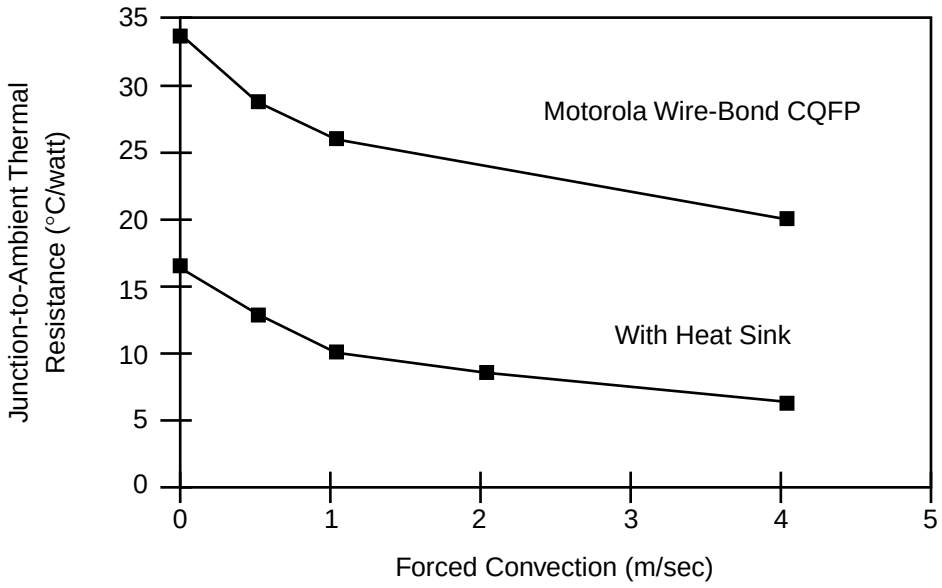


Figure 13. Motorola Wire-Bond CQFP Thermal Management Example

The junction temperature can be calculated from the junction-to-ambient thermal resistance, as follows:

Junction temperature: $T_j = T_a + R_{\theta ja} * P$

or

$T_j = T_a + (R_{\theta jc} + R_{cs} + R_{sa}) * P$

Where:

Ta is the ambient temperature in the vicinity of the device
$R_{\theta ja}$ is the junction-to-ambient thermal resistance
$R_{\theta jc}$ is the junction-to-case thermal resistance of the device
R_{cs} is the case-to-heat sink thermal resistance of the interface material
R_{sa} is the heat sink-to-ambient thermal resistance
P is the power dissipated by the device

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the case, from the case to the heat sink, and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

For a power dissipation of 2.5 Watts in an ambient temperature of 40 °C at 1 m/sec with the heat sink measured above, the junction temperature of the device would be as follows:

$T_j = T_a + R_{\theta ja} * P$

T_j = 40 °C + (10 °C/Watt * 2.5 Watts) = 65 °C

which is well within the reliability limits of the device.

Notes: 1. Junction-to-ambient thermal resistance is based on measurements on single-sided printed circuit boards per SEMI (Semiconductor Equipment and Materials International) G38-87 in natural convection.

2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

The vendors who supply heat sinks are Aavid Engineering, IERC, Thermalloy, and Wakefield Engineering. Any of these vendors can supply heat sinks with sufficient thermal performance.

1.7.6 Thermal Management Information for the IBM Package

This section provides a thermal management example for the 603; this example is based on a typical desktop configuration using a 240-lead, 32 mm x 32 mm, IBM C4-CQFP package. The heat sink used for this data is a pinfin configuration from Thermalloy, part number 2338, and a flat aluminum plate with dimensions of 24 mm x 24 mm and 1.5 mm thickness.

1.7.6.1 Thermal Characteristics for the IBM C4-CQFP Package

The thermal characteristics for a C4-CQFP package are as follows:

Thermal resistance (junction to heat sink) = $R_{\theta js}$ or θ_{js} = 1.1°C/Watt (junction to heat sink)

1.7.6.2 Thermal Management Example

The following example is based on a typical desktop configuration using an IBM C4-CQFP package. The heat sink used for this data is a pinfin heat sink #2338 attached to the C4-CQFP package with 2-stage epoxy.

The junction temperature can be calculated from the junction to ambient thermal resistance, as follows:

$$\text{Junction temperature} = T_j = T_a + R_{\theta ja} * P$$

or

$$T_j = T_a + (R_{\theta js} + R_{sa}) * P$$

Where:

T_a is the ambient temperature in the vicinity of the device
$R_{\theta ja}$ is the junction-to-ambient thermal resistance
$R_{\theta js}$ is the junction-to-heat sink thermal resistance
R_{sa} is the heat sink-to-ambient thermal resistance
P is the power dissipated by the device

Note: $R_{\theta js}$ includes the resistance of a typical layer of thermal compound. If a lower conductivity material is used, its thermal resistance must be included.

In this environment, it can be assumed that all the heat is dissipated to the ambient through the heat sink, so the junction-to-ambient thermal resistance is the sum of the resistances from the junction to the heat sink and from the heat sink to the ambient.

Note that verification of external thermal resistance and case temperature should be performed for each application. Thermal resistance can vary considerably due to many factors including degree of air turbulence.

Figure 14 provides a thermal management example for the IBM C4-CQFP package.

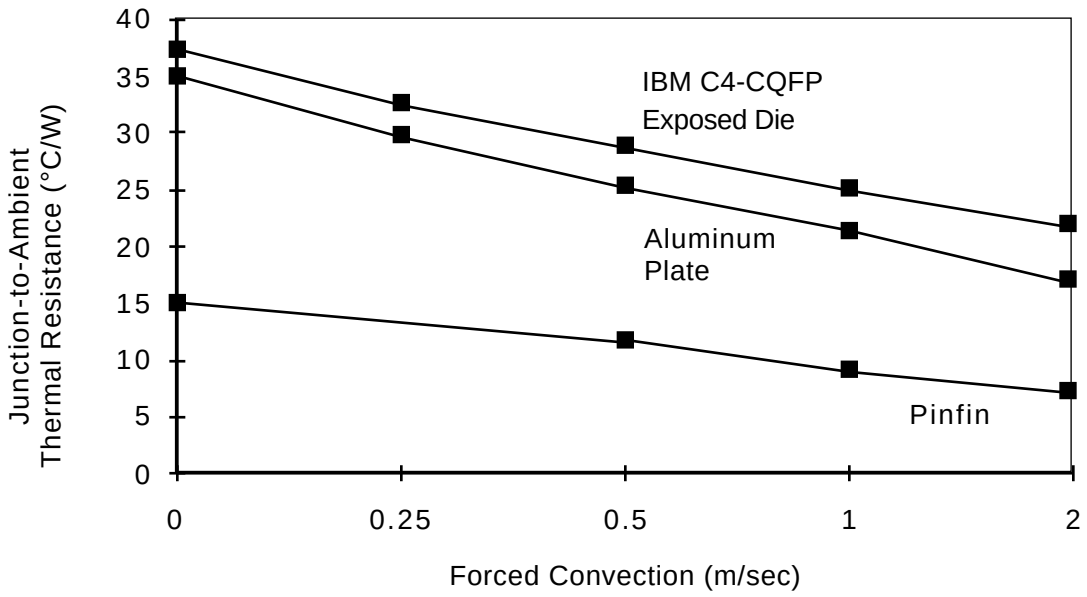


Figure 14. IBM C4-CQFP Thermal Management Example

For a power dissipation of 2.5 Watts in an ambient temperature of 40 °C at 1 m/sec with the pinfin heat sink measured above, the junction temperature of the device would be as follows:

$T_j = T_a + R_{\theta ja} * P$

$T_j = 40\ °C + (9.1\ °C/Watt * 2.5\ Watts) = 63\ °C$

which is well within the reliability limits of the device.

Notes: 1. Junction-to-ambient thermal resistance is based on modeling.

2. Junction-to-heat sink thermal resistance is based on measurements and model using thermal test chip and thermal couple which is placed on the base of the heat sink.
3. θ_{ja} is not measured for 0.25 m/sec convection for the pinfin.

The vendors who supply heat sinks are Aavid Engineering, Thermalloy, and Wakefield Engineering. Any of these vendors can supply heat sinks with sufficient thermal performance.

1.8 Ordering Information

This section provides the ordering information for the 603. Note that the individual part numbers correspond to a specific combination of 603 internal/bus frequencies, which must be observed to ensure proper operation of the device. For other frequency combinations, temperature ranges, power-supply tolerances package types, etc., contact your local Motorola or IBM sales office.

Table 11. Ordering Information for the PowerPC 603 Microprocessor

Package Type		Internal Frequency	Bus Frequency	Required PLL_CFG [0–3] Setting	Part Numbers	
Motorola	IBM				Motorola	IBM
Wire-bond CQFP	C4-CQFP	80 MHz	40 MHz	0100	MPC603AFE80CX	PPC603-FX-080-2
		66.67 MHz	33.33 MHz	0100	MPC603AFE66CX	PPC603-FX-066-2
			66.67 MHz	0000	MPC603AFE66AX	PPC603-FX-066-1

1.8.1 Motorola Part Number Key

Figure 15 provides a detailed description of the Motorola part number for the 603.

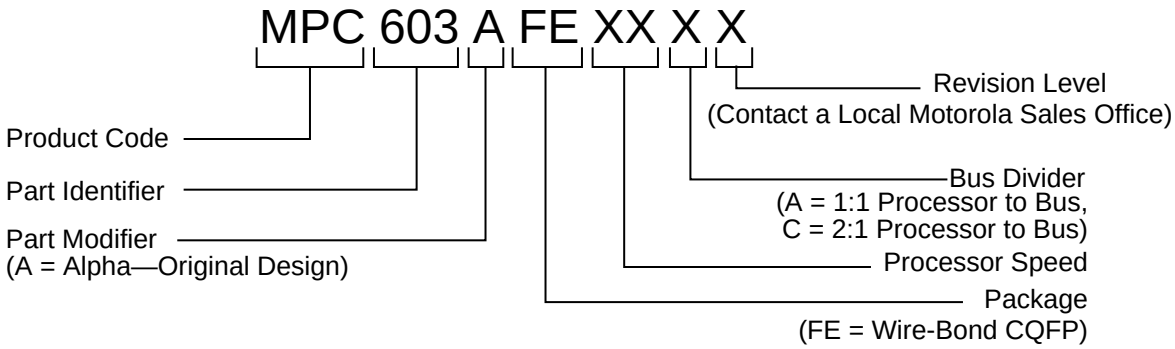


Figure 15. Motorola Part Number Key

1.8.2 IBM Part Number Key

Figure 16 provides a detailed description of the IBM part number for the 603.

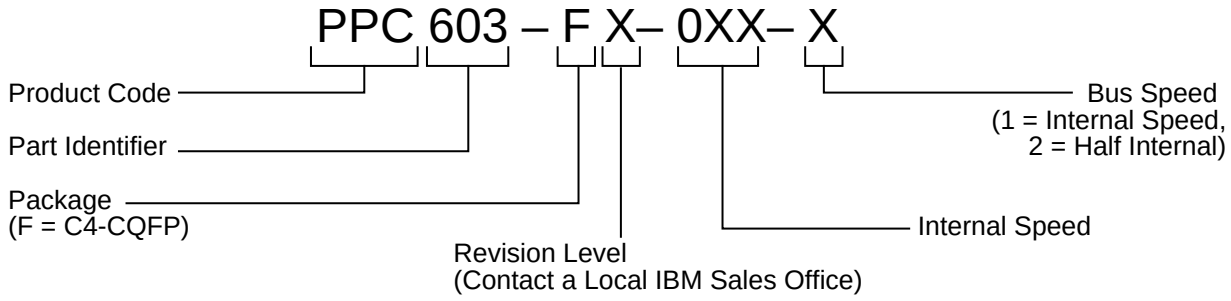


Figure 16. IBM Part Number Key

Appendix A
General Handling Recommendations for the IBM Package

The following list provides a few guidelines for package handling:

- Handle the electrostatic discharge sensitive (ESD) package with care before, during, and after processing.
- Do not apply any load to exceed 3 Kg after assembly.
- Components should not be hot dip tinned
- The package encapsulation is an acrylated urethane. Use adequate ventilation (local exhaust) for all elevated temperature processes.

The package parameters are as follows:

Heat sink adhesive	AIEG-7655
IBM reference drawing	99F4869
Test socket	Yamaichi QFP-PO 0.5-240P
Signal	165
Power/ground	75
Total	240

A.1 Package Environmental, Operation, Shipment, and Storage Requirements

The environmental, operation, shipment, and storage requirements are as follows:

- Make sure that the package is suitable for continuous operation under business office environments.
  - — Operating environment: 10 °C to 40 °C, 8% to 80% relative humidity
  - — Storage environment: 1 °C to 60 °C, to 80% relative humidity
  - — Shipping environment: 40 °C to 60 °C, 5% to 100% relative humidity
- This component is qualified to meet JEDEC moisture Class 2 of bag
  - — After expiration of shelf life, packages may be baked at 120 °C (+10/–5 °C) for 4 hours minimum and packaged. Shelf life is as specified above.

A.2 Card Assembly Recommendations

This section provides recommendations for card assembly process. Follow these guidelines for card assembly.

- This component is supported for aqueous, IR, convection reflow, and vapor phase card assembly processes.
- The temperature of packages should not exceed 220 °C for longer than 5 minutes.
- The package entering a cleaning cycle must not be exposed to temperature greater than that occurring during solder reflow or hot air exposure.
- It is not recommended to re-attach a package that is removed after card assembly.

A.2.1 Card Assembly Process

During the card assembly process, no solvent can be used with the C4FP, and no more than 3 Kg of force must be applied normal to the top of the package prior to, during, or after card assembly. Other details of the card assembly process follow:

Solder paste	Either water soluble (for example, Alpha 1208) or no clean
Solder stencil thickness	0.152 mm
Solder stencil aperature	Width reduced to 0.03 mm from the board pad width
Placement tool	Panasonic MPA3 or equivalent
Solder reflow	Infrared, convection, or vapor phase
Solder reflow profile	Infrared and/or convection •Average ramp-up—0.48 to 1.8 °C/second •Time above 183 °C—45 to 145 seconds •Minimum lead temperature—200 °C •Maximum lead temperature—240 °C •Maximum C4FP temperature—245 °C Vapor phase •Preheat (board)—60 °C to 150 °C •Time above 183 °C—60 to 145 seconds •Minimum lead temperature—200 °C •Maximum C4FP temperature—220 °C •Egress temperature—below 150 °C

Clean after reflow	De-ionized (D.I.) water if water-soluble paste is used •Cleaner requirements—conveyorized, in-line •Minimum of four washing chambers —Pre-clean chamber: top and bottom sprays, minimum top-side pressure of 25 psig, water temperature of 70 °C minimum, dwell time of 24 seconds minimum, water is not re-used, water flow rate of 30 liters/minute. —Wash chamber #1: top and bottom sprays, minimum top-side pressure of 48 psig, minimum bottom-side pressure of 44 psig, water temperature of 62.5 °C (±2.5 °C), dwell time of 48 seconds minimum, water flow rate of 350 liters/minute. —Wash chamber #2: top and bottom sprays, minimum top-side pressure of 32 psig, minimum bottom-side pressure of 28 psig, water temperature of 72.5 °C (±2.5 °C), dwell time of 48 seconds minimum, water flow rate of 325 liters/minute. —Final rinse chamber: top and bottom sprays, minimum top-side pressure of 25 psig, water temperature of 72.5 °C minimum, dwell time of 24 seconds minimum, water flow rate of 30 liters/minute. •No cleaning required if “no clean solder paste” is used
Touch-up and repair	Water soluble (for example, Kester 450) or No Clean Flux
C4FP removal	Hot air rework
C4FP replace	Hand solder

Motorola Literature Distribution Centers:
USA: Motorola Literature Distribution, P.O. Box 20912, Phoenix, Arizona 85036; FAX (602) 994-6430
JAPAN: Nippon Motorola Ltd., 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd., Silicon Harbour Centre, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
Technical Information: Motorola Inc. Semiconductor Products Sector Technical Responsiveness Center; (800) 521-6274.
Document Comments: FAX (512) 891-2638, Attn: RISC Applications Engineering.

IBM Microelectronics Division:
USA: IBM Microelectronics Division, Mail Stop A25/862-1, PowerPC Marketing, 1000 River Street, Essex Junction, VT 05452-4299; Tel.: (800) PowerPC [(800) 769-3772]; FAX (800) POWERfax [(800) 769-3732].
EUROPE: IBM Microelectronics Division, PowerPC Marketing, Dept. 1045, 224 Boulevard J.F. Kennedy, 91105 Corbeil-Essonnes CEDEX, France; Tel. (33) 1-60-88 5167; FAX (33) 1-60-88 4920.
JAPAN: IBM Microelectronics Division, PowerPC Marketing, Dept., R0260, 800 Ichimiyake, Yasu-cho, Yasu-gun, Shinga-ken, Japan 520-23; Tel. (81) 775-87-4745; FAX (81) 775-87-4735.

IBM

MOTOROLA