Intel® 41210 Serial to Parallel PCI Bridge

Design Guide

May 2005

Order Number: 278801-004

Contents

Figures

Tables

Revision History

Date	Revision	Description
May 2005	004	Removed Section 5.3, VCCPE and REFCLKn/REFCLKp Information Added signals to Section 8.3.1 Updated Table 19, Table 20, and Table 21
October 2004	003	Updated PCI Express operation information in Section 2.1 and Table 19. Added signal NC17 information in Table 21.
July 2004	002	Updated Chapters 4, 5, and 12
October 2003	001	Updated content; second draft of this document; initial public release of this document.
July 2003	000	First internal draft of this document.

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About This Document 1

This document provides layout information and guidelines for designing platform or add-in board applications with the Intel® 41210 Serial to Parallel PCI Bridge (also called the 41210 Bridge). It is recommended that this document be used as a guideline. Intel recommends employing best-known design practices with board level simulation, signal integrity testing and validation for a robust design.

Designers should note that this guide focuses upon specific design considerations for the 41210 Bridge and is not intended to be an all-inclusive list of all good design practices. Use this guide as a starting point and use empirical data to optimize your particular design.

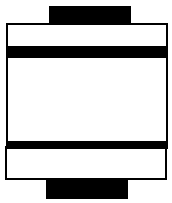
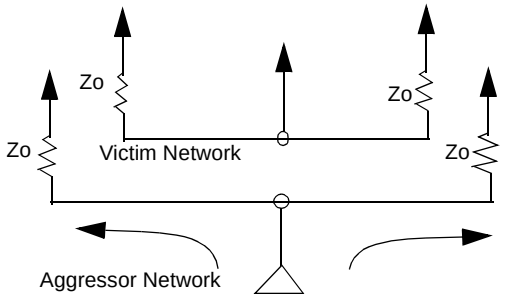
1.1 Terminology and Definitions

Table 1 provides a list of terms and definitions that may be useful when working with the 41210 Bridge product.

Table 1. Terminology and Definitions (Sheet 1 of 2)

Term	Definition	
Stripline		Stripline in a PCB is composed of the conductor inserted in a dielectric with GND planes to the top and bottom. **NOTE:** An easy way to distinguish stripline from microstrip is that you need to strip away layers of the board to view the trace on stripline.
Microstrip		Microstrip in a PCB is composed of the conductor on the top layer above the dielectric with a ground plane below
Prepreg	Material used for the lamination process of manufacturing PCBs. It consists of a layer of epoxy material that is placed between two cores. This layer melts into epoxy when heated and forms around adjacent traces.	
Core	Material used for the lamination process of manufacturing PCBs. This material is two sided laminate with copper on each side. The core is an internal layer that is etched.	

Table 1. Terminology and Definitions (Sheet 2 of 2)

Term	Definition	
PCB	 Example of a Four-Layer Stack	Printed circuit board. Example manufacturing process consists of the following steps: • Consists of alternating layers of core and prepreg stacked • The finished PCB is heated and cured. • The via holes are drilled • Plating covers holes and outer surfaces • Etching removes unwanted copper • Board is tinned, coated with solder mask and silk screened
SSTL_2	Series Stub Terminated Logic for 2.5 V	
JEDEC	Provides standards for the semiconductor industry.	
Aggressor	A network that transmits a coupled signal to another network is aggressor network. 	
Victim	A network that receives a coupled cross-talk signal from another network is a victim network.	
Network	The trace of a PCB that completes an electrical connection between two or more components.	
Stub	Branch from a trunk terminating at the pad of an agent.	
CRB	Customer Reference Board	
Downstream	Downstream refers either to the relative position of an interconnect/system element (Link/device) as something that is farther from the Root Complex, or to a direction of information flow, i.e., when information is flowing away from the Root Complex.	
Upstream		
Local memory	Memory subsystem on the Intel XScale® core DDR SDRAM or Peripheral Bus Interface busses.	
DWORD	32-bit data word.	
Flip Chip	FC-BGA (flip chip-ball grid array) chip packages are designed with processor core flipped up on the back of the chip, facing away from the PCB. This allows more efficient cooling of the package.	
Mode Conversion	Mode Conversions are due to imperfections on the interconnect which transform differential mode voltage to common mode voltage and common mode voltage to differential voltage.	
PCI-E	PCI-Express	

Introduction 2

The Intel®41210 Serial to Parallel PCI Bridge integrates two PCI Express-to-PCI bridges. Each bridge follows the PCI-to-PCI Bridge programming model. The PCI Express port is compliant to the *PCI Express Specification*, Revision 1.0. The two PCI bus interfaces are fully compliant to the *PCI Local Bus Specification*, Revision 2.3.

2.1 PCI Express Interface Features

- *PCI Express Specification*, Revision 1.0b compliant.
- Support for single x8, single x4 or single x1 PCI Express operation.
- 64-bit addressing support.
- 32-bit CRC (cyclic redundancy checking) covering all transmitted data packets.
- 16-bit CRC on all link message information.
- Raw bit-rate on the data pins of 2.5 Gbit/s, resulting in a raw bandwidth per pin of 250 MB/s.
- Maximum realized bandwidth on PCI Express interface is 2 GB/s (in x8 mode) in each direction simultaneously, for an aggregate of 4 GB/s.

2.2 PCI-X Interface Features

- *PCI Local Bus Specification*, Revision 2.3 compliant.
- *PCI-to-PCI Bridge Specification*, Revision 1.1 compliant.
- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a compliant.
- 64-bit 66 MHz, 3.3 V, NOT 5 V tolerant.
- On Die Termination (ODT) with 8.2KΩ pull-up to 3.3V for PCI signals.
- Six external REQ/GNT Pairs for internal arbiter on segment A and B respectively.
- Programmable bus parking on either the last agent or always on Lanai.
- 2-level programmable round-robin internal arbiter with Multi-Transaction Timer (MTT)
- External PCI clock-feed support for asynchronous primary and secondary domain operation.
- 64-bit addressing for upstream and downstream transactions
- Downstream LOCK# support.
- No upstream LOCK# support.
- PCI fast Back-to-Back capable as target.
- Up to four active and four pending upstream memory read transactions
- Up to two downstream delayed (memory read, I/O read/write and configuration read/write) transaction.

- Tunable inbound read prefetch algorithm for PCI MRM/MRL commands
- Local initialization via SMBus
- Secondary side initialization via Type 0 configuration cycles.

2.3 Power Management

- Support for PCI Express Active State Power Management (ASPM) L0s link state
- Support for PCI PM 1.1 compatible D0, D3hot and D3cold device power states
- Support for PME# event propagation on behalf of PCI devices

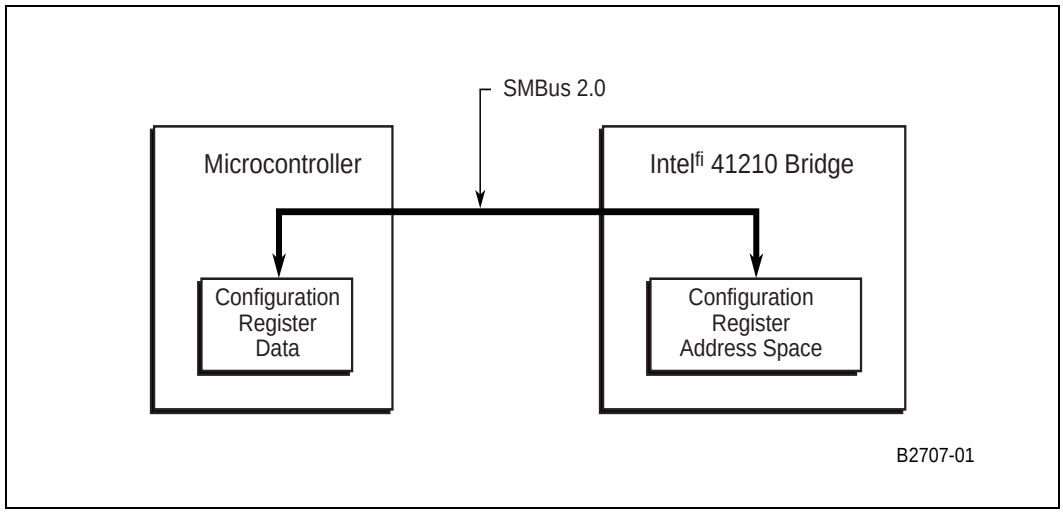
2.4 SMBus Interface

- Compatible with *System Management Bus Specification*, Revision 2.0
- Slave mode operation only.
- Full read/write access to all configuration registers

2.4.1 SMBus for configuration register initialization

- Support for local initialization of the configuration registers can be implemented using a microcontroller via SMB. Figure 1shows this SMBus and the data transfer that occurs between the 41210 Bridge and the microcontroller.
- Configuration Register information is stored internally in a microcontroller and the information is transferred to the product via System Managed Bus (SMBus) protocols when the device receives power or reset.
- The requirements of the microcontroller are as follows:
  - Supports I^2C and SMBus Protocols
  - Has at least 256 Byte of internal EEprom space
  - To facilitate this programming on the Customer Reference Board a Microchip part PIC16F876A was used.
  - Code space: estimated code size is ~2K words of program space and 32 words of RAM

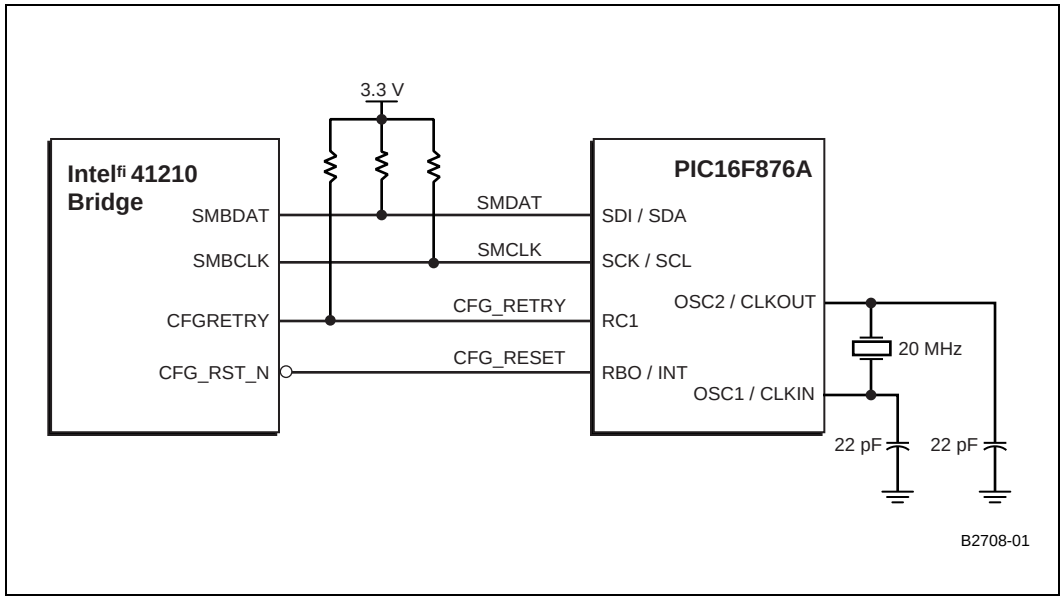
Figure 1. 41210 Bridge Microcontroller Block Diagram



2.4.2 Microcontroller Connections to the 41210 Bridge

The following diagram shows the SMB interface from the 41210 Bridge to the microcontroller.

Figure 2. 41210 Bridge Microcontroller Connections



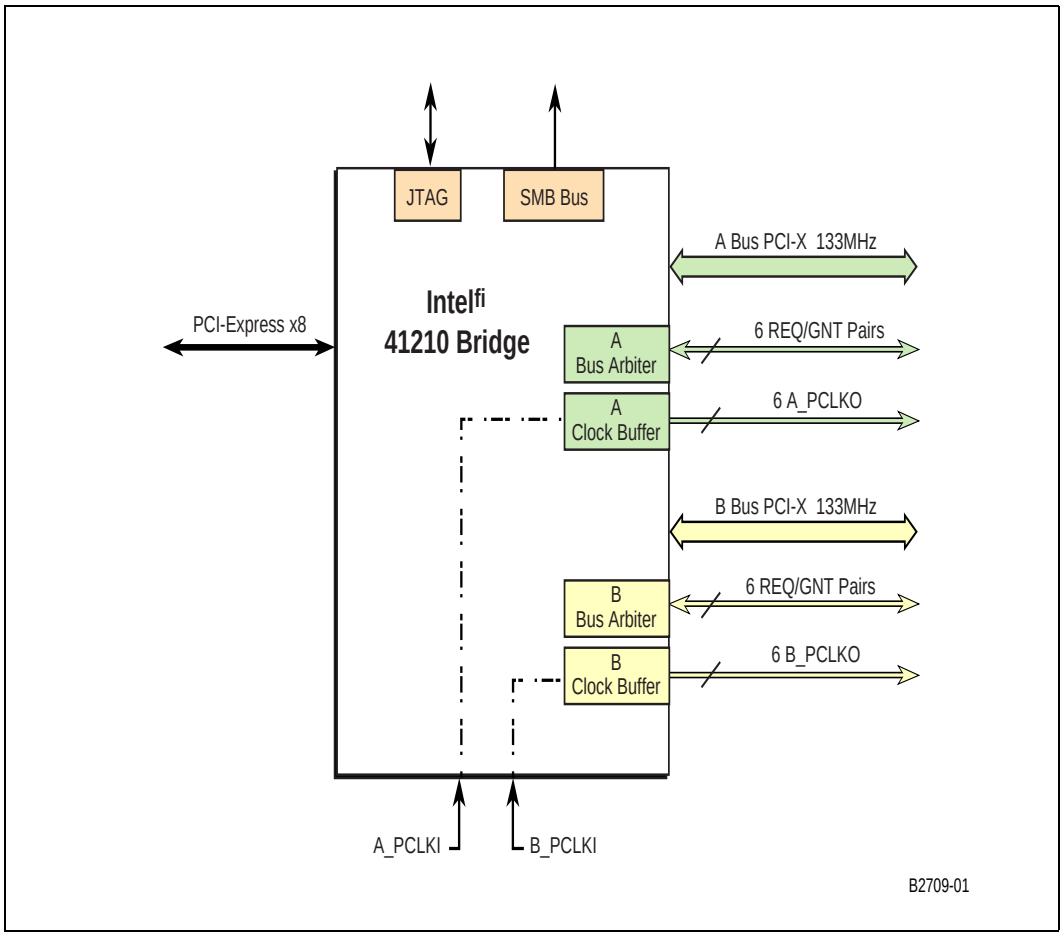
2.5 JTAG

- Compliant with *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1a*

2.6 Related Documents

- *Intel® 41210 Serial to Parallel PCI Bridge Design Specification (EDS)*, Revision 1.0.
- *PCI Express Specification*, Revision 1.0, from www.pci-sig.com.
- PCI Express Design Guide, Revision 0.5
- *PCI Local Bus Specification*, Revision 2.3, from www.pci-sig.com.
- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a, from www.pci-sig.com.
- *IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1a*
- *System Management Bus Specification*, Revision 2.0

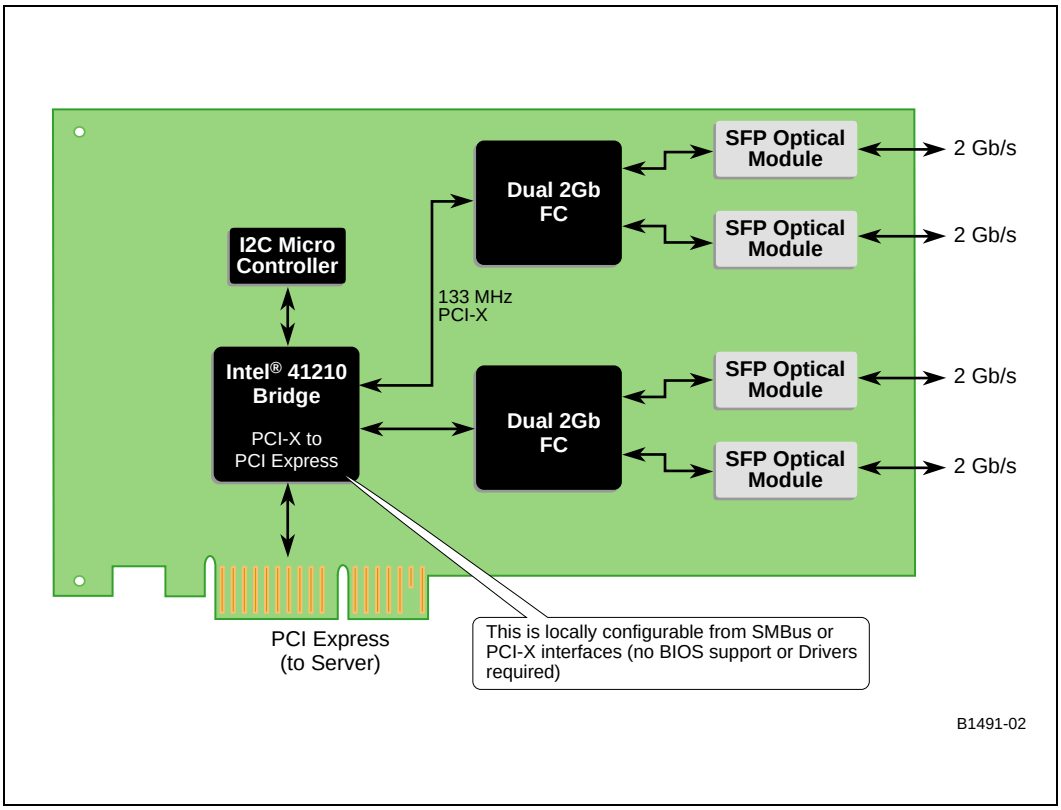
Figure 3. 41210 Bridge Block Diagram



2.7 Intel®41210 Serial to Parallel PCI Bridge Applications

This section provides a block diagram for a typical the 41210 Bridge application. This application shows a PCI-E adapter card with two Dual 2Gb Fibre Channel controllers. Each of the PCI-X bus segments is connected to the Dual 2Gb Fibre Channel chip running at 133MHz. The two Dual FC chips provides the four 2Gb/s outputs.

Figure 4. Intel® 41210 Bridge Adapter Card Block Diagram



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Package Information 3

3.1 Package Specification

The 41210 Bridge is in a 567-ball FCBGA package, 31mm X 31mm in size, with a 1.27mm ball pitch.

Figure 5. Top View - 41210 Bridge 567-Ball FCBGA Package Dimensions

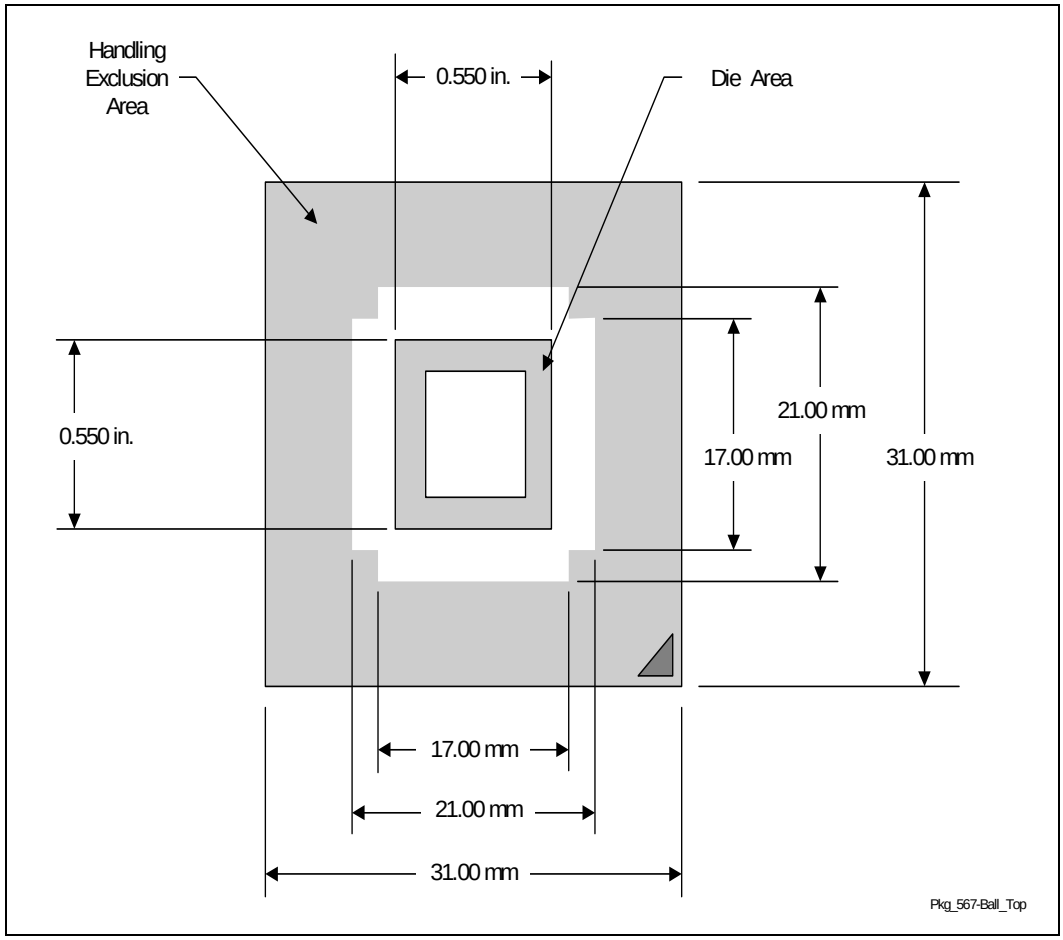


Figure 6. Bottom View - 41210 Bridge 567-Ball FCBGA Package Dimensions

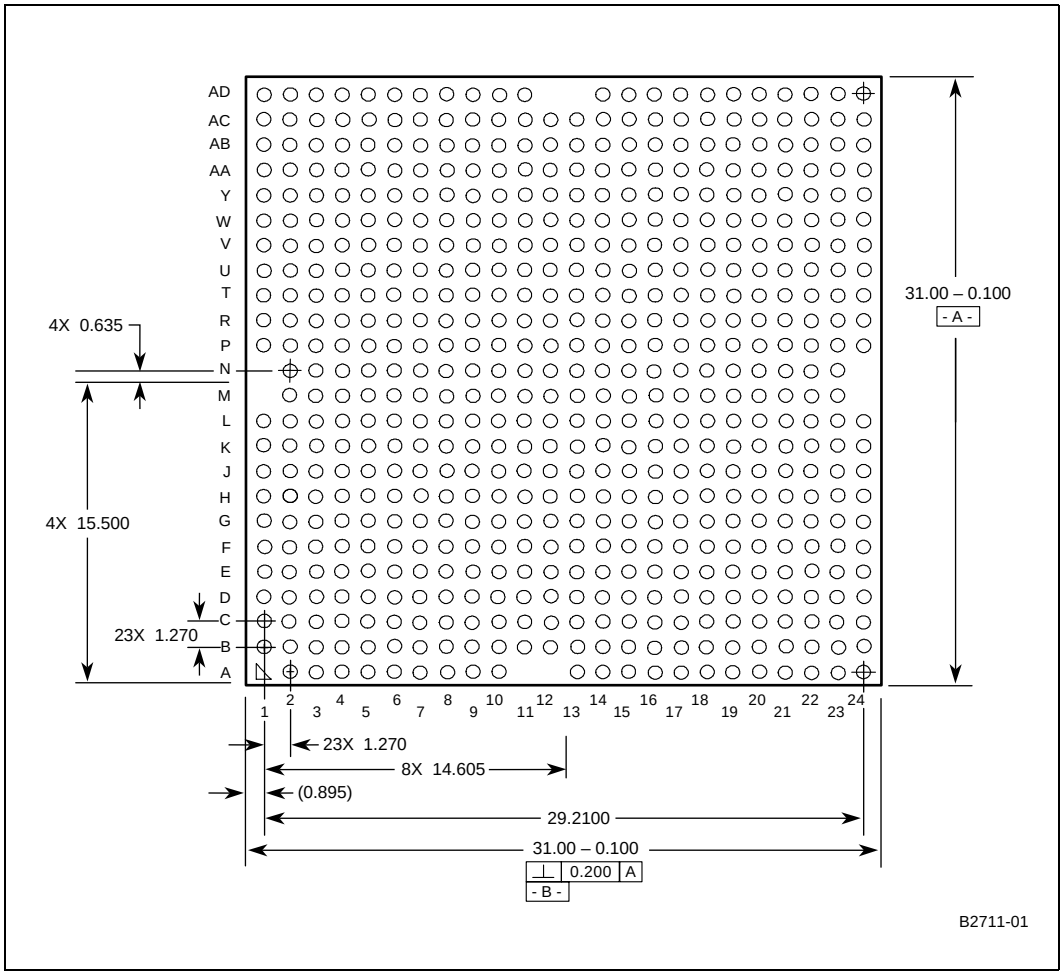
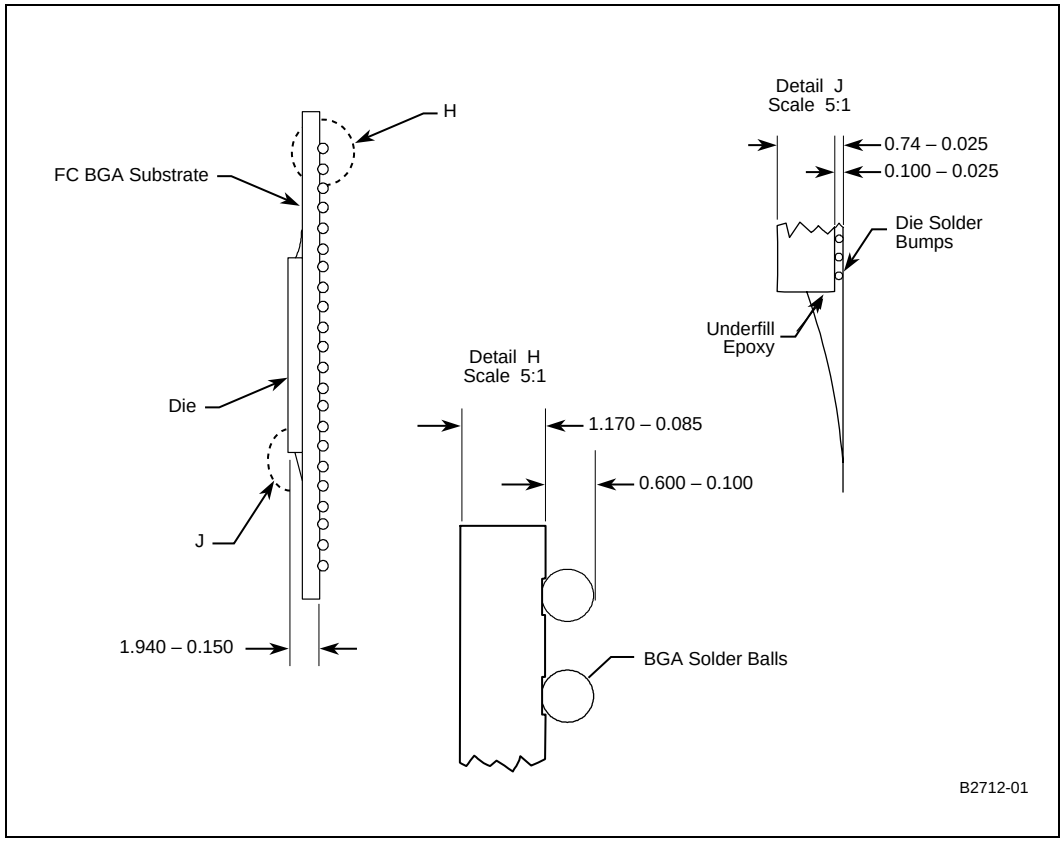


Figure 7. Side View - 41210 Bridge 567-Ball FCBGA Package Dimensions



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Power Plane Layout 4

This chapter provides details on the decoupling and voltage planes needed to bias the 41210 Bridge package.

4.1 41210 Bridge Decoupling Guidelines

Table 2 lists the decoupling guidelines for the 41210 Bridge. Figure 8 and Figure 9 provide the decoupling capacitors around the 41210 Bridge ball grid pins.

Figure 8. Decoupling Placement for Core and PCI Express Voltage Planes

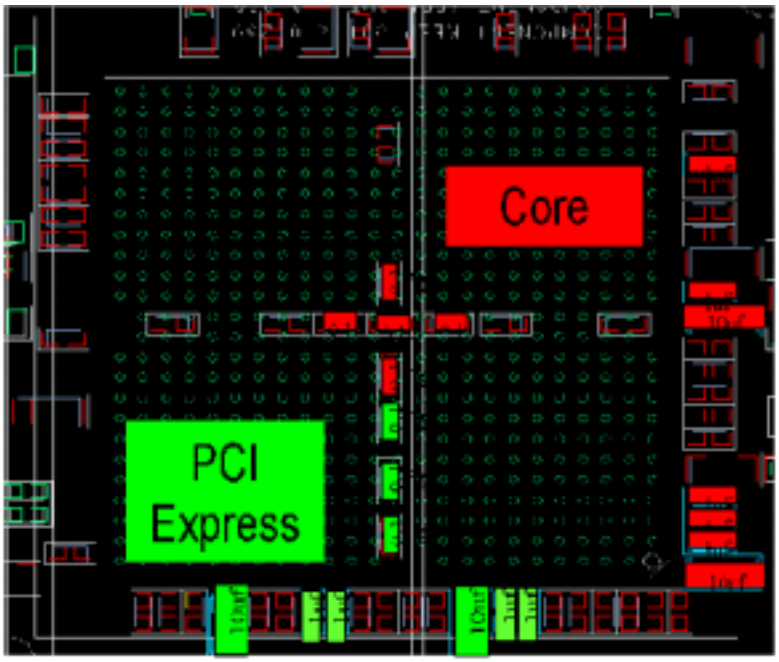


Figure 9. Decoupling Placement for PCI/PCI-X 1.5V and 3.3V Voltage Planes

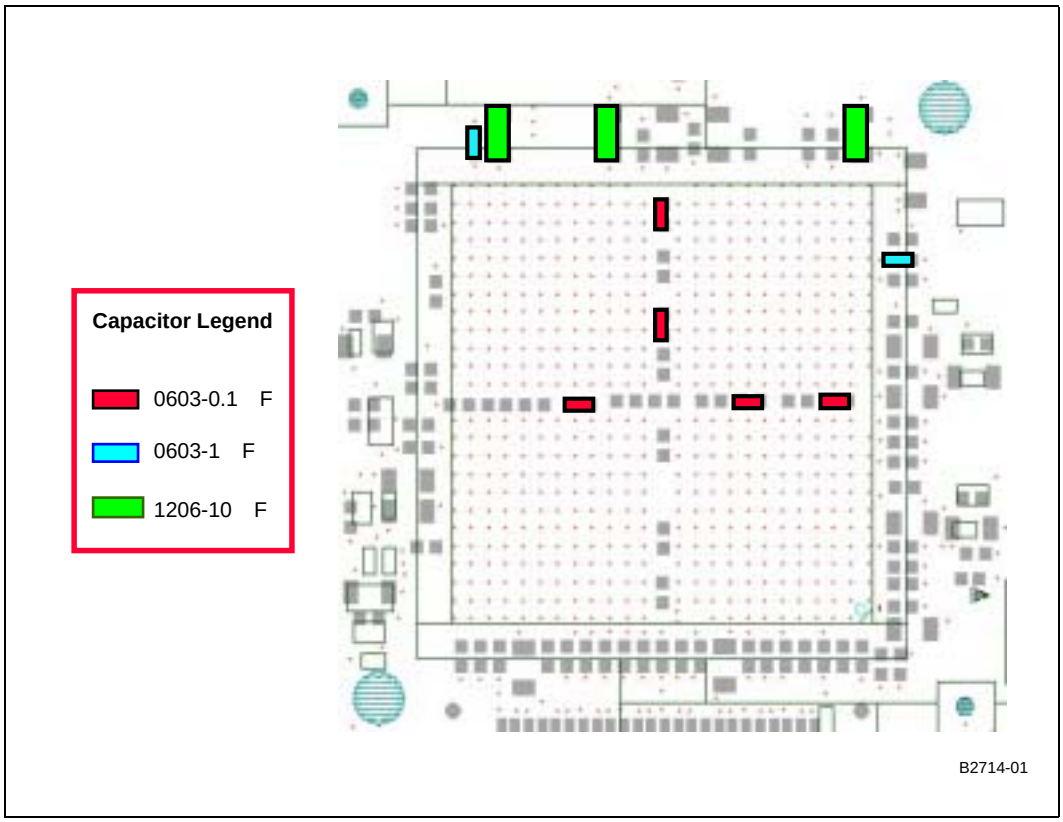


Table 2. 41210 Bridge Decoupling Guidelines

Voltage Plane	Voltage	41210 Pins	C (uF)	Package	ESR (mΩ)	ESL (nH)	# of Caps	Location
PCI/PCI-X Voltage	3.3V	VCC33	0.1	0603	50-300	1.0-3.0	5	Beneath 41210 Bridge BGA
PCI/PCI-X Voltage	3.3V	VCC33	1.0	0603	50-300	1.0-3.0	2	As close as design rules will allow to 41210 Bridge BGA
PCI/PCI-X Voltage	3.3V	VCC33	10	1206	50-300	1.0-3.0	3	As close as design rules will allow to 41210 Bridge BGA
Core Voltage	1.5V	VCC15	0.1	0603	200	2.0	5	Beneath 41210 Bridge BGA
Core Voltage	1.5V	VCC15	1.0	0805	200	2.3	5	As close as design rules will allow to 41210 Bridge BGA
Core Voltage	1.5V	VCC15	10	1206	200	1.9	2	As close as design rules will allow to 41210 Bridge BGA
PCI Express Voltage	1.5V	VCCPE	0.1	0603	200	2.0	3	Beneath 41210 Bridge BGA
PCI Express Voltage	1.5V	VCCPE	1	0805	200	2.3	4	As close as design rules will allow to 41210 Bridge BGA
PCI Express Voltage	1.5V	VCCPE	10	1206	200	1.9	2	As close as design rules will allow to 41210 Bridge BGA

4.2 Split Voltage Planes

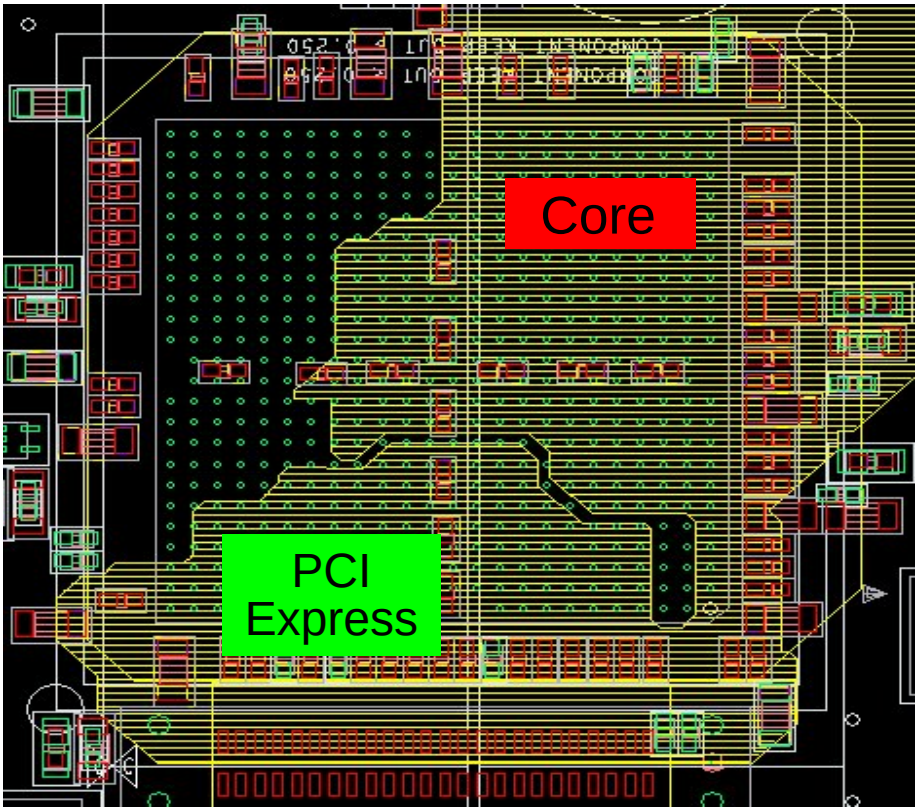
There are two 1.5V voltage planes that supply power to the 41210 Bridge:

- VCC15:1.5V ±5% (1.5V core voltage)
- VCCPE:1.5V ±3% (1.5V PCI Express voltage)

The 41210 Bridge core (VCC15), PCI-Express (VCCPE) voltages should be supplied by two separate voltage regulators or a single regulator. If VCC15 and VCCPE is supplied by a single voltage regulator the power planes should be split as shown in Figure 10.

Note: Linear voltage regulators are recommended when using 1.5 Volt power supplies.

Figure 10. 41210 Bridge Single-Layer Split Voltage Plane



41210 Bridge Reset and Power Timing Considerations 5

This chapter describes the 41210 Bridge reset timing considerations.

5.1 A_RST#,B_RST# and PERST# Timing Requirements

The PCI-X Specification requires that there is a 100ms delay from valid power (**PERST#**) to reset deassertion (**A_RST#/B_RST#**). 41210 Bridge will keep A_RST#/B_RST# asserted for a minimum of 320ms after PERST# is deasserted.

5.2 VCC15 and VCC33 Voltage Requirements

The following steps are the power sequencing requirements that must be followed with the 41210 Bridge:

1. The 41210 Bridge requires that the VCC33 voltage rail be no less than 0.5V below VCC15 (absolute voltage value) at all times during 41210 operation, including during system power up and power down. In other words, the following must always be true:

   VCC33 >= (VCC15 – 0.5V)

   This can be accomplished by placing a diode (with a voltage drop <0.5V) between VCC15 and VCC33. A node will be connected to VCC15 and cathode will be connected to VCC33.

   If VCC15 (1.5V PCI-X I/O voltage) and VCC15 (1.5V core voltage) are tied together on the platform, then both voltages must meet the above rule.

Note: Linear voltage regulators are recommended when using 1.5 Volt power supplies.

2. If a voltage regulator solution is used which shunts VCC15 to ground while VCC33 is powered, the maximum allowable time that VCC15 can be shunted to ground while VCC33 is fully powered is 20ms.
3. The maximum allowed time between VCC33 and VCC15 ramping is 525ms.

Note: There is no minimum sequencing time requirement other than requirements in Steps 2 and 3.

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General Routing Guidelines 6

This chapter provides some basic routing guidelines for layout and design of a printed circuit board using the 41210 Bridge. The high-speed clocking required when designing with the 41210 Bridge requires special attention to signal integrity. In fact, it is highly recommended that the board design be simulated to determine optimum layout for signal integrity. The information in this chapter provides guidelines to aid the designer with board layout. Several factors influence the signal integrity of a 41210 Bridge design. These factors include:

- power distribution
- minimizing crosstalk
- decoupling
- layout considerations when routing the PCI Express bus and PCI-X bus interfaces

6.1 General Routing Guidelines

This section details general routing guidelines for designing with the 41210 Bridge. The order in which signals are routed varies from designer to designer. Some designers prefer to route all clock signals first, while others prefer to route all high-speed bus signals first. Either order can be used, provided the guidelines listed here are followed.

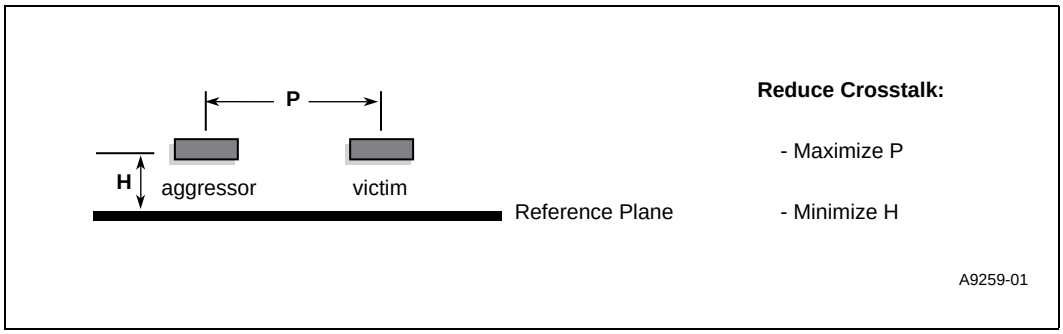
6.2 Crosstalk

Crosstalk is caused by capacitive and inductive coupling between signals. Crosstalk is composed of both backward and forward crosstalk components. Backward crosstalk creates an induced signal on victim network that propagates in the opposite direction of the aggressor signal. Forward crosstalk creates a signal that propagates in the same direction as the aggressor signal.

Circuit board analysis software is used to analyze your board layout for crosstalk problems. Examples of 2D analysis tools include Parasitic Parameters from **ANSOFT*** and XFS from **Quad Design***. Crosstalk problems occur when circuit etch lines run in parallel. When board analysis software is not available, the layout should be designed to maintain at least the minimum recommended spacing for bus interfaces.

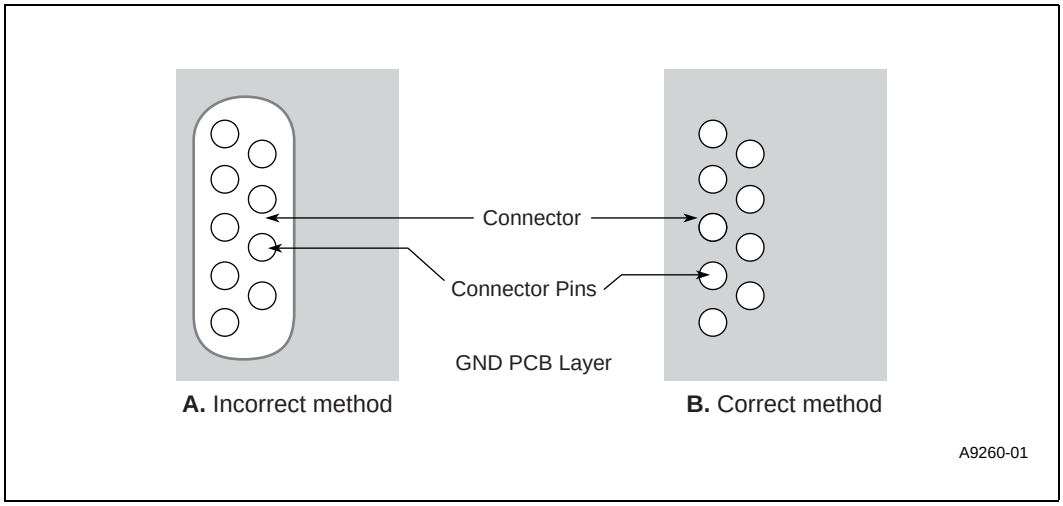
- A general guideline to use is, that space distance between adjacent signals be a least 3.3 times the distance from signal trace to the nearest return plane. The coupled noise between adjacent traces decreases by the square of the distance between the adjacent traces.
- It is also recommended to specify the height of the above reference plane when laying out traces and provide this parameter to the PCB manufacturer. By moving traces closer to the nearest reference plane, the coupled noise decreases by the square of the distance to the reference plane.

Figure 11. Crosstalk Effects on Trace Distance and Height



- Avoid slots in the ground plane. Slots increases mutual inductance thus increasing crosstalk.
- Make sure that ground plane surrounding connector pin fields are not completely cleared out. When this area is completely cleared out, around the connector pins, all the return current must flow together around the pin field increasing crosstalk. The preferred method of laying out a connector in the GND layer is shown in Figure 12.

Figure 12. PCB Ground Layout Around Connectors



6.3 EMI Considerations

It is highly recommended that good EMI design practices be followed when designing with the 41210 Bridge.

- To minimize EMI on your PCB a useful technique is to not extend the power planes to the edge of the board.
- Another technique is to surround the perimeter of your PCB layers with a GND trace. This helps to shield the PCB with grounds minimizing radiation.

The below link can provide some useful general EMI guidelines considerations:

http://developer.intel.com/design/auto/mcs96/applnots/272673.htm

6.4 Power Distribution and Decoupling

Have ample decoupling to ground, for the power planes, to minimize the effects of the switching currents. Three types of decoupling are: the bulk, the high-frequency ceramic, and the inter-plane capacitors.

- Bulk capacitance consist of electrolytic or tantalum capacitors. These capacitors supply large reservoirs of charge, but they are useful only at lower frequencies due to lead inductance effects. The bulk capacitors can be located anywhere on the board.
- For fast switching currents, high-frequency low-inductance capacitors are most effective. Place these capacitors as close to the device being decoupled as possible. This minimizes the parasitic resistance and inductance associated with board traces and vias.
- Use an inter-plane capacitor between power and ground planes to reduce the effective plane impedance at high frequencies. The general guideline for placing capacitors is to place high-frequency ceramic capacitors as close as possible to the module.

6.4.1 Decoupling

Inadequate high-frequency decoupling results in intermittent and unreliable behavior.

A general guideline recommends that you use the largest easily available capacitor in the lowest inductance package. For specific decoupling requirements for a 41210 Bridge application please refer to Chapter 4.

6.5 Trace Impedance

All signal layers require controlled impedance 60 Ω +/- 15%, microstrip or stripline for add-in card applications. Selecting the appropriate board stack-up to minimize impedance variations is very important. When calculating flight times, it is important to consider the minimum and maximum trace impedance based on the switching neighboring traces. Use wider spaces between traces, since this can minimize trace-to-trace coupling, and reduce cross talk.

When a different stack up is used the trace widths must be adjusted appropriately. When wider traces are used, the trace spacing must be adjusted accordingly (linearly).

It is highly recommended that a 2D Field Solver be used to design the high-speed traces. The following Impedance Calculator URL provide approximations for the trace impedance of various topologies. They may be used to generate the starting point for a full 2D Field solver.

http://emclab.umr.edu/pcbtlc/

The following website link provides a useful basic guideline for calculating trace parameters:

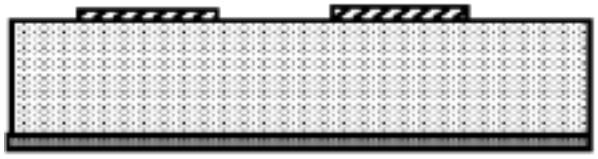
http://www.ultracad.com/calc.htm

Note: Using stripline transmission lines may give better results than microstrip. This is due to the difficulty of precisely controlling the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

6.5.1 Differential Impedance

The PCI Express standard defines a 100 Ω differential impedance. This section provides some basic background information on the differential impedance calculations. In the cross section of Figure 13 shows the cross section of two traces of a differential pair.

Figure 13. Cross Section of Differential Trace



To calculate the coupled impedance requires a 2x2 matrix. The diagonal values in the matrix represent the impedance of the traces to ground and the off-diagonal values provide a measure of how tightly the traces are coupled. The “differential impedance is the value of the line-to-line resistor terminator that optimally terminates pure differential signals.” The two by two matrix is shown below as:

Figure 14. Two-by-two Differential Impedance Matrix

$$Z_o = \begin{bmatrix} Z11 & Z12 \\ Z21 & Z22 \end{bmatrix}$$

B2717 -01

For a symmetric trace Z11 = Z22, the differential impedance can be calculated from this equation:

$Z_{differential} = 2(Z11-Z12)$

For two traces to be symmetric, they must have the same width, thickness and height above the ground plane.[1] With the traces terminated with the appropriate differential, impedance ringing is minimized.

1. “Terminating Differential Signals on PCBs”, Steve Kaufer and Kelee Crisafulli, Printed Circuit Design, March 1999

Board Layout Guidelines 7

This chapter provides details on adapter card stackup suggestions. It is highly recommended that signal integrity simulations be run to verify each 41210 Bridge PCB layout especially if it deviates from the recommendations listed in these design guidelines.

7.1 Adapter Card Topology

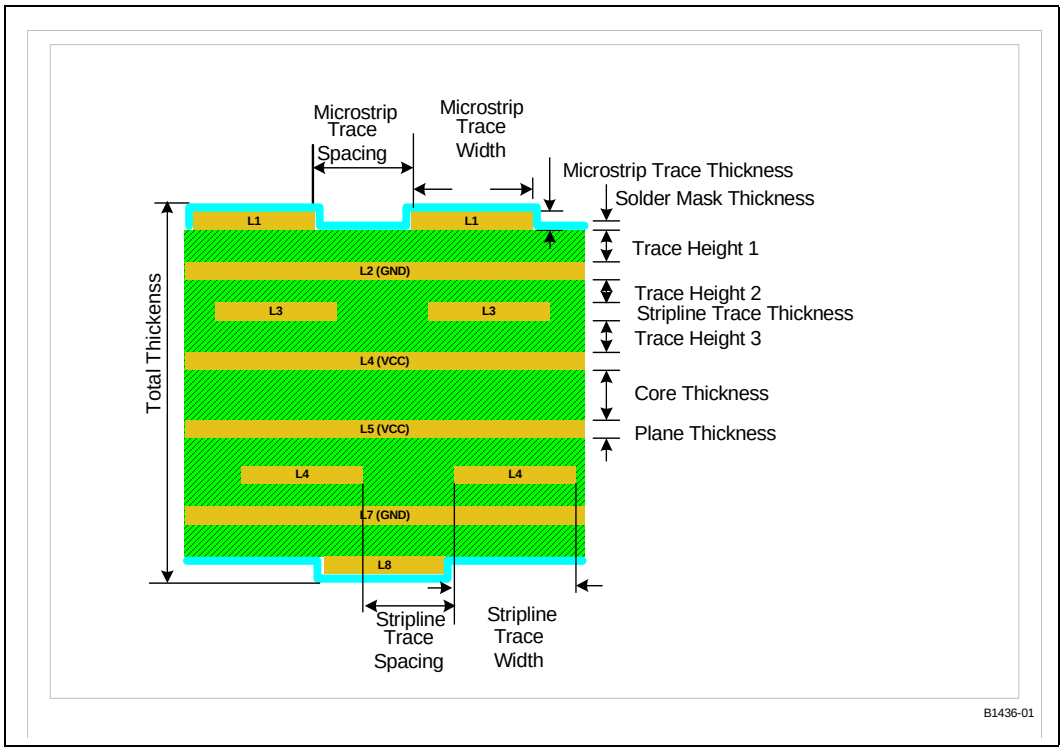
The 41210 Bridge will be implemented on PCI-E adapter cards with an eight layer stackup PCB. The specified impedance range for all adapter card implementations will be 60Ω +/-15%. Adjustments will be made for interfaces specified at other impedances. Table 3 defines the typical layer geometries for eight layer boards.

Table 3. Adapter Card Stack Up, Microstrip and Stripline

Variable	Type	Nominal (mils)	Minimum (mils)	Maximum (mils)	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	2.8	3.0	3.2	
Core E_r	N/A	4.3	3.75	4.85	2113 material
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	The trace height will be determined to achieve a nominal 60 Ω.
	2	3.5	3.3	3.7	
	3	10.5	9.9	11.1	
Preg E_r	Microstrip	4.30	3.75	4.85	2113 material
	Stripline1	4.30	3.75	4.85	2113 material
	Stripline2	4.3	3.75	4.85	7628 material. Trace height 3 is composed of one piece of 2113 and one piece of 7628.
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	4.0	2.5	5.5	
	Stripline	4.0	2.5	5.5	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Spacing (using microstrip E2E/C2C)	[12]/[16]				
Trace Spacing (using stripline E2E/C2C)	[12]/[16]				
Trace Impedance	Microstrip	60	51	69	
	Stripline	60	51	69	

NOTE: Each interface will set the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.

Figure 15. Adapter Card Stackup



PCI-X Layout Guidelines 8

This chapter describes several factors to be considered with a 41210 Bridge PCI/PCI-X design. These include the PCI IDSEL, PCI RCOMP, PCI Interrupts and PCI arbitration.

8.1 Interrupts

PCI Express provides interrupt messages that emulate the legacy wired mechanism. This allows IO devices to signal PCI-style interrupts using a pair of ASSERT and DEASSERT messages This message pairing preserves the level-sensitive semantics of the PCI interrupts on PCI Express.

The 41210 Bridge uses four interrupts - A_INTA:A_INTD on bus A segment and four interrupts B_INTA:B_INTD that corresponding to the four interrupts defined in the PCI specification. The 41210 Bridge routes its PCI interrupt pins and the internal interrupts, to PCI Express INTx interrupts according to Table 4.

Table 4. INTx Routing Table

A_INT# Interrupt Pins	B_INT# Interrupt Pins	PCI Express INTx Message
A_INTA	B_INTA	INTA
A_INTB	B_INTB	INTB
A_INTC	B_INTC	INTC
A_INTD	B_INTD	INTD

The 41210 Bridge will use its primary bus number and device number in the Requester ID field for the PCI Express INTx messages. As stated in the PCI Express specification, the function number is reserved for interrupt messages and will always be 0.

Note: PCI Express Assert_INTx/Deassert_INTx messages are not inhibited by the BME bit.

8.1.1 Interrupt Routing for Devices Behind a Bridge

Given the legacy interrupt sharing scheme shown in Table 4, to get the best legacy interrupt performance (by reducing interrupt sharing), adapter boards have to select the appropriate A_INTX#, B_INTX# (where X is A, B, C or D) input pin to use on each PCI bus segment. The chosen interrupt input also imposes a PCI device number requirement for the interrupt source as specified in the PCI-to-PCI Bridge specification and reproduced in Table 5.

Table 5. Interrupt Binding for Devices Behind a Bridge

Device Number on Secondary Bus	Interrupt Pin on Device	Interrupt on 41210 Bridge
-[a]. 4, 8[b], 12, 16, 20, 24, 28	INTA#	INTA#
	INTB#	INTB#
	INTC#	INTC#
	INTD#	INTD#
1, 5, 9[b], 13, 17, 21, 25, 29	INTA#	INTB#
	INTB#	INTC#
	INTC#	INTD#
	INTD#	INTA#
2, 6, 10[b], 14, 18, 22, 26, 30	INTA#	INTC#
	INTB#	INTD#
	INTC#	INTA#
	INTD#	INTB#
3, 7, 11[b], 15, 19, 23, 27, 31	INTA#	INTD#
	INTB#	INTA#
	INTC#	INTB#
	INTD#	INTC#

a. Device number 0 is reserved for the Bridge and should not be assigned to secondary devices.
b. AD[27:24] which correspond to devices 11:8 should not be used for IDSEL# connections as these signals are used when accessing the extended configuration space in the bridge from the secondary bus.

8.2 PCI Arbitration

The 41210 Bridge supports a high-performance internal PCI arbiter that supports up to seven masters on each PCI segment A and B PCI Buses. The request inputs into the internal arbiter include: six external request inputs and 1 internal request input. All request inputs to the internal arbiter are split into two groups, a high priority group and a low priority group. Any master, including the internal master, can be programmed to be in either of the two groups. This could also mean that all the request inputs into the arbiter could be in one single group. Within a group, priority is round-robin. The entire low-priority group represents one slot in the high priority group. The 41210 Bridge provides a 16-bit arbiter control register to control two aspects of the internal arbiter behavior:

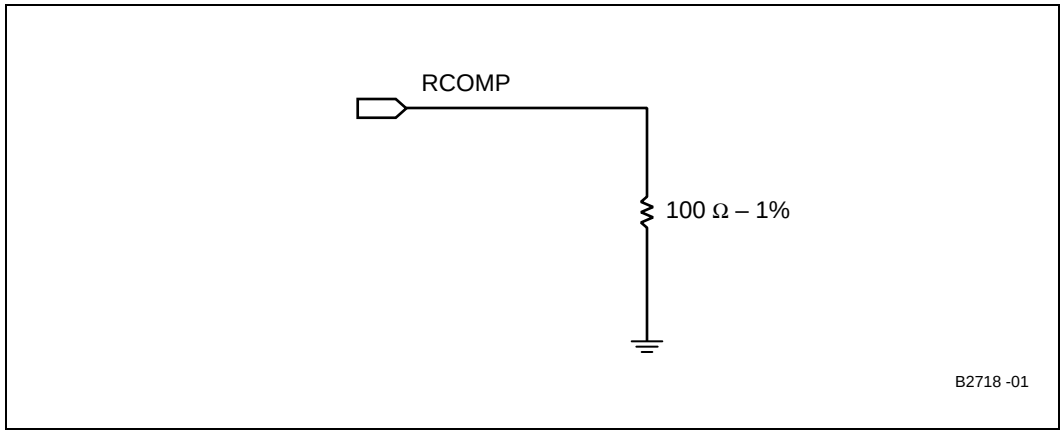
- Priority group for a master (i.e., whether a master is in low priority group or high priority group).
- Bus parking on last PCI agent or the bridge.

By default the arbiter parks the bus on the bridge and drives the A/D, C/BE# and PAR lines to a known value while the bus is idle.

8.2.1 PCI Resistor Compensation

Figure 16 provides the recommended resistor compensation pin termination for the PCI A and PCI B buses.

Figure 16. PCI RCOMP



8.3 PCI General Layout Guidelines

For acceptable signal integrity with bus speeds up to 133 MHz it is important to PCB design layout to have controlled impedance.

- Signal traces should have an unloaded impedance of 60 +/- 10% Ω
- Signal trace velocity should be roughly 150 – 190 ps/inch

There are a couple of general guidelines which should be used when routing your PCI bus signals:

- Avoid routing signals > 8”.
- The following signals have no length restrictions: A_INTA#, A_INTB#, A_INTC#, A_INTD#, B_INTA#, B_INTB#, B_INTC#, B_INTD# and TCK, TDI, TDO, TMS and TRST#. Most PCI-X signals are timing critical. These signals have length restrictions for propagation, setup, and hold requirements. Table 6 shows the PCI-X signals.

Table 6. PCI-X Signals

Timing Critical Signals	A PCI Bus Segment: A_ACK64#, A_AD[63:0], A_CBE_[7:0]#, A_DEVSEL#, A_FRAME#, A_GNT_[5:0]#, A_IRDY#, A_LOCK#, A_PAR64, A_REQ64#, A_REQ_[5:0]#, A_STOP#, A_TRDY#, A_CLKO[6:0], A_CLKI B PCI Bus Segment: B_ACK64#, B_AD[63:0], B_CBE_[7:0]#, B_DEVSEL#, B_FRAME#, B_GNT_[5:0]#, B_IRDY#, B_LOCK#, B_PAR64, B_REQ64#, B_REQ_[5:0]#, B_STOP#,B_TRDY#, B_CLKO[6:0], B_CLKI
Reset Signals	A PCI Bus Segment: A_RST#, A_PME# B PCI Bus Segment: B_RST#, B_PME#
Non Timing Critical Signals	A PCI Bus Segment: A_133EN, A_IRQ[15:0]#, A_M66EN, A_PCIXCAP, A_PERR#, A_SERR# B PCI Bus Segment: B_133EN, B_IRQ[15:0]#, B_M66EN, B_PCIXCAP, B_PERR#, B_SERR#

Table 7. PCI/PCI-X Frequency/Mode Straps

A_PCIXCAP, B_PCIXCAP	A_M66EN, B_M66EN	A_133EN, B_133EN (on board)	Bus Mode/ Freq
0	0	X	**PCI 33**
0	1	X	**PCI 66**
PCI-X 66MHz cards connect this signal to ground through a 10KΩ ±5% resistor in parallel with a 0.01uF ±10% capacitor.	X	X	**PCI-X 66**
PCI-X 133 MHz cards connect PCIXCAP to ground through a 0.01uF ±10% capacitor.	X	0	**PCI-X 100**
PCI-X 133 MHz cards connect PCIXCAP to ground through a 0.01uF ±10% capacitor.	X	1	**PCI-X 133**

Note: All signals sampled on the rising edge of **PERST#**.

8.3.1 PCI Pullup Resistors Not Required

PCI control signals on the 41210 Bridge do NOT require pullup resistors on the adapter card to ensure that they contain stable values when no agent is actively driving the bus. These include:

A_ACK64#, A_AD[63:32], A_CBE#[7:4], A_DEVSEL#, A_FRAME#, A_INTA#, A_INTB#, A_INTC#, A_INTD#, A_IRDY#, A_PERR#, A_PAR, A_GNT#[5:0], A_REQ#[5:0], A_LOCK#, A_PAR64, A_REQ64#, A_SERR#, A_STOP#, A_TRDY#, B_ACK64#, B_AD[63:32],

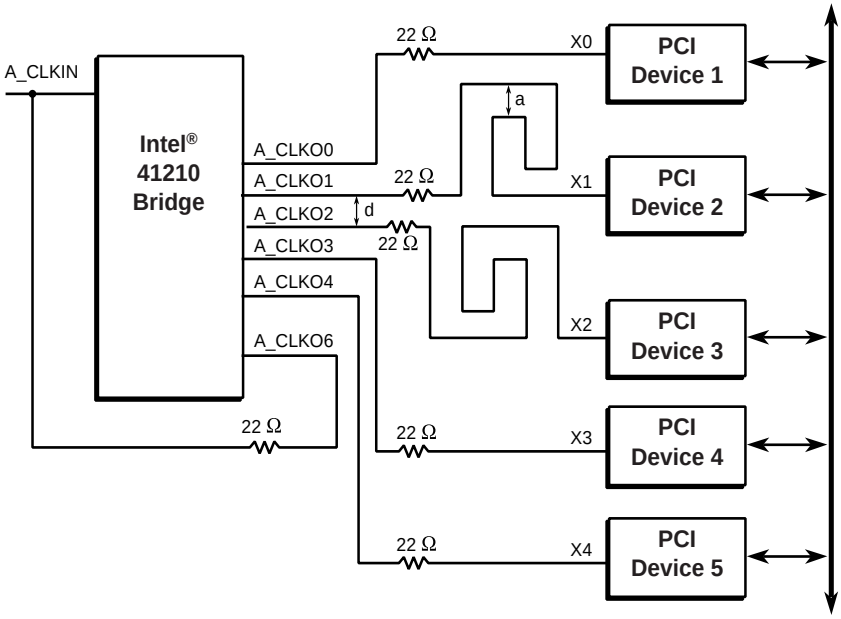
B_CBE#[7:4], B_DEVSEL#, B_FRAME#, B_INTA#, B_INTB#, B_INTC#, B_INTD#, B_IRDY#, B_PERR#, B_PAR, B_GNT#[5:0], B_REQ#[5:0], B_LOCK#, B_PAR64, B_REQ64#, B_SERR#, B_STOP#, and B_TRDY#.

8.4 PCI Clock Layout Guidelines

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b compliant, allows a maximum of 0.5 ns clock skew timing for each of the PCI-X frequencies: 66 MHz, 100 MHz and 133 MHz. A typical PCI-X application may require separate clock point-to-point connections distributed to each PCI device. The 41210 Bridge provides seven buffered clocks on the PCI bus to connect to multiple PCI-X devices. The Figure 17 shows the use of four PCI “A” clock outputs and length matching requirements. These same guidelines apply to the 41210 Bridge PCI “B” clock outputs. The recommended clock buffer layout are specified as follows:

- Match each of the used the 41210 Bridge output clock lengths A_CLK[6:0] and B_CLK[6:0] to within 0.1” to help keep the timing within the 0.5 ns maximum budget.
- Keep the distance between the clock lines and other signals “d” at least 25 mils from each other.
- Keep the distance between the clock line and itself “a” at a minimum of 25 mils apart (for serpentine clock layout).
- A_CLKIN gets connected to A_CLKO6 through a 22Ω +/- 1% resistor and likewise for B_CLKIN is connected to B_CLKO6 through a 22Ω resistor.
- The 22 +/- 1% Ω resistor is within 500 mils of A_CLKO.

Figure 17. PCI Clock Distribution and Matching Requirements



Notes:
– PCI Clock Lengths X0, X1, X2, X3 and X4 should be matched within 0.1 inch of each other.
– Minimum separation between two different CLKs, "d".
– Minimum separation between two segments of the same CLK line, "a".

B1499-04

Table 8. PCI-X Clock Layout Requirements Summary

Parameter	Routing Guidelines
Signal Group	PCI Clocks B_CLKO[6:0], A_CLK[6:0]
Reference Plane	Route over unbroken ground or power plane
Stripline Trace Width	4 mils
Stripline Trace Spacing: Separation between two different clock lines, “d” clock lines	25 mils center to center from any other signal
Stripline Trace Spacing: Separation between two segments of the same clock line (on serpentine layout), “a” dimension	25 mils center to center from any other signal
Stripline Trace Spacing: Separation between clocks and other lines	50 mils center to center from any other signal
Length Matching Requirements	All 41210 Bridge Output Clocks B_CLK0[6:0] and A_CLK[6:0] connected to devices must be length matched to 0.1 inch of each other.
	The clock feedback line lengths from A_CLKOUT to A_CLKIN and B_CLKOUT to B_CLKIN should be length matched to all other clock lines within 0.1”.
Total Length of the 41210 Bridge PCI CLKs on the adapter card	10” -14”
A_CLKIN, B_CLKIN Series Termination	Connect A_CLKIN to one end of a 22Ω +/- 1% resistor and the other end connected to A_CLKOUT and connect B_CLKIN to one end of a 22Ω resistor and the other end connected to B_CLKOUT
A_CLK[6:0], B_CLK[6:0] Series Termination	Each of the clock outputs A_CLKO[6:0] and B_CLK[6:0] should have series 22Ω resistor located within 500 mils of the 41210 Bridge clock output.
Routing Guideline 1	Point to point signal routing should be used to keep the reflections low.
Routing Guideline 2	Minimize number of vias

8.5 PCI-X Topology Layout Guidelines

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b compliant, recommends the following guidelines for the number of loads for your PCI-X designs. Any deviation from these maximum values requires close attention to layout with regard to loading and trace lengths.

Table 9. PCI-X Slot Guidelines

Frequency	Maximum Loads	Maximum Number of Slots
66 MHz	8	4
100 MHz	4	2
133 MHz	2	1

8.6 Intel® 41210 Serial to Parallel PCI Bridge Design Guide Layout Analysis

The following sections describes layout recommendations based on the presilicon signal integrity analysis. This analysis was conducted using the following parameters:

- Card stack up: 60 Ω +/- 15% single-ended impedance
- Driver Model 41210 Bridge IBIS
- Receiver Model: generic models for PCI-X and PCI
- Driver Package Model: Preliminary 41210 Bridge Model
- Cross talk and ISI impact on timing were not modeled

8.6.1 Embedded PCI-X 133 MHz

This section lists the routing recommendations for PCI-X 133 MHz without a slot. Figure 18 shows the block diagram of this topology and Table 10 describes the routing recommendations.

Figure 18. Embedded PCI-X 133 MHz Topology

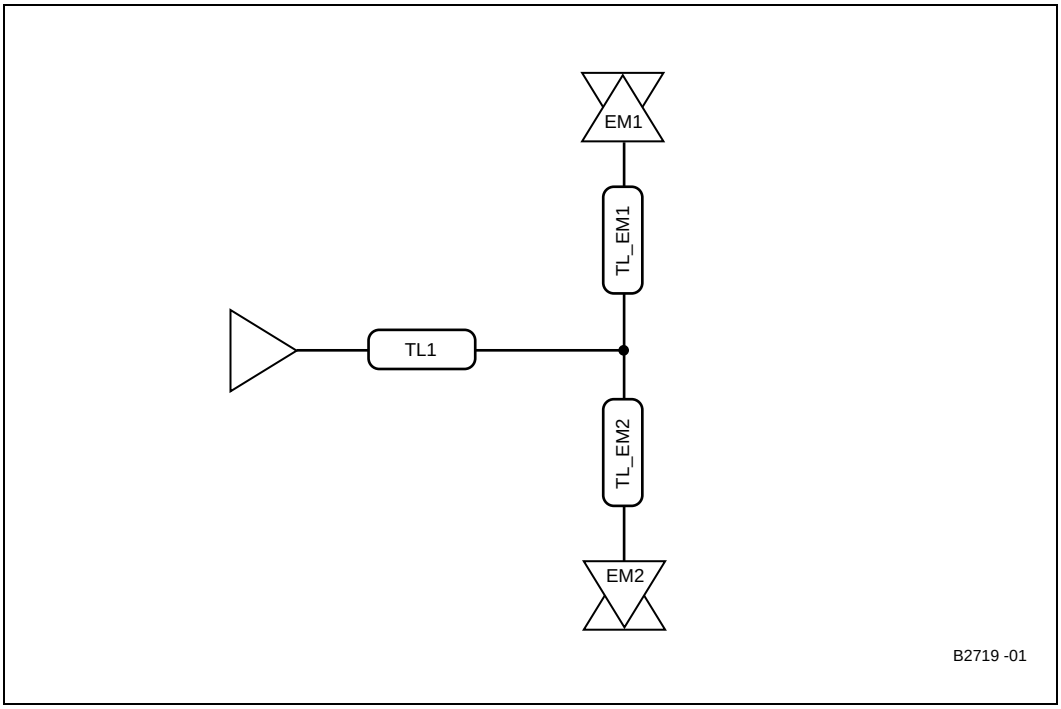


Table 10. Embedded PCI-X 133 MHz Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane	Route over an unbroken ground plane
Board Impedance	60 Ω +/- 15%
Stripline Trace Spacing	12 mils from edge to edge
Microstrip Trace Spacing	18 mils, from edge to edge
Break Out	5 mils on 5 mils spacing. Maximum length of breakout region can be 500 mils
Group Spacing	Spacing from other groups: 25 mils min, edge to edge
Trace Length 1 (TL1): From 41210 Bridge signal Ball to first junction	1.75” min - 4.0” max
Trace Length 3 junction of TL_EM1 and TL_EM2 to the embedded device	1.25” min - 3.25” max
Length Matching Requirements:	Clocks coming form the clock driver must be on the same layer and length matched to within 25 mils.
Number of vias	3 vias max per path

8.6.2 Embedded PCI-X 100 MHz

This section lists the embedded routing recommendations for PCI-X 100 MHz. Figure 19 shows the block diagram of this topology and Table 11 describes the routing recommendations.

Figure 19. Embedded PCI-X 100 MHz Topology

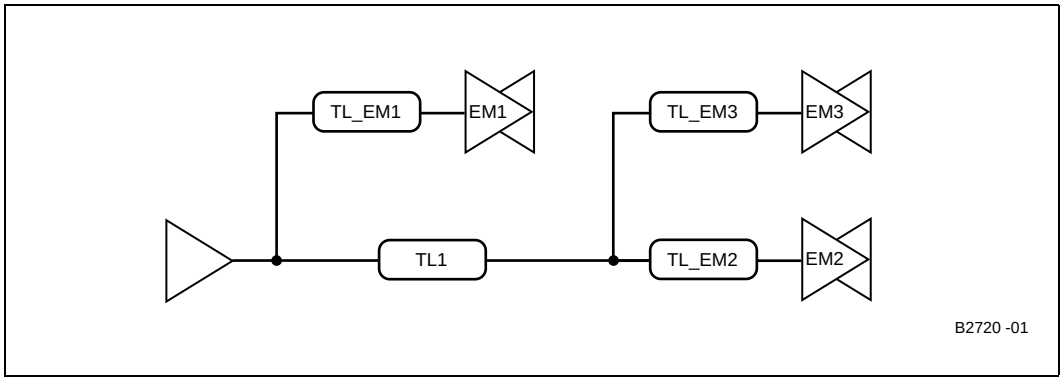


Table 11. Embedded PCI-X 100 MHz Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane	Route over an unbroken ground plane
Board Impedance	60 Ω +/- 15%
Stripline Trace Spacing	12 mils from edge to edge
Microstrip Trace Spacing	18 mils, from edge to edge
Break Out	5 mils on 5 mils spacing. Maximum length of breakout region can be 500 mils
Group Spacing	Spacing from other groups: 25 mils min, edge to edge
Trace Length 1 (TL1): From 41210 Bridge signal Ball to first junction	0.5” min - 3.0” max
Trace Length: TL_EM1: from 41210 Bridge signal ball to the first embedded device	2.5” min - 3.5” max
Trace Length TL_EM2 - TL_EM3: from junction to the embedded device	1.5” min - 3.5” max
Length Matching Requirements:	Clocks coming form the clock driver must be on the same layer and length matched to within 25 mils.
Number of vias	4 vias max per path

8.6.3 PCI-X 66 MHz Embedded Topology

Figure 20 and Table 12 provide routing details for a topology with an embedded PCI-X 66 MHz application.

Figure 20. PCI-X 66 MHz Embedded Routing Topology

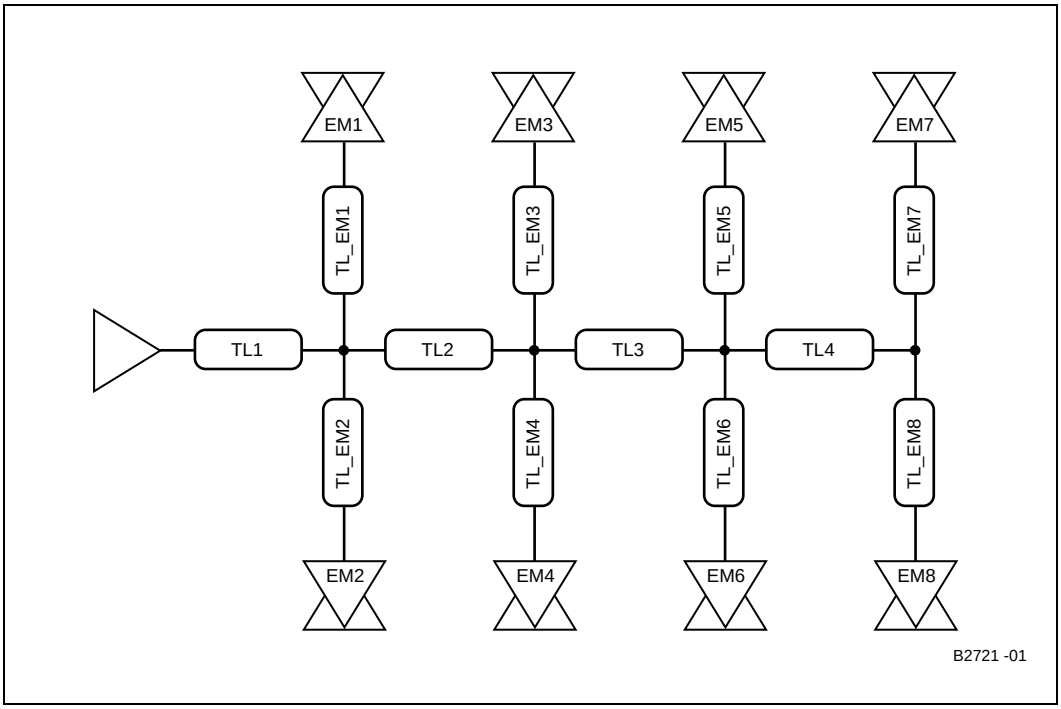


Table 12. PCI-X 66 MHz Embedded Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane	Route over an unbroken ground plane
Board Impedance	60 Ω +/- 15%
Stripline Trace Spacing	12 mils edge to edge
Microstrip Trace Spacing	18 mils, edge to edge
Break Out	5 mils on 5 mils. Maximum length of breakout region can be 500 mils
Group Spacing	Spacing from other groups: 25 mils min, edge to edge
Trace Length 1 (TL1): From 41210 Bridge signal Ball to first junction	1.0” - 5.0” max
Trace Length TL2 to TL4 - between junctions	1.0” min - 2.5” max
Trace Length TL_EM1 to TL_EM8 from junction connector to the embedded device	2.0” min - 3.0” max
Length Matching Requirements:	Clocks coming form the clock driver must be length matched to within 25 mils and routed identical in layers.
Number of vias	4 vias max.

8.6.4 PCI 66 MHz Embedded Topology

Figure 21 and Table 13 provide routing details for a topology with an embedded PCI 66 MHz design.

Figure 21. PCI 66 MHz Embedded Topology

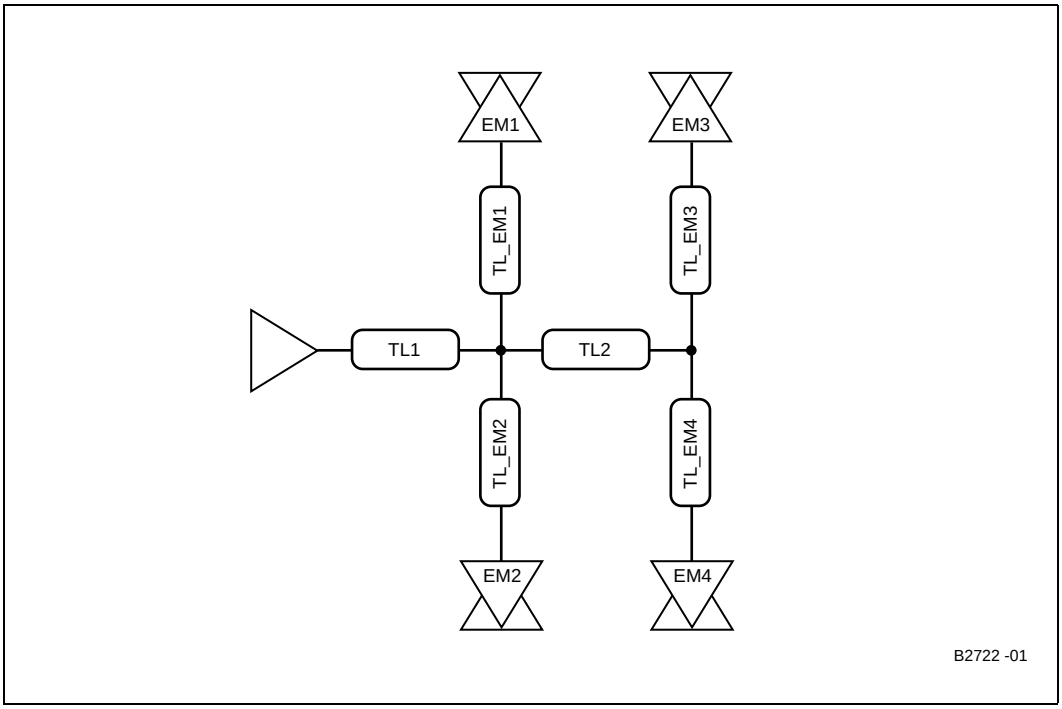


Table 13. PCI 66 MHz Embedded Table

Parameter	Routing Guideline for Lower AD Bus
Reference Plane	Route over an unbroken ground plane
Board Impedance	60 Ω +/- 15%
Microstrip Trace Spacing	18 mils center to center
Stripline Trace Spacing	12 mils center to center
Group Spacing	Spacing from other groups: 25 mils min, edge to edge
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region can be 500 mils.
Trace Length 1 TL1: From 41210 Bridge signal Ball to first junction	5.0” max
Trace Length TL2 between junctions	0.5” min - 3.5” max
Trace Length TL_EM1 to TL_EM4 from junction to embedded devices	2.0” min - 3.0” max
Length Matching Requirements	Clocks coming from the clock driver must be length matched to within 25 mils.
Number of vias	4 vias max.

8.6.5 PCI 33 MHz Embedded Mode Topology

Figure 22 and Table 14 provide routing details for a topology with an embedded PCI 33 MHz design.

Figure 22. PCI 33 MHz Embedded Mode Routing Topology

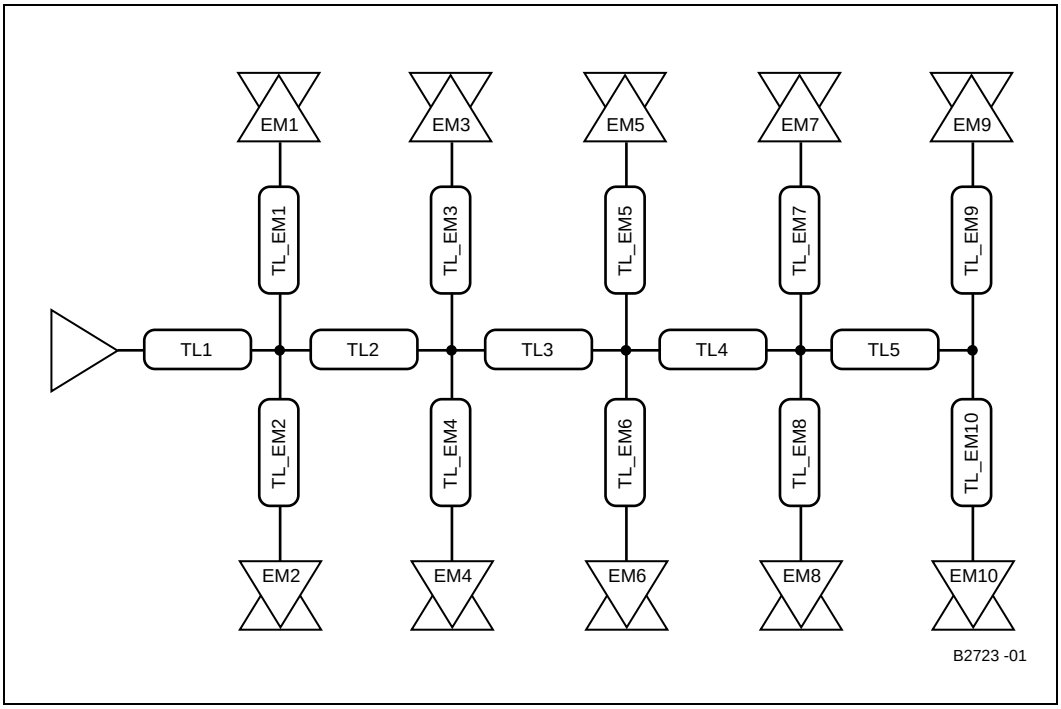


Table 14. PCI 33 MHz Embedded Routing Recommendations

Parameter	Routing Guideline for Lower AD Bus
Reference Plane	Route over an unbroken ground plane
Board Impedance	60 Ω +/- 15%
Stripline Trace Spacing	12 mils, edge to edge
Microstrip Trace Spacing	18 mils edge to edge
Group Spacing	Spacing from other groups: 25 mils min, edge to edge
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region can be 500 mils.
Trace Length 1 TL1: From 41210 Bridge signal Ball to first junction	5.0” max
Trace Length TL2 to TL5 - between junctions	0.5” min - 3.5” max
Trace Length TL_EM1 to TL_EM10 from junction to embedded devices	2.0” min - 3.0” max
Length Matching Requirements	Clocks coming from the clock driver must be length matched to within 25 mils.

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PCI Express Layout 9

This section provides an overview of the PCI-Express stackup recommended based on Intel presimulation results. For additional information, refer to the *Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual* or the *PCI Express Specification*, Revision 1.0a from the www.pcisig.com website.

9.1 General recommendations

PCI Express is a serial differential low-voltage point-to-point interconnect. The PCI Express was designed to support 20 inches between components with standard FR4. The 41210 Bridge supports x8 lanes. PCI-Express requires special considerations be made for interconnect losses, jitter, crosstalk and mode conversions. The below list provides some general guidelines for the layout of a PCI-Express trace:

1. **Jitter**: Trace lengths of a PCB trace can introduce around 1 to 5 ps of jitter and 0.35 to 0.5 dB of loss per inch of differential pair. An add-in card the trace length from edge-finger pad to device is limited to 3 inches.
2. **Matching within pair**: Trace lengths of matching differential pairs are required to be matched within +/-5 mil delta. Each net within a differential pair should be length matched on a segment-by-segment basis at point of discontinuity such as an breakout area, routes between vias, routes between AC coupling capacitors and connector pins.
3. **Trace Symmetry**: Trace Symmetry is required between two traces of the same differential pair.
4. **Vias**: Vias contribute 0.5 to 1.0 dB/via toward the loss budget. Vias on an add-in card should be limited to one near the breakout section of the pads and one near the edge finger.
5. **Bends**: Trace bends should be kept to a minimum. If bends are used they should be at a 45-degree angle or smaller. The number of left and right bends should be matched as closely as possible to even out the overall lengths of each segment of the differential pair.
6. **AC Coupling capacitors:** AC coupling capacitor with a value of 75nF to 200nF should line up at the same location from one trace to the other within the pair. The 0402 size capacitor with a small pad size is highly recommended. The breakout from the capacitor should be symmetrical for both signal traces in the differential pair.
7. **Connector pins:** Length compensation for the connector pins of the differential pair being offset from each other the PCB trace should be considered.
8. **Ground Plane Referencing**: Ground plane referencing is required along the entire route of the differential pair. Traces routed near the edge should maintain a 40 mil air gap to the edge. Layer switching should also maintain the ground plane. Grounds between planes should be connected with stitching vias (with one to three recommended per differential pair).
9. **Breakout Areas**: Breakout areas near a device package should be limited to 500 mils in lengths. The necking down to a smaller trace width should be symmetrical on the differential pair.

9.2 PCI-Express Layout Guidelines

The layout guidelines for PCI-Express were developed for an adapter card topologies. The models and assumptions used in development of these guidelines were as follows:

- Add-In Card Stackup: 60 Ω single-ended impedance
- Target Differential Impedance: 100 Ω +/- 20%.
- Driver Model: 41210 Bridge PCI-E IBIS
- Receiver Model: 41210 Bridge PCI-E IBIS. Specification model did not meet specifications
- Driver Package Model: Preliminary 41210 Bridge model.
- No receiver package model used since specification eye is at package pin.
- Assumed that traces in a lane could be routed totally on microstrip, totally on stripline, or a mixture of microstrip and stripline.
- AC coupling capacitors were modeled as a parasitic resistor and inductor in series.
- Add-in card was modeled as micro-strip routes only.
- No vias were modeled at this time.
- Only the receiver eye was evaluated. The next revision will evaluate the eye at the transmitter and connector as well as the receiver.

9.3 Adapter Card Layout Guidelines

Table 15. Adapter Card Routing Recommendations (Sheet 1 of 2)

Parameter	Routing Guidelines
Reference Plane	Route over an unbroken ground plane
Target Single Ended Impedance	60 Ω nominal
Target Differential Impedance	100 Ω +/- 20% Differential Impedance
Microstrip and Stripline Trace Width	4 mils
Microstrip Trace Spacing	Intrapair: 10 mils center-to-center Interpair: 30 mils center-to-center 22 mils. center to center (pair to pair). Transmit and Receive pairs should be interleaved. If no interleaving, then inter pair spacing should be increased to 50 mils (c2c). Center to center of inter pair is defined as center of Positive of one pair to Center of Negative of the next or vice versa
Group Spacing	Spacing from other groups: 25 mils minimum, center to center
Transmit Trace Length (41210 Bridge signal pin to AC coupling capacitor.)	0.25”- 5.0” max
Transmit Trace Length (AC coupling capacitor to card edge finger.)	1.00”- 4.5” max

Table 15. Adapter Card Routing Recommendations (Sheet 2 of 2)

Receive Trace Length (Card edge finger to 41210 Bridge receiver pin	1.0” min - 6.0” max
Length Matching Requirements:	Total allowable intra-pair length mis-match must not exceed 25 mils. Each routing segment should be matched as close as possible. Total skew across all lanes must be less than 20 ns. See the PCI-Express Desktop Design Guidelines for additional routing requirements
Number of vias	4 max

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Circuit Implementations 10

This chapter describes 41210 Bridge circuit implementations.

10.1 41210 Bridge Analog Voltage Filters

The Intel® 41210 Serial to Parallel PCI Bridge requires several external analog voltage filter circuits to be placed on the system board, three for the PCI interface, one for the PCI Express interface, and one for the bandgap voltage. The 41210 Bridge lists the recommended filter values for these filter circuits -- any one of the filter circuits can use any one of the four R, L and C combinations shown in Table 16, except that configuration number 4 cannot be used for the PCI Express analog voltage filter.

Table 16. Recommended R, L and C Values for 41210 Bridge Analog Filter Circuits

Config	R	L	C
1	0.5Ω ±1% 1/16W	4.7uH ±25% PCI, PCI-E: 45mA Bandgap: 30mA	33uF ±20% 6.3V
2	0.5Ω ±1% 1/16W	4.7uH ±20 PCI, PCI-E: 45mA Bandgap: 30mA%	22uF ±20% 6.3V
3	0.5Ω ±1% 1/16W	4.7uH ±20% PCI, PCI-E: 45mA Bandgap: 30mA	2x10uF ±20% 6.3V
4[a]	1.0Ω ±1% 1/16W	4.7uH ±20% PCI: 45mA Bandgap: 30mA	10uF ±20% 6.3V

a. Configuration number 4 cannot be used for the PCI Express analog voltage filter.

Additional notes:

L (Inductor)

- L must be magnetically shielded
- ESR: max < 0.4Ω
- rated at 45mA (or 30mA for bandgap circuit only)

C (Capacitor)

- ESR: max < 0.5Ω
- ESL < 3.0nH

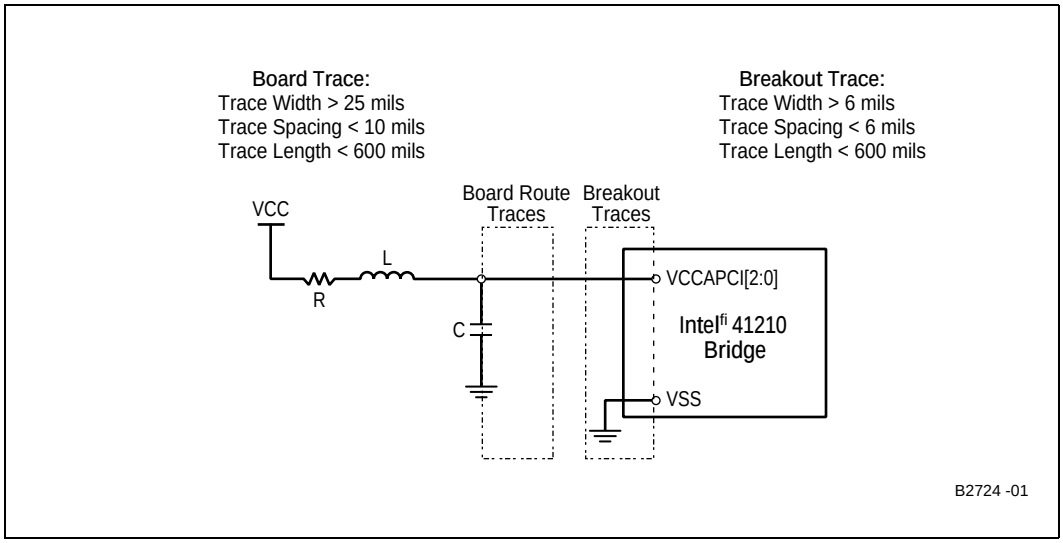
R (Resistor)

- 1/16W

10.1.1 PCI Analog Voltage Filters

The following filter circuit is recommended for the PCI interface. Three separate, identical versions of this circuit should be placed on the system board, one for each **VCCAPCI[2:0]** pin on the Intel® 41210 Serial to Parallel PCI Bridge.

Figure 23. PCI Analog Voltage Filter Circuit



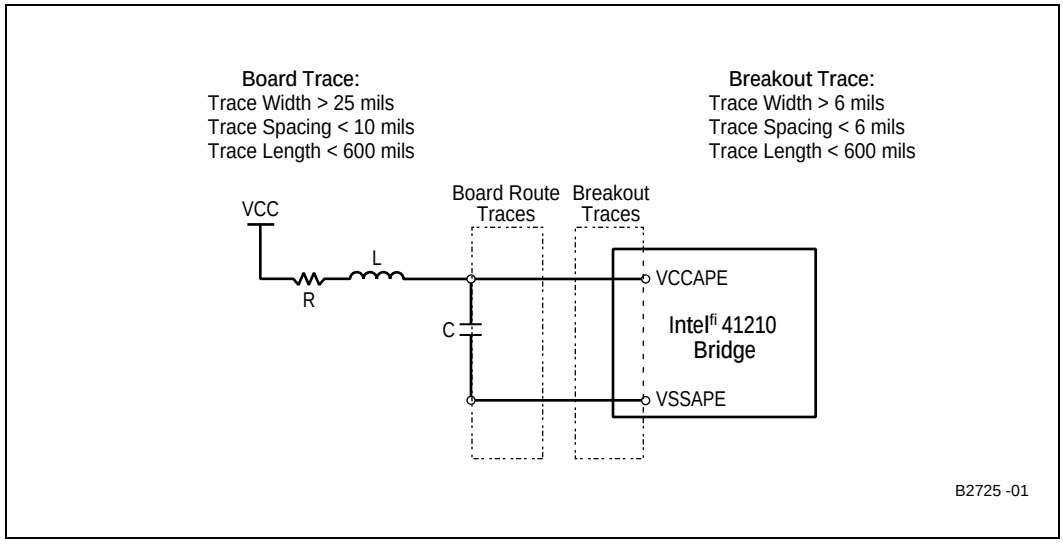
Note: Three of these PCI filter circuits must be placed on the system board, one for each of the **VCCAPCI[2:0]** pins on the Intel® 41210 Serial to Parallel PCI Bridge.

- Place C as close as possible to package pin.
- R must be placed between VCC15 and L.
- Route VCCPCI[x] and VSS as differential traces.
- VCCPCI[x] and VSS traces must be ground referenced (No VCC15 references).
- Max total board trace length = 1.2”.
- Min trace space to other nets = 30 mils.

10.1.2 PCI Express Analog Voltage Filter

Figure 24 shows the PCI Express Analog Voltage Circuit.

Figure 24. PCI Express Analog Voltage Filter Circuit



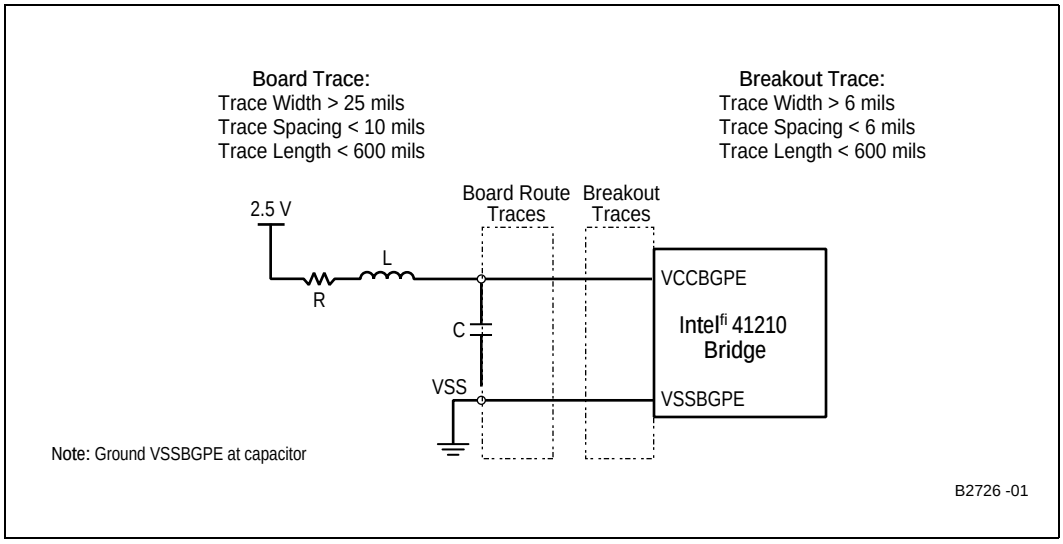
Note: .

- Place C as close as possible to package pin.
- R must be placed between VCC15 and L.
- Route VCCAPE and VSSAPE as differential traces.
- VCCAPE and VSSAPE traces must be ground referenced (No VCC15 references).
- Max total board trace length = 1.2”.
- Min trace space to other nets = 30 mils.

10.1.3 Bandgap Analog Voltage Filter

Figure 25 Shows the Bandgap Analog Voltage Filter.

Figure 25. Bandgap Analog Voltage Filter Circuit



Note: .

- Place C as close as possible to package pin.
- R must be placed between the 2.5V supply and L.
- Route VCCBGPE and VSSBGPE as differential traces.
- VCCBGPE and VSSBGPE traces must be ground referenced (No 2.5V references).
- VSSBGPE should be grounded at the capacitor.
- Max total board trace length = 1.2”.
- Min trace space to other nets = 30 mils.

10.2 Intel® 41210 Serial to Parallel PCI Bridge Reference and Compensation Pins

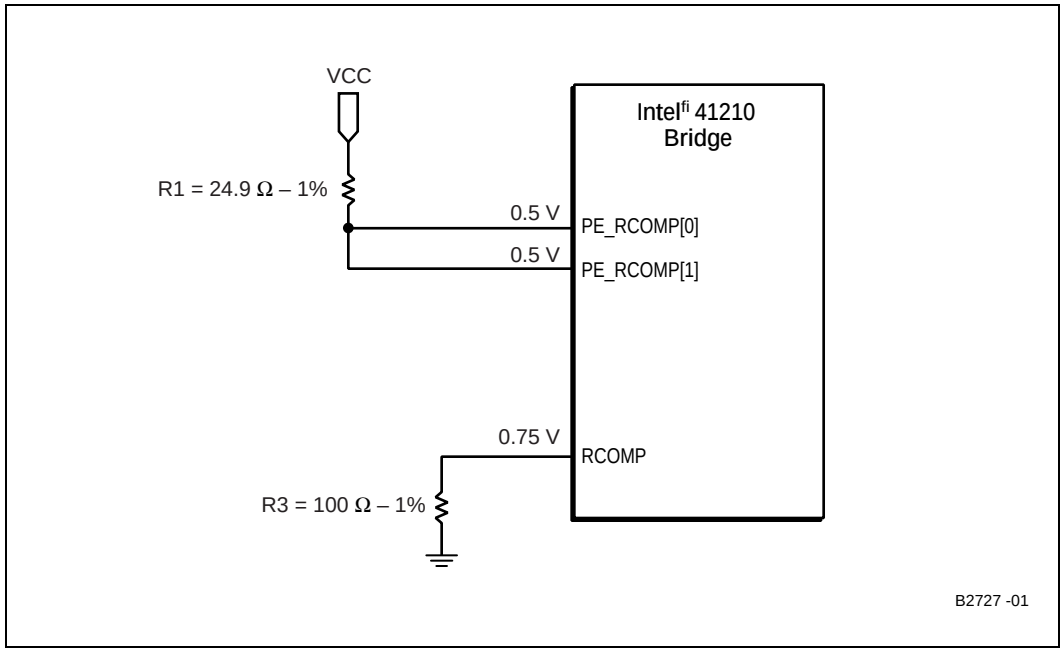
There are three compensation pins on Intel® 41210 Serial to Parallel PCI Bridge.

PE_RCOMP[1:0] are two separate pins that provide voltage compensation for the PCI Express interface on the Intel® 41210 Serial to Parallel PCI Bridge. The nominal compensation voltage is 0.5V. An external 24.9Ω ±1% pullup resistor should be used to connect to VCC15. A single pullup resistor can be used to for both of these signals.

RCOMP is an analog PCI interface compensation pin, providing 0.75V to the Intel® 41210 Serial to Parallel PCI Bridge. A 100Ω ±1% pulldown resistor should be used to connect the **RCOMP** pin to ground.

These implementations are shown in Figure 26.

Figure 26. Reference and Compensation Circuit Implementations



10.2.1 SM Bus

The SMBus interface does not have configuration registers. The SMBus address is set by the states of pins **SMBUS[5]** and **SMBUS [3:1]** when **PERST#** is asserted as described in Table 17.

Table 17. SMBUs Address Configuration

Bit	Value
7	1
6	1
5	SMBUS[5]
4	0
3	SMBUS[3]
2	SMBUS[2]
1	SMBUS[1]

Refer to Section 2.4 for details on how to use the SMBus to initialize 41210 Bridge registers with a microcontroller.

41210 Bridge Customer Reference Boards 11

This chapter describes the 41210 Bridge Customer Reference Board (CRB).

11.1 Board Stack-up

The proposed layout of the PCB is eight layers with the following stackup:

- Signal #1 (Top/Component Side)
- Ground Plane: GND
- Signal #2
- Power Plane
- Power Plane
- Signal #3
- Ground Plane
- Signal #4 (Bottom)

The permittivity constant Er = 4.5

Table 18. CRB Board Stackup

Layer	Type	Thickness (mils)	Copper Weight
1	Signal	2.00	1/2 + plating
	Prepreg	4.50	
2	Plane: GND	1.20	1
	Core	4.80	
3	Signal	1.20	1
	Prepreg	14.00	
4	Plane: PWR	1.20	1
	Core	3.8	
5	Plane: PWR	1.20	1
	Prepreg	14.00	
6	Signal	1.20	1
	Core	4.80	
7	Plane: Power	1.20	1
	Prepreg	4.50	
8	Signal	2.00	1/2 + plating
Est. Total Thickness		**62 +/- 7**	

11.2 Material

The following materials are used with the 41210 Bridge CRB:

- FR-4, 0.062 in. +/- .007, 1.0 oz Copper Power/GND.
- Full length PCI Raw Card (3.3V Universal) 6.2” high x 7.00” long max with ½ inch cut away.

11.3 Impedance

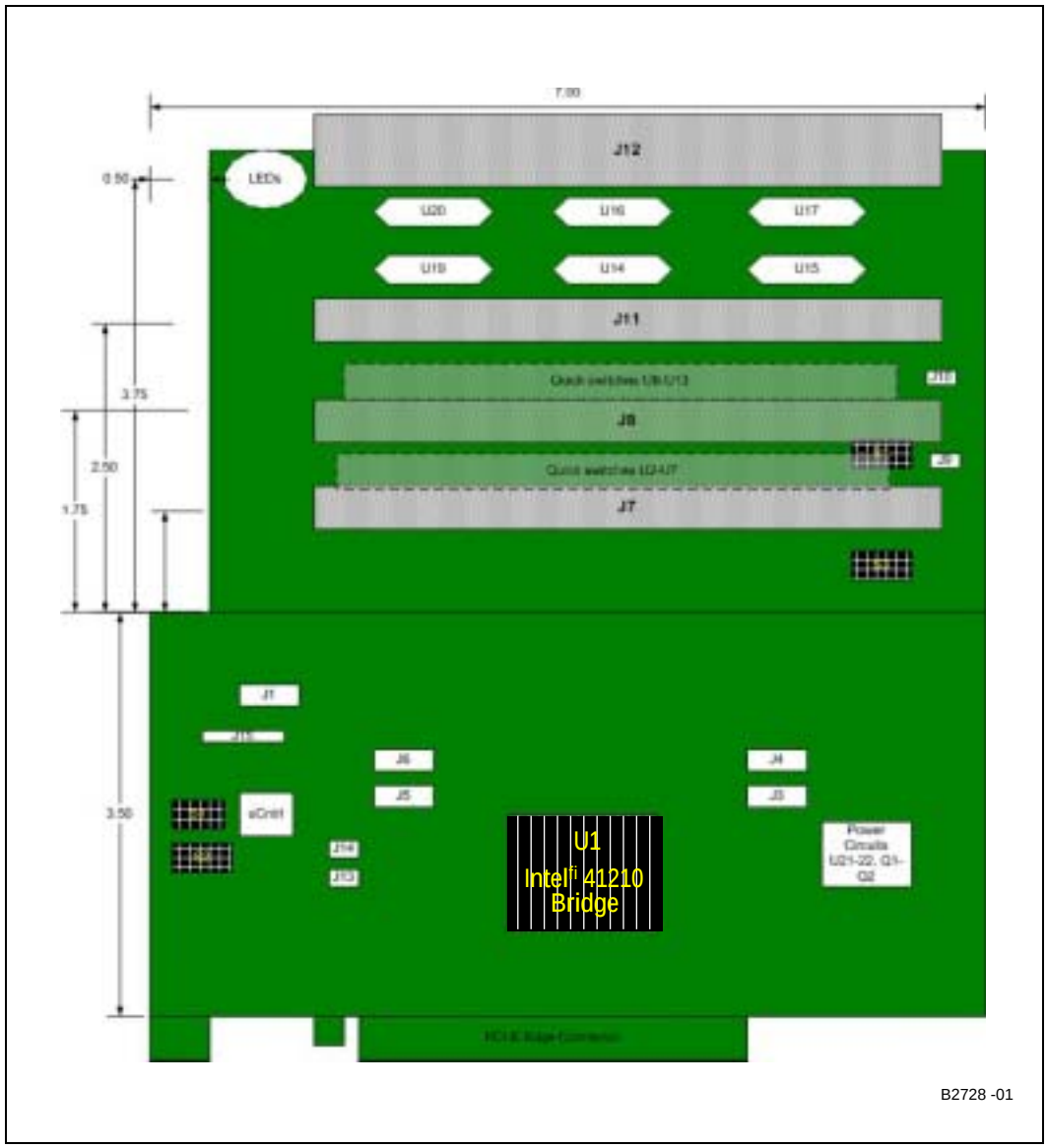
Most signal layers require controlled Impedance of 60 Ω +/- 5% microstrip or stripline where appropriate.

Differential signals for the PCI-E interface require matched 100 Ω differential termination realized as matched 50Ω resistances referenced to ground.

11.4 Board Outline

Figure 27 provides the mechanical outline of the 41210 Bridge CRB.

Figure 27. Mechanical Outline of the 41210 Bridge



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Design Guide Checklist 12

This checklist highlights design considerations that should be reviewed prior to manufacturing an adapter card that implements the 41210 Bridge product. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. This is not a complete list and does **not** guarantee that a design will function properly.

Table 19. PCI Express Interface Signals

Signals	Recommendations	Reason/Impact
REFCLKn, REFCLKp	Must be connected to clock from a PCI Express connector for add-in card designs or to a 100MHz oscillator for an embedded design.	
PE_RCOMP[1:0]	24.9Ω ±1% pullup resistor to 1.5V. A single resistor can be used for both signals. Place resistor as close as possible to REFCLKn, REFCLKp pins.	PCI Express compensation pin. 0.5V nominal.
PERP[7:0] PERN[7:0]	For X1 mode, only signals PERp[0] and PERn[0] or PERp[7] and PERn[7] are used. For X4 mode, only signals PERp[3:0] and PERn[3:0] are used. For X8 mode, all of these signals, PERp[7:0] and PERn[7:0], are used.	PCI Express data serial inputs (differential data receive signals).
PETP[7:0] PETN[7:0]	For X1 mode, only signals PETp[0] and PETn[0] or PETp[7] and PETn[7] are used. For X4 mode, only signals PETP[3:0] and PETN[3:0] are used. For X8 mode, all of these signals, PETP[7:0] and PETN[7:0], are used.	PCI Express data serial inputs (differential data transmit signals).

Table 20. PCI/PCI-X Interface Signals

Signals	Recommendations	Reason/Impact
X_AD[63:32] X_CBE[7:4]# X_DEVSEL# X_FRAME# X_IRDY# X_TRDY# X_STOP# X_PERR# X_SERR# X_REQ[5:0]# X_GNT[5:0]# X_LOCK# X_PAR X_PAR64 X_ACK64# X_REQ64#	No external pullup resistors required on system board.	41210 Bridge has internal pullup resistors on these signals. X_AD[31:0] and X_CBE#[3:0] signals do not require pullups according to the PCI Specification.
A_133EN B_133EN	Only relevant when running in PCI-X Mode (X_PCIXCAP = 1). Determines the max PCI-X Mode 1 frequency for a particular segment (100 MHz or 133 MHz): 0 = 100 MHz PCI-X max frequency 1 = 133 MHz PCI-X max frequency Use an 8.2KΩ pullup resistor to VCC33. This resistor is located on the system board.	Sampled on the rising edge of PERST#.
A_INTA#, A_INTB#, A_INTC#, A_INTD#, B_INTA#, B_INTB#, B_INTC#, B_INTD#	No pullup resistors required on these signals.	The 41210 Bridge has internal pullup resistors on these signals.

Table 20. PCI/PCI-X Interface Signals

Signals	Recommendations	Reason/Impact
A_M66EN B_M66EN	Controls frequency of the PCI segment when running in conventional PCI mode (33 MHz or 66 MHz): 0 = 33 MHz PCI 1 = 66 MHz PCI • Pull-up using a 8.2KΩ resistor when the PCI bus is to operate at 66 MHz and not already pulled up by system board. This signal is grounded for 33 MHz operation. • Connect **M66EN** to a 0.01 µF capacitor located with-in 0.25 inches of the M66EN pin on the PCI connector (for designs with secondary PCIX bus slots only).	Sampled on the rising edge of PERST#.
A_PCIXCAP B_PCIXCAP	Connects directly to the PCIXCAP pin on the PCI slot. Connect to VCC33 through an 8.2KΩ pullup resistor.	• Design without secondary PCI/PCI-X Slot — If there is at least one legacy PCI device on the PCI/PCI-X bus, tie this pin directly to GND. — If all devices are PCI-X capable and there is at least one PCI-X device that only supports maximum PCI-X 66MHz on the secondary PCI bus, pull down to GND through 10KΩ series resistor parallel with a 0.01uF capacitor. — If all secondary PCI-X devices (and the bus loading) support PCI-X 133MHz, connect PCIXCAP to 3.3V through an 8.2K Ω resistor • Design with secondary PCI/PCI-X Slot — If there is at least one on board legacy PCI device on the secondary PCI bus, tie this pin directly to GND. — Else •Pull up to 3.3V through a 8.2KΩ resistor •Connect this pin to PCIXCAP (Pin B38) of the PCI connector. (Assuming bus loading supports up to PCI-X 133MHz)
IDSEL	The series resistor on IDSEL should be 200Ω ±5%.	

Table 21. Miscellaneous Signals

Signals	Recommendations	Reason/Impact
RSTIN#	Used for debug purposes. Connect to VCC33 through an 8.2KΩ pullup resistor for normal operation.	
A_STRAP0, A_STRAP1, A_STRAP2, A_STRAP6, B_STRAP0, B_STRAP1, B_STRAP2, B_STRAP6 RESERVED [8:1]	These signals REQUIRE external pull-downs to GND on the board 8.2KΩ unless otherwise stated.	
CFGRETRY	Input pin to configure 41210 to retry configuration accesses on it's PCI Express interface. • To retry configuration accesses to the 41210, pull high to 3.3V through a 2K Ω resistor. • To allow configuration accesses to the 41210, ground this pin through a 2K Ω resistor.	
A_TEST1, A_TEST2, B_TEST1, B_TEST2 A_PME#, B_PME#, A_STRAP[3], A_STRAP[4], A_STRAP[5], B_STRAP[3], B_STRAP[4], B_STRAP[5]	These signals REQUIRE an external pull-up, 8.2KΩ to 3.3V.	
NC17	This signal requires an external pull-up, 8.2KΩ to 3.3V.	In normal operating mode, this pin must be tied high.

Table 22. SMBus Interface Signals

Signal	Recommendations	Reason/Impact
SMBCLK	Connect to VCC33 through an 8.2KΩ pullup resistor.	
SMBDAT	Connect to VCC33 through an 8.2KΩ pullup resistor.	
SMBUS[5], SMBUS[3:1]	SMBus addressing: Bit 7----------'1' Bit 6----------'1' Bit 5----------SMBUS[5] Bit 4----------'0' Bit 3----------SMBUS[3] Bit 2----------SMBUS[2] Bit 1----------SMBUS[1] Use 8.2KΩ resistors as pullups to VCC33 for a '1' and as pulldowns to ground for a '0' to set the SMBus address.	Sampled on the rising edge of PERST#.

Table 23. Power and Ground Signals

Signal	Recommendations	Reason/Impact
RCOMP	100Ω ±1% (1/4 W) pulldown resistor to ground. The trace impedance of this signal should be < 0.1Ω.	Analog compensation pin for PCI. 0.75V nominal.
VCC15	Connect to 1.5V power supply. *Note*: Linear voltage regulators are recommended when using 1.5 Volt power supplies. Decoupling: 5 0.1uF caps beneath package (backside of board) 2 1.0 uF caps as close as design rules permit to package 3 10 uF caps as close as design rules permit to package	1.5V ±5% core voltage.
VCC33	Connect to 3.3V power supply. Decoupling: TBD The platform must insure that the VCC33 voltage rail be greater than to (or no less than 0.5V below) VCC15 (absolute voltage value at all times during 41210 Bridge operation, including during system power up, power down or any other time during system operation. This can be accomplished by placing a diode (with a voltage drop < 0.5V) between VCC15 and VCC33. Anode will be connected to VCC15 and cathode will be connected to VCC33.	3.3V ±5% PCI I/O voltage.
VCCAPE	Connect to 1.5V power supply.	1.5V ±3% Analog PCI Express voltage.
VCCAPCI[2:0]	See Figure 23 for circuit.	Analog PCI voltage pins.
VCCBGPE	Voltage output of the bandgap filter circuit into 41210 Bridge, separated from the rest of the VCC15s. See Figure 25 for circuit.	2.5V ±3% PCI Express voltage.
VCCPE	Connect to 1.5V power supply. Decoupling: 3 0.1uF caps beneath package (backside of board) 4 1.0 uF caps as close as design rules permit to package 2 10 uF caps as close as design rules permit to package	1.5V ±3% PCI Express voltage.
VSS	Connect to ground.	Ground reference for all supplies.
VSSAPE	See Figure 24 for circuit.	Analog ground for PCI Express.
VSSBGPE	Ground for the bandgap filter circuit, separated from the rest of the VSSs. See Figure 25 for circuit.	Ground for analog bandgap voltage.

Table 24. JTAG Signals

Signal	Recommendations	Reason/Impact
TCK	If not used for JTAG, leave as No Connect	Internal pull-up
TDI	If not used for JTAG, leave as No Connect	Internal pull-up
TDO	If not used for JTAG, leave as No Connect	Internal pull-up
TMS	If not used for JTAG, leave as No Connect	Internal pull-up
TRST#	Connect to ground via a 1KΩ pulldown resistor.	If TAP interface is not used this should be tied to ground.