WBX-6200F-V

VIA Eden/C3 Fanless Micro PC

User's Manual

Version 1.0



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Safety Precautions

Before getting started, read the following important cautions.

- 1. The WBX-6200F-V may not come equipped with an operating system. An operating system must be loaded first before installing any software into the computer.
- Be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and place all electronic components in any static-shielded devices. Most electronic components are sensitive to static electrical charge.
- 3. Disconnect the power from the WBX-6200F-V before making any installation. Be sure both the system and the external devices are turned OFF. Sudden surge of power could ruin sensitive components. Make sure the WBX-6200F-V is properly grounded.
- 4. Turn OFF the system power before cleaning. Clean the system using a cloth only. Do not spray any liquid cleaner directly onto the system.
- 5. The WBX-6200F-V is not susceptible to intense shock or vibration. When assembling the WBX-6200F-V, make sure it is securely installed.
- 6. If opening the cover for maintenance is a must, only a trained

technician is allowed to do so. Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

- ✓ Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This will help to discharge any static electricity on your body.
- ✓ When handling boards and components, wear a wrist-grounding strap, available from most electronic component stores.
- 7. Follow below instructions and notice the caution for replacing and disposing of the RTC Lithium battery CR2032 for safety consideration:

CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instruction.

Acknowledgments

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Table of Contents

How to Use This Manual	IX
Chapter 1 System Overview	1
Introduction	1
Features	1
System Specification	3
System View	4
I/O connectors 5	
Unpacking	6
Chapter 2 Getting Started	7
Setting Up the System	7
Installing System Software	8
Installing the Drivers	9
Chapter 3 BIOS Setup Information	10
Entering Setup	10
Entering Setup	
· ·	12
Main Menu	12 12
Main MenuStandard CMOS Setup Menu	12 12 13
Main MenuStandard CMOS Setup Menu	12 12 13
Main MenuStandard CMOS Setup MenuAdvanced CMOS SetupAdvanced CMOS Setup Menu	12 13 21
Main MenuStandard CMOS Setup Menu Advanced CMOS SetupAdvanced CMOS Setup MenuAdvanced Chipset Setup Menu	12 13 21 24
Main Menu	12 13 21 24 27
Main Menu Standard CMOS Setup Menu Advanced CMOS Setup Advanced CMOS Setup Menu Advanced Chipset Setup Menu Power Management Setup Menu PCI/Plug and Play Setup	12 13 21 24 27 30
Main Menu	12 13 21 24 27 30 31
Main Menu	1213212427303134

of CPU Board	43
Jumpers Location and list	43
Jumper List	44
Jumper Setting	44
Connector Definitions	46
Connectors Location	46
Appendix B. System Assembly Reference	66

How to Use This Manual

This manual is written for the system integrator, PC technician and knowledgeable PC end user. It describes how to configure your WBX-6200F-V series to meet various operating requirements. The user's manual is divided into four chapters, with each chapter addressing a basic concept and operation of the server board.

Chapter 1: System Overview - presents what you have inside the box and gives you an overview of the product specifications and basic system architecture for the WBX-6200F-V series Micro PC.

Chapter 2: System Installation - describes how to set up the system.

Chapter 3: BIOS Setup Information - specifies the meaning of each setup parameter, how to get advanced BIOS performance and update to a new BIOS. Additionally, the POST checkpoint list will give you a guide for troubleshooting.

The contents of this manual are subject to change without prior notice. These changes will be incorporated in new editions of this manual. I-Tech may make supplements or changes for the product described in this manual at any time.

System Overview

Introduction

WBX-6200F-V series are based-on the features of high performance, cost-effective for VIA C3 or Eden platform with low power consumption.

WBX-6200F-V is mainly designed for industrial automation with slim and true fanless feature. With GPIO connector for data collection and device control, and storage can support internal DOM and external Compact Flash memory card, or one 2.5" HDD.

Features

The WBX-6200F-V features:

■ CPU

VIA C3 1GHz, optional for Eden 300/400/533/667/733/800 MHz

■ System Memory

DDR SDRAM SO-DIMM 256 MB system memory, up to 1GB

■ Mass Storage Device

Internal 2.5" HDD drive bay with optional anti-vibration kit

■ IDE interface

UDMA 133 IDE interface x 1 (40 pins) / DMA 33 IDE interface x 1 (44 pins)

■ PCMCIA interface

One PCI card-bus interface for Complies with PC Card

95/97/98, Card-32(32 bit), PCMCIA V2.1/JEIDA 4.2(16 bit), supports type I/II

■ CF interface

1 x bootable Compact Flash slot for CF type I/II storages via IDE/CF adaptor

(PCMCIA and CF cannot be used simultaneously)

■ Mini-PCI interface

1 x 32-bit Mini-PCI socket (support 802.11b/g and DVB modules)

Audio Function

Dual full-duplex Direct Sound channel between system memory and AC97 link, standard AC97 codec interface with Line-in, Line-out and Microphone-in ports

■ Ethernet Function

supports 10/100 Base-T with external RJ-45 connector (without LED), WOL/PXE function

BIOS

AMI BIOS, 4 MB Flash EEPROM, Plug-and-Play compatible

■ Watchdog Function

1~255 minutes, software programmable

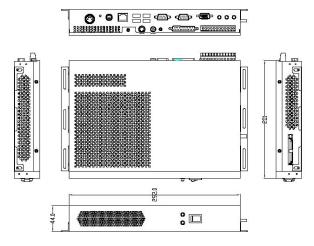
System Specification

NOTE: Specifications are subject to change without notice.

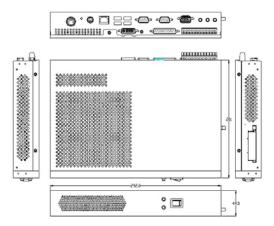
Parts		Specifications	
System	CPU	VIA Eden 733MHz / C3 1GHz	
Board	System memory	One DDR SO-DIMM socket, support up to 1GB	
	I/O	- VGA port x 1 / DVI x 1	
	interfaces	- Serial port (RS-232 x 1, RS-232 /422/485 x 1)	
		- Parallel port x 1 - PS/2 keyboard/mouse port	
		- GPIO: 4-bit input, 4-bit output	
		- LAN RJ-45 x 1	
USB and Audi	io	Four USB 2.0 ports	
		Microphone input connector Line input connector Line output connector	
Storage device	Hard disk drive	2.5" HDD drive bay	
AC-to-DC Power	Output power	Max. 80 Watt	
Adapter	Input voltage	AC90 ~ 264V / 47 ~ 63 Hz, 1.9A	
	Output voltage	DC12V ~ 24V @6.66A	
Dimension		292 × 201 × 44 mm (L x W x H)	
Weight		2.6 Kg	
Environment	Temperature	Operating: 0 °C ~ 40 °C Storage: -20 °C ~ 60 °C	
	Humidity	10% ~ 90% @ RH, non-condensing	

System View Outline Drawing

CF interface:

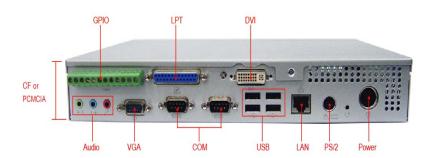


PCMCIA interface:



I/O connectors





Unpacking

After unpacking the shipping carton, you should find these standard items:

- The WBX-6200F-V Micro PC
- Accessory box including the followings:
 - AC adapter x 1
 - AC power cord x 1
 - 44-pin 2.0mm pitch IDE cable x 1
 - Y cable for PS2 keyboard and mouse x 1
 - Mounting bracket x 2, screw x 8
 - CD-ROM for drivers, utility, and user manual
 - Quick installation Guide

Inspect all the items. If any item is damaged or missing, notify your dealer immediately.

Getting Started

This chapter tells you how to set up the system.

Setting Up the System

The following is a summary of the steps in setting up the system for use.

CAUTION: Make sure that power to the system and each of the devices to be connected is switched OFF before plugging in the connectors.

- 1. Make any required external connections such as the keyboard, and mouse.
- 2. Plug the appropriate end of the power cord into the power connector of the system. Then plug the other end of the power cord to an electrical outlet.
- 3. Press the power switch of the system to turn on the system's power.
- 4. If necessary, run the BIOS SETUP program to configure the system (see Chapter 3).
- 5. Install the software drivers if necessary.

Installing System Software

Recent releases of operating systems from major vendors include setup programs, which load automatically and guide you through hard disk preparation and operating system installation. The guidelines below will help you determine the steps necessary to install your operating system on the Micro PC hard drive.

NOTE: Some distributors and system integrators

may have already pre-installed system software prior to shipment of your Micro PC.

Installing software requires an installed HDD. Software can be loaded in the WBX-6200F-V using any of below methods:

1. Method 1: Use the Ethernet

You can use the Ethernet port to download software from the Net to the HDD that has been pre-installed in WBX-6200F-V.

2. Method 2: Use the COM or Parallel Port

By connecting another PC to the WBX-6200F-V with an appropriate cable, you can use transmission software to transmit Operation System Software to the HDD that has been pre-installed in the WBX-6200F-V.

3. Method 3: Use a External CD-ROM

You can use the external CD-ROM to transmit the software to the HDD that has been pre-installed in the WBX-6200F-V.

Installing the Drivers

After installing your system software, you will be able to set up the LAN, VGA, Audio and USB functions. All drivers are stored in a CD disc, which can be found in your accessory pack.

The various drivers and utilities in the disc have their own text files that help users install the drivers and understand their functions.

BIOS Setup Information

WBX-6200F-V is equipped with the AMI BIOS stored in Flash ROM. This BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, WBX-6200F-V communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start-up.

Entering Setup

Turn on or reboot the computer. When the message "Hit if you want to run SETUP" appears, press key immediately to enter BIOS setup program.

If the message disappears before you respond, but you still wish to enter Setup, please restart the system to try "COLD START" again by turning it OFF and then ON, or touch the "RESET" button. You may also restart from "WARM START" by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to,

Press <F1> to Run SETUP or Resume

In HIFLEX BIOS setup, you can use the keyboard to choose among options or modify the system parameters to match the options with your system. The table below will show you all of keystroke functions in BIOS setup.

Keys to navigate within setup menu

Key	Functions
Up Arrow	Move to the previous item
Down Arrow	Move to the next item
Left Arrow	Move to the item on the left (menu bar)
Right Arrow	Move to the item on the right (menu bar)
Move Enter	Move to the item you desired
PageUp key	Increase the numeric value or make changes
PageDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
Esc key	Main Menu Quit and not save changes into CMOS Status Page Setup Menu and Option Page
	Setup Menu Exit current page and return to
E4 1	Main Menu
F1 key	General help on Setup navigation keys
F10 key	Save all the CMOS changes and exit

Main Menu

Once you enter WBX-6200F-V AMI BIOS CMOS Setup Utility, you should start with the Main Menu. The Main Menu allows you to select from eleven setup functions and two exit choices. Use arrow keys to switch among items and press <Enter> key to accept or bring up the sub-menu.

NOTE: It is strongly recommended to reload Optimal Setting if CMOS is lost or BIOS is updated.

Standard CMOS Setup Menu

This setup page includes all the items in standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PageUp>/<PageDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change Date, Time, Drive type, and Boot Sector Virus Protection Status.

■ Menu selections

Item	Options	Description
Date		Set the system date. Note that the 'Day' automatically changes when you set the date
Time	Hh: mm: ss	Set the system time

	1	1
Drive A	Non Installed	Select the type of floppy disk
Drive B	360KB, 5 1/4	drive installed in your system
	1.2MB, 5 1/4	
	720KB, 3 1/2	
	1.44MB, 3 1/2	
Pri Master	Select a suitable	Press <pageup> or</pageup>
	item or keep it in	<pagedn> to select a</pagedn>
	Auto for automatic	suitable item
	detection.	
Pri Slave	Select a suitable	Press <pageup> or</pageup>
	item or keep it in	<pagedn> to select a</pagedn>
	Auto for automatic	suitable item
	detection.	
Sec Master	Select a suitable	Press <pageup> or</pageup>
	item or keep it in	<pagedn> to select a</pagedn>
	Auto for automatic	suitable item
	detection.	
Sec Slave	Select a suitable	Press <pageup> or</pageup>
	item or keep it in	<pagedn> to select a</pagedn>
	Auto for automatic	suitable item
	detection.	

Advanced CMOS Setup

This setup reference table includes all the Optimal, Failsafe, and Other options setting in each BIOS setup item. It is very easy to cross reference. If you want to go details, you can directly refer to item description in sub-section.

■ ADVANCED CMOS SETUP DEFAULTS

BIOS Setup Items	Optimal	Failsafe	Other Options
	Default	Default	
Quick Boot	Enabled	Disabled	
1st Boot Device	IDE-0	IDE-0	Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy, ARMD-FDD, ARMD-HDD, CD/DVD-0, CD/DVD-1, CD/DVD-2, CD/DCD-3, Legacy SCSI, Legacy NETWO, BBS-0, BBS-1, BBS-2, BBS-3, BBS-4, BBS-5, BBS-6, BBS-7, BBS-8, BBS-9, USB FDD, USB CDROM, USB RMD-FDD, USB RMD-FDD, USB RMD-HDD
2nd Boot Device	CD/DVD-0	CD/DVD-0	
3rd Boot Device	Disabled	Disabled	
Try Other Boot Device	Yes	Yes	No
S.M.A.R.T. for Hard Disks	Disabled	Disabled	Enabled
Boot Up Num-Lock	On	On	Off
PS/2 Mouse Support	Enabled	Enabled	Disabled
System Keyboard	Absent	Absent	Present
Primary Display	Absent	Absent	VGA/EGA,,Mono
Password Check	Setup	Setup	Always
Boot To OS/2	No	No	Yes
L1 Cache	Enabled	Enabled	Disabled
L2 Cache	Enabled	Disabled	
System BIOS Cacheable		Disabled	

C000, 32K Shadow	Cached	Cached	Enabled, Disabled
C800, 16K Shadow	Disabled	Disabled	Enabled, Disabled
CC00, 16K Shadow	Disabled	Disabled	Enabled, Disabled
D000, 16K Shadow	Disabled	Disabled	Cached, Enabled
D400, 16K Shadow	Disabled	Disabled	Cached, Enabled
D800, 16K Shadow	Disabled	Disabled	Cached, Enabled
DC00, 16K Shadow	Disabled	Disabled	Cached, Enabled

■ ADVANCED CHIPSET SETUP

BIOS Setup	Optimal	Failsafe	Other Options
Items	Default	Default	
Configure SDRAM	Enabled	Disabled	Enabled
Timing by SPD			
SDRAM Frequency	Auto	Auto	200Mhz, 266Mhz
SDRAM CAS#	2.5	2.5	2
Latency			
SDRAM Bank	Disabled	Disabled	2-way, 4-way
Interleave			
SDRAM Command	2T	2T	1T
Rate			
Memory Hole	Disabled	Disabled	512KB-640KB,
			15MB-16MB,
			14MB-16MB
AGP Aperture Size	64MB	64MB	4,8,16,32,128,256MB
USB Controller	All USB	Disabled	2 USB Ports,
	Ports		4 USB Ports.
USB Device Legacy	All Device	Disabled	No mice,
Support			All Device
Spread Spectrum	Normal	Normal	Test Mode,
Control			Three Stated,
			-0.5%, +/-0.5%,
			+/-0.25%, +/-0.38%
HDD UDMA Mode	Normal	Normal	Force Mode 2
Control			
WDT Timer Control	Disabled	Disabled	1 Minute,
			2 Minute,
			4 Minute,
			8 Minute,
			16 Minute,
			32 Minute,
			255 Minute,

▮ POWER MANAGEMENT SETUP DEFAULTS

BIOS Setup Items	Optimal	Failsafe	Other
	Default	Default	Options
ACPI Aware O/S	Yes	Yes	No
ACPI Standby State	S1/POS	S1/POS	Auto, S3/STR
USB Device Wakeup	Disabled	Disabled	
Function			
Power Management/ APM	Enabled	Disabled	
Video Power Down Mode	Disabled	Disabled	Stand By, Suspend
Hard Disk Power Down	Disabled	Disabled	Stand By,
Mode	Disabled	Disabled	Suspend
Standby Time Out	Disabled	Disabled	1, 2, 4, 8,
(Minute)	Disabled	Disablea	10, 20, 30,
(Will late)			40, 50, 60.
Suspend Time Out	Disabled	Disabled	1, 2, 4, 8,
(Minute)	Bisabisa	Disabioa	10, 20, 30,
(40, 50, 60.
Throttle Slow Clock	50 %-56.25%	50 %-56.25%	
Ratio	00 70 00.2070	00 70 00.2070	6.25%-12.5%,
			18.75%-25%,
			31.25%- 37.5%,
			37.5%-43.75%
			43.75%-50%
			56.25%-62.5%
			62.5%-68.75%
			68.75%-75%
			75%-87.5%
			75%-81.25%
			81.25%-87.5%
			87.5%-93.75%
			93.75%-100%
Display Activity	Ignore	Ignore	Monitor
IRQ3	Monitor	Ignore	Ignore
IRQ4	Monitor	Ignore	Ignore
IRQ5	Ignore	Ignore	Monitor
IRQ7	Monitor	Ignore	Ignore
IRQ9	Ignore	Ignore	Monitor
IRQ10	Ignore	Ignore	Monitor

IRQ11	Ignore	Ignore	Monitor
IRQ13	Ignore	Ignore	Monitor
IRQ14	Monitor	Ignore	Ignore
IRQ15	Ignore	Ignore	Monitor
Power Button Function	On/Off	On/Off	Suspend
Restore on AC/Power	Power Off	Power Off	Power On Last
			State
Resume On RTC Alarm	Disabled	Disabled	Enabled
RTC Alarm Date	15	15	Everyday,
			01-31
RTC Alarm Hour	12	12	00-23
RTC Alarm Minute	30	30	00-59
RTC Alarm Second	30	30	00-59

PCI / PLUG AND PLAY SETUP

BIOS Setup	Optimal Default	Failsafe Default	Other Options
Plug and Play Aware O/S	No	No	Yes
Clear NVRAM	No	No	Yes
On Chip VGA Frame Buffer Size	16MB	16MB	None, 8, 32MB
PCI Latency Timer (PCI Clocks)	32	32	64, 96, 128, 160, 192, 224, 248
Boot Device Select	CRT	CRT	LCD, CRT+LCD, TV CRT+TV DVI DVI+CRT
TV Type	NTSC	NTSC	PAL, PALM, PALN, PALNc,
TV Output Connector	Composite	Composite	S-Video0, R/G/B, Cr/Y/Cb, SDTV-R/G/B, SDTV-Pr/Y/Pb, S-Video1
Allocate IRQ to PCI VGA	Yes	No	

■ PERIPHERAL SETUP DEFAULTS

BIOS Setup Items	Optimal	Failsafe	Other
•	Default	Default	Options
On Board Serial Port1	3F8/COM1	3F8/COM1	Auto, Disabled, 2F8/COM2, 3E8/COM3, 2E8/COM4
On Board Serial Port2	2F8/COM2	2F8/COM2	Auto, Disabled, 3F8/COM1, 3E8/COM3, 2E8/COM4
On Board FIR Port	Disabled	Disabled	Enabled
FIR IRQ Select	11	11	3, 4, 10
FIR DMA1 Select	6	6	5, 7
On Board Parallel Port	378	378	Auto, Disabled, 278, 3BC
Parallel Port Mode	Normal	Normal	Bi-Dir, ECP, EPP, EPP+ECP
EPP Version	N/A	N/A	
Parallel Port DMA Channel	N/A	N/A	
Parallel Port IRQ	7	7	5
On Board IDE	Both	Both	Disabled, Primary, Secondary
On Board LAN	Enabled	Disabled	
On Board LAN P.M.E	Enabled	Disabled	
Onboard AC' 97 Audio	Enabled	Enabled	Disabled

HARDWARE MONITOR SETUP DEFAULTS

BIOS Setup Items	Optimal Default	Failsafe Default	Other Options
CPU Temperature		===	
CPU Fan Speed		===	
System Fan Speed		===	
Vcore		===	
Vtt		===	
+ 3.300V		===	
+ 5.000V		===	
+ 12.000V		===	·

Standard CMOS Setup Menu

This setup page includes all the items in standard compatible BIOS. Use the arrow keys to highlight the item and then use the <PageUp>/<PageDn> or <+>/<-> keys to select the value or number you want in each item and press <Enter> key to certify it.

Follow command keys in CMOS Setup table to change Date, Time, Drive type, and Boot Sector Virus Protection Status.

Advanced CMOS Setup Menu

This setup includes all of the advanced features in the system. The detail descriptions are specified as below.

Quick Boot

Set "Disabled" for normal booting or select "Enabled" to skip minor BIOS test items to obtain quick boot response.

1st Boot Device / 2nd Boot Device / 3rd Boot Device

These fields set the type of device for the first boot drive that the AMIBIOS attempts to boot from after AMIBIOS POST is completed. If it fails to boot from the first boot drive, it will attempt to boot from the second, then third boot drive as specified in the corresponding field.

Options are: Disabled, IDE-0, IDE-1, IDE-2, IDE-3, Floppy,
ARMD-FDD, ARMD-HDD, CD/DVD-0, CD/DVD-1, CD/DVD-2,
CD/DCD-3, Legacy SCSI, Legacy NETWO, BBS-0, BBS-1,
BBS-2, BBS-3, BBS-4, BBS-5, BBS-6, BBS-7, BBS-8, BBS-9,
USB FDD, USB CDROM, USB HDD, USB RMD-FDD, USB
RMD-HDD

Try Other Boot Device

Select "Yes" to enable trying to boot from different devices in sequence. Selected "No" for booting only from the first boot device.

S.M.A.R.T for Hard Disks

Set this option to Enabled to permit the BIOS to use the SMART(System Management and Reporting Technologies) protocol for reporting server system information over a network. Enabling this feature allows you to back up your data when your hard disk is about to fail.

Boot Up Num-Lock

Select "On" to enable numeric function of the numeric keypad, or "Off" to disregard it.

PS/2 Mouse Support

Select "Enabled" to enable PS/2 mouse function, or "Disabled" to release IRQ12 interrupt for other ISA-bus I/O devices.

System Keyboard

This option will be used to neglect "keyboard error" while you choose *Absent* setting in your BIOS setup and system has no keyboard attached.

Primary Display

Chooses *Absent*, *VGA/EGA*, *CGA40x25*, *CGA80x25*, or *Mono* to meet your monitor type. If you select *Absent*, the "CMOS Display Type Wrong" message will be ignored regardless the mismatched display card.

Password Check

This option enables the password checking when the system boots up or runs CMOS Setup. It only takes effect after setting Change Supervisor Password.

Setup: This option will force system to check password before running Setup if you have already entered the current user password in "Change User Password". By that time, the system will be only able to boot but deny accessing Setup.

Always: Password prompt appears every boot-up. The system will not boot and deny access Setup with invalid password. The best way is to clear CMOS or try to reload BIOS Setup to boot up system.

Boot To OS/2

You should set this option to "Yes" to support OS/2 environment.

L1 Cache

This option controls to turn on or off the CPU's Level 1 built-in cache.

L2 Cache

Enables this option to turn on or off the CPU's Level 2 built-in cache.

System BIOS Cacheable

Enables this option to enhance system performance by shadowing and caching system BIOS. When disabled, this BIOS shadow function will be ignored.

Shadow Memory

Each of segments provides three options "Disabled", "Enabled", and "Cached" for faster adapter's ROM execution. However this shadow function is Chipset oriented and dependent on system hardware feature. In general, C000 64k will be allocated for VGA BIOS and set to *Cached* to get higher display performance by shadowing and caching feature. If user chooses *Enabled* setting, only BIOS shadow function is active.

Advanced Chipset Setup Menu

This setup is very important to keep system stability. If you are not technical person, do not attempt to change any parameters. The best way is to choose optimal default setting.

Configure SDRAM Timing by SPD

This option provides DIMM plug-and-play support by Serial Presence Detect (SPD) mechanism via the System Management Bus (SMBus) interface. You can disable this option to manage the following four SDRAM timing options by yourself. In addition, SDRAM operating timings may follow

serial presence from EEPROM content by setting this option to "Enabled", and all of SDRAM timing options will be not available and hidden.

SDRAM Frequency

PC-100 means the memory bus is running at 100MHz. PC-200 means its bus is running at 200MHz.

SDRAM CAS# Latency

This option controls the number of SCLKs between the time a read command is sampled by the SDRAMs and the time the North Bridge, 8601A, samples correspondent data from the SDRAMs.

SDRAM Bank Interleave

This option is SDRAM by interleave or consecutive mode.

SDRAM Command Rate

This option controls how long the memory controller latches on and asserts the command bus. The lower the value, the faster the the memory controller can send commands out. However, not many SDRAM modules can run with a command rate of only 1T. Failure to do so will result in data corruption and, of course, a system crash.

Memory Hole

This option allows the end user to specify the location of a memory hole for memory space requirement from ISA-bus cards.

AGP Aperture Size

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space.

Host cycles that hit the aperture range are forwarded to the AGP without any translation, usually set as 64MB.

USB Controller

This option will enable / disable on-chip USB function

USB Device Legacy Support

This feature will be automatically disabled and hidden if user chooses the "Disabled" setting from the foregoing USB Function option. Otherwise, enabling this option provides support for USB-keyboard without auxiliary driver under DOS environment.

Spread Spectrum

This option is for EMI test only.

HDD UDMA Mode Control

This Options specifies HDD UltraDMA mode.

Options are: Normal, Force Mode2.

WDT Timer Control

This option specifies the length of the period of the watchdog timer (WDT).

Power Management Setup Menu

This APM (Advanced Power Management) determines how much power energy can be saved by setting below items to handle system power resource. The following descriptions will specify the definition of each item in details.

ACPI Aware O/S

This option allows you to enable / disable the ACIP Power management function.

ACPI Standby State

This option allows you to select the ACPI Suspend type. You can select the optional S3/STR for suspending to DRAM only if your system supports this mode. Or yo can select S1/POS for Power on Suspend under Windows 98 or later O/S ACPI mode.

USB Device Wakeup Function

If ACPI Standby state is set to S3/STR, use this item to enable / disable the USB device wakeup function.

Power Management/APM

This option allows you to enable / disable the Power Management / Advanced Power Management Function.

Video Power Down Mode

This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity has expired.

Hard Disk Power Down Mode

This option specifies the power management state that the HDD enters after the specified period of hard drive inactivity

has expired. It is the same as video power control. If user chooses "Stand By" or "Suspend", it will depend on period of parameter "Stand By Time out" or "Suspend Time out".

Standby Time out (Minute)

This option specifies the length of the period of system inactivity while the computer is in Full-On power state before the computer is placed in Standby mode. When this length of time expires, the computer enters Standby Timeout state. In Standby mode, some power use is curtailed.

Suspend Time out (Minute)

This option is the same as Stand by Time out function. These two features will be enabled to monitor power of sub-items "Display Activity", "Serial port", "Parallel Port", "Floppy", "Pri-HDD", and "Sec-HDD" independently. It is also used to control CPU throttle running function. All of sub-items will be ineffective in selection of disabling "Stand by Time out" or "Suspend Time out" even if it can be choose by user in BIOS setup menu.

Throttle Slow Clock Ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as duty cycle of the STPCLK# signal. This duty cycle indicates the percentage of time the STPCLK# signal is asserted while in the throttle mode.

Display Activity

This option specifies if BIOS is to monitor activity on the display monitor for power conservation purposes. If set to Monitor and the computer is in a power saving state, BIOS

watches for video display activity. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ lines. If set to Ignore, video display monitor activity is not monitored.

IRQ Active

When set to Monitor, these options enable event monitoring on the specified IRQ. If set to Monitor and the computer is in a power saving state, BIOS watches for activity on the device with specified IRQ line. The computer enters the full on power state if any activity occurs. BIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ. No monitoring activity occurs if the option is set to Ignore. The settings for each of these options are Monitor or Ignore.

Power Button Function

The option is select power button function of ON/OFF or suspend.

Restore On AC/Power Loss

Allows you to set the restore state from AC/Power loss.

Resume On RTC Alarm

This option allows you to enable disable the Resume On RTC Alarm function.

RTC Alarm Date / Hour/ Minute / Second

If resume On RTC is enabled, this option allows you to set the Alarm date, hour, minute and second.

Date Choices: Everyday, 01-31

Hour choices: 00-23

Minute choices: 00-59 Second choices: 00-59

PCI/Plug and Play Setup

This section describes configuring the PCI bus system. PCI (Peripheral Component Interconnect) is a system which allows I/O devices to operate at speeds nearing CPU's when they communicate with own special components.

All of options described in this section are important and technical and it is strongly recommended that only experienced users could make any changes to the default settings.

Plug and Play Aware O/S

Set this option to "Yes" if the operating system installed in the computer is Plug and Play-aware. BIOS only detects and enables PnP ISA adapter cards that are required for system boot. The Windows 95 operating system detects and enables all other PnP-aware adapter cards. Windows 95 is PnP-aware. Set this option to "No" if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

Clear NVRAM

This option is used to clear NVRAM and check or update ESCD (Extended System Configuration Data) data after system power on. Set this option to No that will not clear NVRAM and the operation of update ESCD is effective in different ESCD

data comparison. If you select the "Yes" setting, then the BIOS will update ESCD each time of power on.

On Chip VGA Frame Buffer Size

Options are: None, 8MB, 16Mb, 32MB.

PCI Latency Timer (PCI Clocks)

This option is used to control PCI latency timer period (follow PCI clocks). Based on PCI specification 2.1 or later and PCI bus frequency in system, user can select different timer to meet their PCI bus environment.

Boot Device Select

This option specifies the type of display being used with the system.

Options are: LCD, CRT+LCD, TV, CRT+TV, DVI, DVI+CRT.

TV Type

Options are: NTSC, Pal, PALM, PALN, PALNc.

TV Output Connector

Options are: Composite, S-Video0, R/G/B, Cr/Y/Cb, SDTV-R/G/B, SDTV-Pr/Y/Pb, S-Video1.

Allocate IRQ to PCI VGA

This option will be used to allocate IRQ for PCI VGA card. In general, some of PCI VGA cards need IRQ support.

Peripheral Setup

This section describes I/O resources assignment for all of on-board peripheral devices.

On Board Serial Port 1/Port 2

These fields control the resource assignments of two on-board serial interfaces SIO1 and SIO2. The following lists show current options in On Board Serial Port 1/ Port 2:

Auto → cannot set serial I/O resources by manual operation
 Disabled → indicates on-board COM port function is ineffective

3F8h/COM1 → assign I/O address 3F8h to COM1

2F8h/COM2 → assign I/O address 2F8h to COM2

3E8h/COM3 → assign I/O address 3E8h to COM3

2E8h/COM4 → assign I/O address 2E8h to COM4

On Board FIR Port

This option allows you to enable / disable the onboard Fast Infrared(FIR) interface

FIR IRQ Select

This option is only valid if the **Onboard FIR Port** option is set to *Enabled*. This option sets the IRQ used by the FIR port.

FIR DMA1 Select

This option is only valid if the **Onboard FIR Port** option is set to *Enabled*. This option sets the DMA1 channel used by the FIR port

On Board Parallel Port

There are four optional items Parallel Port Mode, EPP Version, Parallel Port IRQ, and Parallel Port DMA Channel used to control on-board parallel port interface while user select I/O base address manually. The following lists are available options of on-board parallel port:

Auto → user can not control all of LPT port I/O resources

Disabled → on-board parallel port function is ineffective and N/A

378h → locate IRQ7 for this default I/O address

278h → assign this I/O address to LPT1

3BCh → assign this I/O address to LPT1

Parallel Port Mode:

This option specifies the parallel port mode. ECP and EPP are both bi-directional data transfer schemes that adhere to the IEEE P1284 specifications. This Parallel Port Mode includes four options "Normal", "Bi-Dir", "EPP", and "ECP".

Setting	Description		
Normal	Uni-direction operation at normal speed		
Bi-Dir	Bi-direction operation at normal speed		
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bi-directional data transfer driven by the host device.		
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve data transfer rates up to 2.5 Megabits per second. ECP provides symmetric bi-directional communication.		

© EPP Version :

This option is only valid if the Parallel Port Mode option is set to EPP. This option specifies the version of the Enhanced Parallel Port specification that will be used by AMIBIOS.

Parallel Port DMA Channel :

This option is only available if **On Board Parallel Port** is set to fixed I/O address and the setting of **Parallel Port Mode** is ECP. This option sets the DMA channel used by ECP-capable parallel port.

Parallel Port IRQ:

This option is only valid if the **Onboard Parallel Port** option is not set to *Disabled*. This option sets the IRQ used by the parallel port.

On Board IDE

This option specifies the onboard IDE controller channels that will be used. The settings are *Disabled*, *Primary*, *Secondary*, or *Both*.

On Board LAN

This option allows you to enable / disable the onboard LAN controller.

On Board LAN P.M.E

This option allows you to enable / disable the onboard LAN PME signal (for LAN wake-up) function.

On Board AC'97 Audio

This option allows you to enable / disable the onboard AC'97 Audio function.

Hardware Monitor Setup

This setup describes current system status detected from hardware monitor controller. The status showed on screen will include:

- There are two on-board temperature sensors, TSENS1, and TSENS2.
- Current System Temperature (Generally indicates the inside temperature of chassis or surface temperature of SBC)
- Current Fan Speed

System operating voltage includes "CPU Vcore",
 "+3.300V", "+5.000V", "+12.000V".

BIOS POST Check Point List

AMIBIOS provides all IBM standard Power On Self Test (POST) routines as well as enhanced AMIBIOS POST routines. The POST routines support CPU internal diagnostics. The POST checkpoint codes are accessible via the Manufacturing Test Port (I/O port 80h). Whenever a recoverable error occurs during the POST, the system BIOS will display an error message describing the message and explaining the problem in detail so that the problem can be corrected.

During the POST, the BIOS signals a checkpoint by issuing one code to I/O address 80H. This code can be used to establish how far the BIOS has executed through the power-on sequence and what test is currently being performed. This is done to help troubleshoot faulty system board.

If the BIOS detect a terminal error condition, it will halt the POST process and attempt to display the checkpoint code written to port 80H. If the system hangs before the BIOS detects the terminal error, the value at port 80H will be the last test performed. In this case, the terminal error cannot be displayed on the screen. The following POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 07/15/95 version 6.27 (Enhanced).

Uncompressed Initialization Codes — The uncompressed initialization checkpoint hex codes are listed in order of execution:

Code	Description	
DO	NMI is disabled. CPU ID saved. INIT code checksum verification	
D0	will be started.	

D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and going to 4GB flat mode.	
D3	To start memory sizing.	
D4	Returning to real mode. Executing any OEM patches and setting the stack next.	
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The INIT code is copied to segment 0 and control will be transferred to segment 0.	
D6	Control is in segment 0. Next, checking if <ctrl><home> was pressed and verifying the system BIOS checksum. If either <ctrl><home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.</home></ctrl></home></ctrl>	
D7	To pass control to interface module.	
D8	Main BIOS runtime code is to be decompressed.	
D9	Passing control to the main system BIOS in shadow RAM next.	

Bootblock Recovery Codes — The bootblock recovery checkpoint hex codes are listed in order of execution:

Code	Description	
	The onboard floppy controller if available is initialized. Next,	
EO	beginning the	
	base 512KB memory test.	
E1	Initializing the interrupt vector table next.	
E2	Initializing the DMA and Interrupt controllers next.	
Code	Description	
E6	Enabling the floppy drive controller and Timer IRQs. Enabling	
EO	internal cache memory.	
ED	Initializing the floppy drive.	
EE	Start looking for a diskette in drive A: and read first sector of the	
	diskette.	
EF	A read error occurred while reading the floppy drive in drive A: .	
FO	Next, searching for the AMIBOOT.ROM file in the root directory.	
F1	The AMIBOOT ROM file is not in the root directory.	
F2	Next, reading and analyzing the floppy diskette FAT to find the	
ΓZ	clusters occupied by the AMIBOOT.ROM file.	
F3	Start reading AMIBOOT.ROM file, cluster by cluster.	
F4	The AMIBOOT.ROM file is not the correct size.	
F5	Next, disabling internal cache memory.	
FB	Next, detecting the type of Flash ROM.	
FC	Erasing the Flash ROM.	
FD	Programming the Flash ROM	

Flash ROM programming was successful. Next, restarting the system BIOS.
system BIOS.

Uncompressed Initialization Codes — The following runtime checkpoint hex codes are listed in order of execution. These codes are uncompressed in F0000h shadow RAM.

Code	Description		
03	The NMI is disabled. Next, checking for a soft reset or a power on		
condition.			
05	The BIOS stack has been built. Next, disabling cache memory.		
06	Uncompressing the POST code next.		
07	Next, initializing the CPU and the CPU data area.		
80	The CMOS checksum calculation is done next.		
ОВ	Next, performing any required initialization before the keyboar BAT command is issued.		
OC	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.		
OE	The keyboard controller BAT command result has been verified Next, performing any necessary INIT after the K/B controller BAT command test.		
OF	The keyboard command byte is written next.		
	Next, issuing the pin 23 and 24 blocking and unblocking		
10	commands.		
Code	Description		
11	Next, checking if the <end> or <ins> keys were pressed during power on.</ins></end>		
12	To initialize CMOS if the <i>initialize CMOS RAM in every boot</i> is set or the <end> key is pressed. Going to disable DMA and Interrupt controllers.</end>		
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.		
14	The 8254 timer test will begin next.		
19	The 8254 timer test is over. Starting the memory refresh test next.		
1A	The memory refresh line is toggling. Checking the 15us on/off time next.		
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.		
24	The configuration or setup required before interrupt vector initialization has completed. Interrupt vector init. is about to begin		

	Interrupt vector initialization is done. Clearing the password if	
25	the POST	
	DIAG switch is on.	
27	Any initialization before setting video mode to be done.	
28	Going for monochrome mode and color mode setting.	
	Bus initialization system, static, output devices will be done	
2A	next, if present.	
	Passing control to the video ROM to perform any required	
2B	configuration before the video ROM test.	
2C	To look for optional video ROM and give control.	
20	The video ROM has returned control to BIOS POST. Performing	
2D	any required processing after the video ROM had control.	
	Completed post-video ROM test processing. If the EGA/VGA	
ar.		
2E	controller is not found, performing the display memory	
	read/write test next.	
2F	EGA/VGA not found. Display memory R/W test about to begin.	
30	Display memory R/W test passed. Look for retrace checking	
	next.	
31	Display memory R/W test or retrace checking failed. To do	
	alternate display retrace checking.	
32	Alternate display memory R/W test passed. To look for the	
32	alternate display retrace checking.	
34	Video display checking is over. Setting the display mode next.	
34 37		
	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description	
37 Code	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description	
37	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next.	
37 Code	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present.	
37 Code 38 39	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message.	
37 Code 38	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying	
37 Code 38 39	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit message next.	
37 Code 38 39 3A 40	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next.	
37 Code 38 39 3A 40 42	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next.	
37 Code 38 39 3A 40	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics	
37 Code 38 39 3A 40 42 43	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next.	
37 Code 38 39 3A 40 42	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing	
37 Code 38 39 3A 40 42 43	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.	
37 Code 38 39 3A 40 42 43	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and	
37 Code 38 39 3A 40 42 43	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.	
37 Code 38 39 3A 40 42 43	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next. The memory wraparound test has completed. The memory size	
37 Code 38 39 3A 40 42 43 44	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next. The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next.	
37 Code 38 39 3A 40 42 43 44	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next. The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next. The memory pattern has been written to extended memory.	
37 Code 38 39 3A 40 42 43 44 45 46	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next. The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory. Writing patterns to the base 640 KB memory test.	
37 Code 38 39 3A 40 42 43 44 45 46	Video display checking is over. Setting the display mode next. The display mode is set. Displaying the power on message next. Description Initializing the bus input, IPL, and general devices next, if present. Displaying bus initialization error message. The new cursor position has been read and saved. Displaying the Hit < DEL > message next. Preparing the descriptor tables next. Entering protected mode for the memory test next. Entered protected mode. Enabling interrupts for diagnostics mode next. Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next. Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next. The memory wraparound test has completed. The memory size calculation has been done. Writing patterns to test memory next. The memory pattern has been written to extended memory.	

	1MP poyt		
40	1MB next.		
49	The amount of memory below 1MB has been found and verified.		
45	Determining the amount of memory above 1MB memory next.		
4B	The amount of memory above 1MB has been found and verified.		
	Checking for a soft reset and clearing the memory below 1MB for		
	the soft reset next.		
_	If this is a power on situation, going to checkpoint 4Eh next.		
4C	The memory below 1MB has been cleared via a soft reset.		
	Clearing the memory above 1MB next.		
4D	The memory above 1MB has been cleared via soft reset. Savi		
	the memory size next. Going to checkpoint 52h next.		
4E	The memory test started, but not as the result of a soft reset.		
	Displaying the first 64KB memory size next.		
4F	Memory size display started. This will be updated during		
	memory test.		
	Performing the sequential and random memory test next.		
50	Memory testing/initialization below 1MB completed. Going to		
	adjust displayed memory size for relocation and shadowing.		
51	The memory size display was adjusted for relocation and		
	shadowing.		
	Testing the memory above 1MB next.		
52	The memory above 1MB has been tested and initialized. Saving		
	the memory size information next.		
53	The memory size information and the CPU registers are saved.		
ပိ			
	Entering real mode next.		
Code	Entering real mode next. Description		
	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the		
Code 54	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.		
Code	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled.		
Code 54	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and		
Code 54 57	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.		
Code 54	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing.		
Code 54 57	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the		
Code 54 57 58	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing.		
Code 54 57	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the		
Code 54 57 58	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit < DEL > message next. The Hit < DEL > message is cleared. The < WAIT > message is		
Code 54 57 58	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit < DEL> message next. The Hit < DEL> message is cleared. The < WAIT> message is displayed.		
Code 54 57 58	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit < DEL> message next. The Hit < DEL> message is cleared. The < WAIT> message is displayed. Staring the DMA and interrupt controller test next.		
Code 54 57 58	Entering real mode next. Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit < DEL> message next. The Hit < DEL> message is cleared. The < WAIT> message is displayed.		
54 57 58 59	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit message next. The Hit message is cleared. The <wait> message is displayed. Staring the DMA and interrupt controller test next. The DMA page register test passed. To do DMA#1 base register test.</wait>		
Code 54 57 58	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit message next. The Hit message is cleared. The <wait> message is displayed. Staring the DMA and interrupt controller test next. The DMA page register test passed. To do DMA#1 base register</wait>		
54 57 58 59 60 62	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit message next. The Hit message is cleared. The <wait> message is displayed. Staring the DMA and interrupt controller test next. The DMA page register test passed. To do DMA#1 base register test. DMA#1 base register test passed. To do DMA#2 base register test.</wait>		
Code 54 57 58 59 60 62 65	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit message next. The Hit message is cleared. The <wait> message is displayed. Staring the DMA and interrupt controller test next. The DMA page register test passed. To do DMA#1 base register test. DMA#1 base register test passed. To do DMA#2 base register test. DMA#2 base register test passed. To program DMA unit 1 and 2.</wait>		
54 57 58 59 60 62	Description Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next. The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next. The memory size was adjusted for relocation and shadowing. Clearing the Hit message next. The Hit message is cleared. The <wait> message is displayed. Staring the DMA and interrupt controller test next. The DMA page register test passed. To do DMA#1 base register test. DMA#1 base register test passed. To do DMA#2 base register test.</wait>		

7F	Extended NMI sources enabling is in progress.		
80	The keyboard test has started. Clearing the output buffer and		
	checking for stuck keys. Issuing the keyboard reset command		
	next.		
81	A keyboard reset error or stuck key was found. Issuing the		
	keyboard		
	Controller interface test command next.		
82	The keyboard controller interface test completed. Writing the		
	command byte and initializing the circular buffer next.		
83	Command byte written, Global data init done. To check for		
	lock-key.		
84	Locked key checking is over. Checking for a memory size		
	mismatch with		
	CMOS RAM data next.		
85	The memory size check is done. Displaying a soft error and		
0.4	checking for a password or bypassing Setup next.		
86	Password checked. About to do programming before setup.		
87	The programming before Setup has completed. Uncompressing		
00	the Setup code and executing the AMIBIOS Setup utility next.		
88	Returned from CMOS setup program and screen is cleared.		
00	About to do programming after setup.		
89	The programming after Setup has completed. Displaying the power on		
	Screen message next.		
8B			
OB	The first screen message has been displayed. The <wait></wait>		
	message is displayed. Performing the PS/2 mouse check and		
0.1.	extended BIOS data area allocation check next.		
Code	Description		
8C	Programming the Setup options next.		
8D	Going for hard disk controller reset.		
8F	Hard disk controller reset done. Floppy setup to be done next.		
91	The floppy drive controller has been configured. Configuring the		
95	hard disk drive controller next.		
	Initializing the bus option ROMs from C800 next.		
96 97	Initializing before passing control to the adaptor ROM at C800.		
97	Initialization before the C800 adaptor ROM gains control has completed.		
	The adaptor ROM check is next.		
98	The adaptor ROM trick is rickt. The adaptor ROM had control and has now returned control to		
70	BIOS POST.		
	Performing any required processing after the option ROM		
	returned control.		
99	Any initialization required after the option ROM test has		
, ,	completed.		
L	lacture.		

	Configuring the timer data area and printer base address next.		
9A	Return after setting timer and printer base address. Going to set		
	the RS-232 base address.		
9B	Returned after setting the RS-232 base address. Performing a		
	required initialization before the Coprocessor test next.		
9C	Required initialization before the Coprocessor test is over.		
	Initializing the		
	Coprocessor next.		
9D	Coprocessor initialized. Going to do any initialization after		
	Coprocessor test.		
9E	Initialization after the Coprocessor test is complete. Checking		
	the extended keyboard, keyboard ID, and Num Lock key next.		
4.0	Issuing the keyboard ID command next.		
A2	Displaying any soft errors next.		
А3	Soft error display complete. Going to set keyboard typematic		
Λ.4	rate.		
A4 A5	Keyboard typematic rate set. To program memory wait states.		
A5	Memory wait state programming is over. Clearing the screen and		
A7	enabling parity and the NMI next.		
A/	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.		
A8	Initialization before passing control to the adaptor ROM at		
Ao	E000h completed.		
	Passing control to the adaptor ROM at E000h next.		
A9	Returned from adaptor ROM at E000h control. Performing any		
/ / /	initialization required after the E000 option ROM had control		
	next.		
AA	Initialization after E000 option ROM control has completed.		
, , ,	Displaying the system configuration next.		
AB	Building the multiprocessor table, if necessary.		
AC	Uncompressing the DMI data and initializing DMI POST next.		
BO	The system configuration is displayed.		
B1	Copying any code to specific areas.		
00	Code copying to specific areas is done. Passing control to INT 19		
	h boot		
	loader next.		
_			

Flash BIOS Utility

Utilize AMI Flash BIOS programming utility to update on-board BIOS for the future new BIOS version. Please contact your technical window to get this utility if necessary.

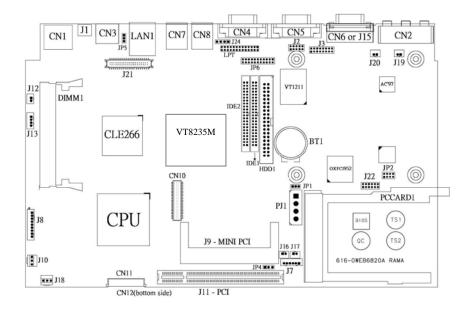
NOTE: Remark or delete any installed Memory Management Utility (such as HIMEM.SYS, EMM386.EXE, QEMM.EXE, ..., etc.) in the CONFIG.SYS files before running Flash programming utility.

Appendix A. Jumper Setting and Connectors List of CPU Board

This appendix gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on WBX-6200F-V are in the proper position. The default settings shipped from factory are marked with (default).

Jumpers Location and list

In general, jumpers on the single board computer are used to select options for certain features. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connect".



Jumper List

CONNECTOR	FUNCTION	REMARK
JP1	RTC CMOS Clear Jumper	1x3 pin header,
JFT		Pitch=2mm
JP2	Touch Screen configuration	2x4 pin header,
JP2		Pitch=2mm
JP4	3.3V or 5V Panel Power	1x3 pin header,
JP4	select	Pitch=2mm
JP5	DVI port configuration	1x3 pin header,
JPS	-	Pitch=2mm
JP6	COM2 RS-232/422/485	2x11 pin header,
JPO	select	Pitch=2mm

Jumper Setting

Jumper Notes

To close or enable a setting, put a jumper cap over the jumper pins. To open or disable a setting, make sure there is no jumper cap covering the jumper pins. See the table below for illustration.

Notation	Description	Illustration
CLOSE	Pins 1 & 2 closed	1 2
OPEN	Pins 1 & 2 open	1 0 2
2-3	Pins 2 & 3 closed	1 3

Table Jumper Setting Example

Note: In this chapter, settings which are marked with (default) are default factory settings.

Jumper Setting

RTC CMOS Clear Jumper Setting (JP1)

Jumper Setting	Illustration	Description.		
1-2 (default)	1 00 3	Normal operation		
2-3	1 0-0 3	Clear CMOS contents		

Touch Screen configuration (JP2)

Jumper Setting	imper Setting Description		ON (SHORT)		
1-2	Baud Rate	19200 (default)	9600		
3-4	PNP	Enable (default)	Disable		
5-6	Wire	4,8 (default)	5		
7-8	Wire	5	4,8 (default)		

 $\begin{smallmatrix}2\\0&0&0&0\\1&&&&&&7\end{smallmatrix}$

Default Setting Illustration:

LCD Panel Power select (JP4)

Jumper Setting	Illustration	Description.
1-2	1 🕒 🔾 3	+LCD→5V
2-3 (default)	1 0-0 3	+LCD→3.3V

DVI Port configuration (JP5)

Jumper Setting	Illustration	Description.
1-2 (default)	1 🗀 🔾 3	DVI Port → DVI
2-3	1 0-0 3	DVI Port → TV

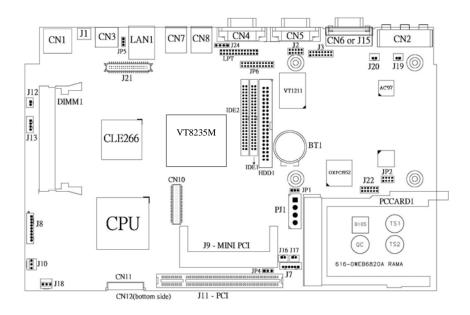
CN4 RS-232/422/485 select (JP6)

Jumper Setting	Illustration	Description.
5-6,9-11,10-12,15-17,16-18	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	RS-232

Jumper Setting	Illustration	Description.
3-4,7-9,8-10,13-15,14-16,21-22	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	RS-422
1-2,7-9,8-10,19-20	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	RS-485

Connector Definitions

Connectors Location



CAUTION:

When connecting the power connector to the motherboard, make sure that the system is not connected to an electrical outlet.

When connecting a signal cable (also called ribbon cable), Pin 1 of the cable should be aligned with Pin 1 of the connector on the motherboard. Pin 1 side of the cable is identified by a color, usually red, stripe. Pin 1 of the motherboard connector is identified by the number 1 imprinted or an additional shading on the board.

Connectors List

The connectors on the PCBA of WBX-6200F-V are used to connect external devices such as hard disk drives, printers, keyboard, CRT, panel, serial ports, etc.

Specifically, the PCBA of *WBX-6200F-V* has the following connectors:

CONNECTOR	FUNCTION	REMARK
J1	Reset Button	
J2	GPIO Connector	2x5 pin header, Pitch=2mm
J3	Internal VGA Connector (Optional)	2x8 pin box header, Pitch=2mm
J4/5/6	N/A	
J7	Inverter Power Connector	
J8	Touch Pad Interface	
J9	Mini-PCI Slot	
J10	CPU Fan Connector	
J11	PCI Slot	
J12	Power Button	
J13	Power & HDD LED	
J14	N/A	
J15	VGA Connector	
J16	Backlight Brightness Control (UP)	(Optional)
J17	Backlight Brightness Control (Down)	(Optional)
J18	System Fan Connector	
J19	Speaker out (Right channel)	2 watts
J20	Speaker out (Left channel)	2 watts
J21	DVI Port	
J22	Internal Serial Port (Optional)	COM1
J24	Internal USB Port	1x4 pin header, Pitch=0.1"

CONNECTOR	FUNCTION	REMARK
JP1	RTC CMOS Clear Jumper	1x3 pin header, Pitch=2mm
JP2	Touch Screen configuration	Pitch=2mm
JP4	3.3V or 5V Panel Power select	1x3 pin header, Pitch=2mm
JP5	DVI port configuration	1x3 pin header, Pitch=2mm
JP6	COM2 RS-232/422/485 select	2x11 pin header, Pitch=2mm
CN1	Power Jack Connector	
CN2	Audio Jack (Line-out, Line-in, Mic)	
CN3	KB/MS 6 pin MINI-DIN female	
CN4	COM2 Serial Port	(RS-232/422/485)
CN5	COM3 Serial Port (RS-232)	
CN6	COM4 Serial Port (RS-232)	
CN7	USB A Port 2/3	
CN8	USB A Port 0/1	
CN9	N/A	
CN10	TTL Panel Connector	
CN11	LVDS1 Panel Connector	
CN12	LVDS2 Panel Connector (optional)	
DIMM1	200Pin DDR SO-DIMM Slot	
HDD1	Primary IDE Connector	40Pin box header, Pitch=0.1"
IDE1	Primary IDE Connector	44Pin box header, Pitch=2mm
IDE2	Secondary IDE Connector	
LAN1	RJ45 LAN connector	
LPT	Internal LPT Port	2x13 pin header
PCCARD1	PCMCIA CardBus Interface	

CONNECTOR	FUNCTION	REMARK
PJ1	HDD Power Connector	

Reset Button (J1)

PIN No.	Signal Description
1	Reset
2	Ground

GPIO Connector (J2)

Pin head on MB

PIN No.	Signal Description	PIN No.	Signal Description
1	1 GPO1 3 GPO2		GPI1
3			GPI2
5	GPO3	6	GPI3
7	7 GPO4		GPI4
9	+5V	10	Ground

Pin head on Chassis

1	2	3	4	5	6	7	8	9	10
+5V	GPO4	GPO3	GPO2	GPO1	Ground	GPI4	GPI3	GPI2	GPI1

Internal VGA Connector (J3-optional)

PIN No.	Name	Description
1	R	Red Video
2	G	Green Video
3	В	Blue Video
4	NC	Not connected
5	DGND	Digital ground

PIN No.	Name	Description
6	R Return	Red ground
7	G Return	Green ground
8	B Return	Blue ground
9	+5V	+5VDC
10	SGND	Sync Ground
11	NC	Not connected
12	SDA	DDC Serial Data Line
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	SCL	DDC Data Clock Line
16	NC	Not connected

Inverter power connector (J7)

PIN No.	Name	Description
1	VCC	+12V
2	VCC	+12V
3	VEEON	Backlight Enable
4	LCD_ ADJ	Brightness control
5	GND	Ground
6	GND	Ground

Touch Pad Interface (J8)

PIN No.	Signal Description		
	8-wire	4-wire	5-wire
1	Right Sense	N/A	N/A
2	Left Sense	N/A	N/A
3	Bottom Sense	N/A	N/A
4	Top Sense	N/A	Sense (S)
5	Right Excite	Right	LR (X)
6	Left Excite	Left	LL (L)
7	Bottom Excite	Bottom	UR (H)
8	Top Excite	Тор	UL (Y)
9	Ground	Ground	Ground

Mini-PCI Slot (J9)

PIN No.	Signal Description	PIN No.	Signal Description
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	Reserved
17	INTB#	18	5V
19	3.3V	20	INTA#
21	Reserved	22	Reserved
23	Ground	24	3.3VAUX
25	CLK	26	RST#
27	Ground	28	3.3V
29	REQ#	30	GNT#
31	3.3V	32	Ground
33	AD [31]	34	PME#
35	AD [29]	36	Reserved
37	Ground	38	AD [30]
39	AD [27]	40	3.3V
41	AD [25]	42	AD [28]
43	Reserved	44	AD [26]
45	C/BE [3]#	46	AD [24]
47	AD [23]	48	IDSEL
49	Ground	50	Ground
51	AD [21]	52	AD [22]
53	AD [19]	54	AD [20]
55	Ground	56	PAR
57	AD [17]	58	AD [18]
59	C/BE [2]#	60	AD [16]
61	IRDY#	62	Ground
63	3.3V	64	FRAME#
65	CLKRUN#	66	TRDY#
67	SERR#	68	STOP#
69	Ground	70	3.3V
71	PERR#	72	DEVSEL#
73	C/BE [1]#	74	Ground
75	AD [14]	76	AD [15]

PIN No.	Signal Description	PIN No.	Signal Description
77	Ground	78	AD [13]
79	AD [12]	80	AD [11]
81	AD [10]	82	Ground
83	Ground	84	AD [09]
85	AD [08]	86	C/BE [0]#
87	AD [07]	88	3.3V
89	3.3V	90	AD [06]
91	AD [05]	92	AD [04]
93	Reserved	94	AD [02]
95	AD [03]	96	AD [00]
97	5V	98	NC
99	AD [01]	100	NC
101	Ground	102	Ground
103	NC	104	M66EN
105	NC	106	NC
107	NC	108	NC
109	NC	110	NC
111	NC	112	Reserved
113	NC	114	Ground
115	NC	116	NC
117	NC	118	NC
119	NC	120	NC
121	Reserved	122	NC
123	VCC5VA	124	3.3VAUX

CPU Fan Connector (J10)

PIN No.	Name	Description
1	GND	Ground
2	VCC	+12V-
3	CPU FAN	CPU FAN

PCI_Slot (J11)

PIN No.	Signal Description	PIN No.	Signal Description
B1	NC	A1	NC
B2	NC	A2	+12V
В3	Ground	А3	NC
B4	NC	A4	NC

PIN No.	Signal Description	PIN No.	Signal Description
B5	+5V	A 5	+5V
В6	+5V	A6	INTR#D
B7	INTR#A	A7	INTR#B
B8	INTR#C	8	+5V
В9	NC	Α9	RSVAD26
B10	REQ#3	A10	+5V
B11	NC	A11	NC
B12	Ground	A12	Ground
B13	Ground	A13	Ground
B14	CLKG2	A14	GNT#3
B15	Ground	A15	RESET#
B16	CLKG	A16	+5V
B17	Ground	A17	GNT#2
B18	REQ#2	A18	Ground
B19	+5V	A19	PME#
B20	AD31	A20	AD30
B21	AD29	A21	NC
B22	Ground	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	Ground
B25	NC	A25	AD24
B26	CBE#3	A26	IDSELD225
B27	AD23	A27	NC
B28	Ground	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	Ground
B31	NC	A31	AD18
B32	AD17	A32	AD16
B33	CBE#2	A33	NC
B34	Ground	A34	FRAME#
B35	IRDY#	A35	Ground
B36	NC	A36	TRDY#
B37	DEVSEL#	A37	Ground
B38	Ground	A38	STOP#
B39	LOCK#	A39	NC
B40	PERR#	A40	PullGround
B41	NC	A41	NC
B42	SERR#	A42	Ground

PIN No.	Signal Description	PIN No.	Signal Description
B43	NC	A43	PAR
B44	CBE#1	A44	AD15
B45	AD14	A45	NC
B46	Ground	A46	AD13
B47	AD12	A47	AD11
B48	AD10	A48	Ground
B49	Ground	A49	AD9
B50	N/A	A50	N/A
B51	N/A	A51	N/A
B52	AD8	A52	CBE#0
B53	AD7	A53	NC
B54	NC	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	Ground
B57	Ground	A57	AD2
B58	AD1	A58	AD0
B59	+5V	A59	+5V
B60	Pull high +5V	A60	Pull high +5V
B61	+5V	A61	+5V
B62	+5V	A62	+5V

Power Bottom (J12)

PIN No.	Name	Description
1	PS_ ON	+5V_SB
2	GND	Through 100 ohm to Ground

Power & HDD LED (J13)

PIN No.	Name	Description
1	HDD_LED	HDD Active
2	VCC	Through 330 ohm to +5V_SB
3	VCC	Through 330 ohm to +5V_SB
4	Power LED	System Power State

LED State	Power off	Power On	HDD Active	S1, S3
Green Pin4→Low	Х	0	0	FLASH
Red Pin1→Low	Х	Х	FLASH	X

VGA connector (J15)

PIN No.	Name	Description
1	R	Red Video
2	G	Green Video
3	В	Blue Video
4	RES	Reserved
5	DGND	Digital ground
6	R Return	Red ground
7	G Return	Green ground
8	B Return	Blue ground
9	+5V	+5VDC
10	SGND	Sync Ground
11	ID0	Monitor ID Bit 0 (optional)
12	SDA	DDC Serial Data Line
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	SCL	DDC Data Clock Line

Backlight Brightness Control (Optional) (J16/J17)

J16 (Raise LCD ADJ)		J17 (Lower LCD ADJ)	
PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	1	BK_DW
2	BK_UP	2	Ground

System Fan Connector (J18)

PIN No.	Name	Description
1	GND	Ground
2	VCC	+12V
3	Chass_FAN	System_FAN

Passive Speaker Connector (2W+2W) (J19, J20)

J19		J20	
PIN No.	Signal Description	PIN No.	Signal Description
1	AMP OUT_R+	1	AMP OUT_L+
2	AMP OUT_R-	2	AMP OUT_L-

DVI Port (J21)

PIN No.	Signal Description	PIN No.	Signal Description
1	N/C	2	N/C
3	Ground	4	Ground
5	DVID0	6	DVID1
7	DVID2	8	DVID3
9	DVID4	10	DVID5
11	DVID6	12	DVID7
13	DVID8	14	DVID9
15	DVID10	16	DVID11
17	Ground	18	Ground
19	+5V	20	+5V
21	Ground	22	+5V
23	PCIRST#	24	Ground
25	N/C	26	N/C
27	N/C	28	N/C
29	N/C	30	N/C
31	N/C	32	DVI_VREF (+2.5V)
33	DVIHSYNC	34	DVIVSYNC
35	DVICLK	36	TVCLKR
37	DVIDET	38	DVIDE
39	SPCLK2	40	SPD2

Internal Serial Port (J22)

PIN No.	Signal Description	PIN No.	Signal Description
1	Data Carrier Detect	2	Data Set Ready
3	Received Data	4	Request To Send
5	Transmit Data	6	Clear To Send
7	Data Terminal Ready	8	Ring Indicator
9	Ground	10	N/C
11	Ground	12	+5V

Internal USB Port (J24)

PIN No.	Name	Description
1	VBUS	+5V
2	D-	USB DATA-
3	D+	USB DATA+
4	GND	Ground

Power Jack Connector (CN1)

PIN No.	Name	Description
1	GND	Ground
2	GND	Ground
3	DC_IN	12V~24V
4	GND	Ground
5	DC_IN	12V~24V

Audio Jack (Line-out, Line-in, Micro) (CN2)

PIN No.	Name	Description
A1	LOUT_R	LOUT_R
A2	SEBTL#	SEBTL#
А3	NC	Not connected
A4	LOUT_L	LOUT_L
A 5	GND	Ground

PIN No.	Name	Description
B1	LINE_R	LINE_R
B2	GND	Ground
В3	GND	Ground
B4	LINE_L	LINE_L
B5	GND	Ground

PIN No.	Name	Description
C1	NC	Not connected
C2	NC	Not connected

PIN No.	Name	Description
C3	GND	Ground
C4	MICPWR	Micro phone
C5	GND	Ground

KB/MS 6 pin MINI-DIN female (CN3)

PIN No.	Name	Description
1	KB DATA	Keyboard data
2	MS DATA	Mouse data
3	GND	Ground
4	VCC	+5V
5	KB CLK	Keyboard clock
6	MS CLK	Mouse clock

COM2 Pin Definition (CN4)

	RS-232			
PIN No.	Signal Description	PIN No.	Signal Description	
1	Data Carrier Detect	2	Received Data	
3	Transmit Data	4	Data Terminal Ready	
5	Ground	6	Data Set Ready	
7	Request To Send	8	Clear To Send	
9	Ring Indicator			
	RS-	422		
PIN No.	Signal Description	PIN No.	Signal Description	
1	Transmit Data (-)	2	Transmit Data (+)	
3	Receive Data (+)	4	Receive Data (-)	
5	Ground	6	Data Set Ready	
7	Request To Send	8	Clear To Send	
9	Ring Indicator			
	RS-	485		
PIN No.	Signal Description	PIN No.	Signal Description	
1	Transmit Data (-)	2	Transmit Data (+)	
3	N/A	4	N/A	
5	Ground	6	Data Set Ready	
7	Request To Send	8	Clear To Send	
9	Ring Indicator			

COM3/4 Pin Definition (CN5/6)

	RS-232			
PIN No.	Signal Description	PIN No.	Signal Description	
1	Data Carrier Detect	2	Received Data	
3	Transmit Data	4	Data Terminal Ready	
5	Ground	6	Data Set Ready	
7	Request To Send	8	Clear To Send	
9	Ring Indicator			

USB A Port 2/3 (CN7)

PIN No.	Name	Description
1	VBUS	+5V
2	D-	Data -
3	D+	Data +
4	GND	Ground

USB A Port 0/1 (CN8)

PIN No.	Name	Description
1	VBUS	+5V
2	D-	Data -
3	D+	Data +
4	GND	Ground

TTL Interface pin assignment (CN10)

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	SHFCLK
3	Ground	4	HSYNC
5	VSYNC	6	Ground
7	B0	8	B1
9	B2	10	B3
11	Ground	12	Ground
13	B4	14	B5
15	B6	16	B7
17	Ground	18	Ground
19	G0	20	G1
21	G2	22	G3
23	Ground	24	Ground
25	G4	26	G5

PIN No.	Signal Description	PIN No.	Signal Description
27	G6	28	G7
29	Ground	30	Ground
31	RO	32	R1
33	R2	34	R3
35	Ground	36	Ground
37	R4	38	R5
39	R6	40	R7
41	Ground	42	Ground
43	N/C	44	N/C
45	DE	46	N/C
47	+LCD (3.3V or 5V)	48	+LCD (3.3V or 5V)
49	Ground	50	Ground

LVDS1 Panel Connector (CN11/CN12)

CN 11		CN 12 (for LVDS second channel)	
PIN No.	Signal Description	PIN No.	Signal Description
1	+LCD (3.3V or 5V)	1	+LCD (3.3V or 5V)
2	+LCD (3.3V or 5V)	2	+LCD (3.3V or 5V)
3	Ground	3	Ground
4	Ground	4	Ground
5	RxIn0-	5	RxIn0-
6	RxIn0+	6	RxIn0+
7	Ground	7	Ground
8	RxIn1-	8	RxIn1-
9	RxIn1+	9	RxIn1+
10	Ground	10	Ground
11	RxIn2-	11	RxIn2-
12	RxIn2+	12	RxIn2+
13	Ground	13	Ground
14	CKIN-	14	CKIN-
15	CKIN+	15	CKIN+
16	Ground	16	Ground
17	RxIn3- (NC for 18bit)	17	RxIn3- (NC for 18bit)
18	RxIn3+ (NC for 18bit)	18	RxIn3+ (NC for 18bit)
19	Ground	19	Ground
20	Ground	20	Ground

200Pin DDR SO-DIMM Slot (DIMM1)

Follow standard 200 pin DDR SO-DIMM Slot standard

Primary IDE Connector (HDD1)

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	NC
21	DMA REQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Pull-down
29	DMA ACK#	30	Ground
31	INT REQ	32	NC
33	DA1	34	ATA_SEL
35	DA0	36	DA2
37	CS0#	38	CS1#
39	HDD Active#	40	Ground

Primary IDE Connector (IDE1)

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12

PIN No.	Signal Description	PIN No.	Signal Description
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	NC
21	DMA REQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Pull-down
29	DMA ACK#	30	Ground
31	INT REQ	32	NC
33	DA1	34	ATA_SEL
35	DA0	36	DA2
37	CS0#	38	CS1#
39	HDD Active#	40	Ground
41	+5V	42	+5V
43	Ground	44	Ground

Secondary IDE Connector (IDE2)

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	NC
21	DMA REQ	22	Ground
23	IOW#	24	Ground
25	IOR#	26	Ground
27	IOCHRDY	28	Pull-down
29	DMA ACK#	30	Ground
31	INT REQ	32	NC
33	DA1	34	ATA_SEL
35	DA0	36	DA2
37	CS0#	38	CS1#

PIN No.	Signal Description	PIN No.	Signal Description
39	HDD Active#	40	Ground
41	+5V	42	+5V
43	Ground	44	Ground

RJ45 LAN connector (LAN1)

PIN No.	Name	Description
1	TX+	Transmit data +
2	TX-	Transmit data -
3	RX+	Receive data +
4	NC	Not connected
5	NC	Not connected
6	RX-	Receive data -
7	NC	Not connected
8	NC	Not connected

Internal LPT Port (LPT)

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe	2	Auto feed
3	Data Bit 0	4	Error
5	Data Bit 1	6	Initialize
7	Data Bit 2	8	Select In
9	Data Bit 3	10	Ground
11	Data Bit 4	12	Ground
13	Data Bit 5	14	Ground
15	Data Bit 6	16	Ground
17	Data Bit 7	18	Ground
19	Acknowledge	20	Ground
21	Busy	22	Ground
23	Paper End	24	Ground
25	Select	26	NC

PCMCIA CardBus Interface (PCCARD1)

Follow standard CardBus Interface standard

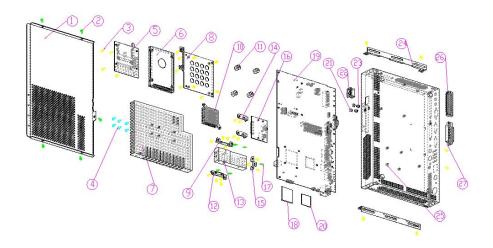
HDD Power Connector (PJ1)

PIN No.	Name	Description
1	VCC	+12V
2	GND	Ground
3	GND	Ground
4	VCC	+5V

Appendix B. System Assembly

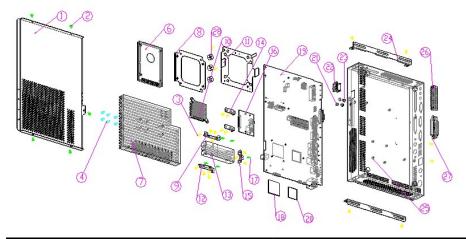
Reference

CF interface:



No	Item Name	Q'ty	No	Item Name	Q'ty
1	Bracket cover	1	15	Bracket CPU-B	1
2	Screw M3x0.5	7	16	DVI board boar	1
3	Screw M3L6	24	17	Screw M3L5	5
4	Washer M3L10	1	18	Heat sink rubber	1
5	CF board	1	19	MB (WEB-6820A)	1
6	Washer M3L10	1	20	Heat sink rubber	1
7	Heat sink base	1	21	Housing LED	1
8	Bracket HDD	1	22	Power switch	1
9	Bracket CPU	1	23	LED	1
10	Heat sink	1	24	Bracket set	1
11	Shock proof	4	25	Bracket bottom	1
12	Bracket CPU-A	1	26	GPIO	1
13	Heat sink	1	27	LPT	1
14	Bracket DVI CPU	1			

PCMCIA interface:



No	Item Name	Q'ty	No	Item Name	Q'ty
1	Bracket cover	1	15	Bracket CPU-B	1
2	Screw M3x0.5	7	16	DVI board boar	1
3	Screw M3L6	24	17	Screw M3L5	5
4	Washer M3L10	1	18	Heat sink rubber	1
		1	19	MB (WEB-6820A)	1
6	Washer M3L10	1	20	Heat sink rubber	1
7	Heat sink base	1	21	Housing LED	1
8	Bracket HDD	1	22	Power switch	1
9	Bracket CPU	1	23	LED	1
10	Heat sink	1	24	Bracket set	1
11	Bracket PCMCIA / CPU	4	25	Bracket PCMCIA bottom	1
12	Bracket CPU-A	1	26	GPIO	1
13	Heat sink	1	27	LPT	1
14	Bracket TV CPU	1	28	damper	1